National Semiconductor

# MICROCIRCUIT DATA SHEET

## MJLF411-X REV 0B0

Original Creation Date: 05/02/95
Last Update Date: 03/31/97
Last Major Revision Date: 05/02/95

# SINGLE OPERATIONAL AMPLIFIER, BI-FET

## General Description

These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

## Industry Part Number

LF411

## NS Part Numbers

JL411BGA
JL411BPA

## Prime Die

LF411

## Controlling Document

38510/11904 REV A

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## Processing

MIL-STD-883, Method 5004

## Quality Conformance Inspection

MIL-STD-833, Method 5005

| Subgrp | Description | Temp ($^{O}$C) |
|---|---|---|
| 1 | Static tests at | +25 |
| 2 | Static tests at | +125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | +25 |
| 5 | Dynamic tests at | +125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | +25 |
| 8A | Functional tests at | +125 |
| 8B | Functional tests at | -55 |
| 9 | Switching tests at | +25 |
| 10 | Switching tests at | +125 |
| 11 | Switching tests at | -55 |
| 12 | Settling time at | +25 |

## Features

| | |
|---|---|
| - Internally trimmed offset voltage | 0.5mV (max) |
| - Input offset voltage drift | 10uV/ C (max) |
| - Low input bias current | 50pA |
| - Low input noise current | 0.01pA/RootHz |
| - Wide gain bandwidth | 3mHz (min) |
| - High slew rate | 10V/uS (min) |
| - Low supply current | 1.8mA |
| - High input impedance | 10E12 Ohms |
| - Low total harmonic distortion Av = 10, Rl = 10K, Vo = 20 Vp-p, BW = 20 Hz - 20KHz | <0.02% |
| - Low 1/f noise corner | 50Hz |
| - Fast settling time to 0.01% | 2uS |

## (Absolute Maximum Ratings)

| | |
|---|---|
| Supply Voltage | ±18V |
| Differential Input Voltage | ±30V |
| Input Voltage Range (Note 1) | ±15V |
| Output Short Circuit Duration | Continuous |
| Power Dissipation (Note 2, 3) | 670mW |
| Tjmax | 175 C |
| ThetaJA | |
| METAL CAN | |
| (Still Air) | 162 C/W |
| (400 LF/Min Air Flow) | 65 C/W |
| CERDIP | |
| (Still Air) | TBD |
| (400 LF/Min Air Flow) | TBD |
| ThetaJC | |
| METAL CAN | 20 C/W |
| CERDIP | TBD |
| Operating Temperature Range | -55 C ≤ TA ≤ +125 C |

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
Note 2: For operating at elevated temperature, these devices must be derated based on a thermal resistance of ThetaJA.
Note 3: Maximum Power Dissipation is defined by the package characteristics. Operating the part near the Maximum Power Dissipation may cause the part to operate outside guaranteed limits.

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage Range | ±5V to ±15V |
| Storage Temperature Range | -65 C ≤ TA ≤ 150 C |
| Lead Temperture | |
| Soldering (10 seconds) | 260 C |
| ESD Tolerance (Note 1) | 2500 |

Note 1: Human body model, 1.5K Ohms in series with 100pF

# Electrical Characteristics

## DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|---|---|---|---|---|---|---|---|---|
| Vio | Input Offset Voltage | +Vcc = 26V, -Vcc = -4V, Vcm = -11V | | | -5 | 5 | mV | 1 |
| | | | | | -7 | 7 | mV | 2, 3 |
| | | +Vcc = 4V, -Vcc = -26V, Vcm = 11V | | | -5 | 5 | mV | 1 |
| | | | | | -7 | 7 | mV | 2, 3 |
| | | | | | -5 | 5 | mV | 1 |
| | | | | | -7 | 7 | mV | 2, 3 |
| | | ±Vcc = ±5V | | | -5 | 5 | mV | 1 |
| | | ±Vcc = ±5V | | | -7 | 7 | mV | 2, 3 |
| +Iib | Input Bias Current | +Vcc = 26V, -Vcc = -4V, Vcm = -11V, t ≤ 25mS | | | -0.4 | 0.2 | nA | 1 |
| | | +Vcc = 26V, -Vcc = -4V, Vcm = -11V, t ≤ 25mS | | | -10 | 50 | nA | 2 |
| | | t ≤ 25mS | | | -0.2 | 0.2 | nA | 1 |
| | | t ≤ 25mS | | | -10 | 50 | nA | 2 |
| | | +Vcc = 4V, -Vcc = -26V, Vcm = 11V, t ≤ 25mS | | | -0.2 | 1.2 | nA | 1 |
| | | +Vcc = 4V, -Vcc = -26V, Vcm = 11V, t ≤ 25mS | | | -10 | 70 | nA | 2 |
| -Iib | Input Bias Current | +Vcc = 26V, -Vcc = -4V, Vcm = -11V, t ≤ 25mS | | | -0.4 | 0.2 | nA | 1 |
| | | +Vcc = 26V, -Vcc = -4V, Vcm = -11V, t ≤ 25mS | | | -10 | 50 | nA | 2 |
| | | t ≤ 25mS | | | -0.2 | 0.2 | nA | 1 |
| | | t ≤ 25mS | | | -10 | 50 | nA | 2 |
| | | +Vcc = 4V, -Vcc = -26V, Vcm = 11V, t ≤ 25mS | | | -0.2 | 1.2 | nA | 1 |
| | | +Vcc = 4V, -Vcc = -26V, Vcm = 11V, t ≤ 25mS | | | -10 | 70 | nA | 2 |
| Iio | Input Offset Current | t ≤ 25mS | | | -0.1 | 0.1 | nA | 1 |
| | | t ≤ 25mS | | | -20 | 20 | nA | 2 |
| +PSRR | Power Supply Rejection Ratio | +Vcc = 10V to 20V, -Vcc = -15V | | | 80 | | dB | 1, 2, 3 |
| -PSRR | Power Supply Rejection Ratio | +Vcc = 15V, -Vcc = -10V to -20V | | | 80 | | dB | 1, 2, 3 |

# Electrical Characteristics

## DC PARAMETERS:(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|---|---|---|---|---|---|---|---|---|
| CMR | Input Voltage Common Mode Rejection | Vcm = -11V to +11V | | | 80 | | dB | 1, 2, 3 |
| Vio(ADJ)+ | Adjustment for Input Offset Voltage | | | | 8 | | mV | 1, 2, 3 |
| Vio(ADJ)- | Adjustment for Input Offset Voltage | | | | | -8 | mV | 1, 2, 3 |
| Ios+ | Output Short Circuit Current | t ≤ 25ms | | | -80 | | mA | 1, 2, 3 |
| Ios- | Output Short Circuit Current | t ≤ 25ms | | | | 80 | mA | 1, 2, 3 |
| Icc | Supply Current | | | | | 3.5 | mA | 1, 2 |
| | | | | | | 4 | mA | 3 |
| DELTA Vio/ DELTA T | Input Offset Voltage | 25 C ≤ TA ≤ +125 C | 1 | | -30 | 30 | uV/ C | 2 |
| | | -55 C ≤ TA ≤ 25 C | 1 | | -30 | 30 | uV/ C | 3 |
| +Vop | Output Voltage Swing | RL = 10K Ohms | | | 12 | | V | 4, 5, 6 |
| | | RL = 2K Ohms | | | 10 | | V | 4, 5, 6 |
| -Vop | Output Voltage Swing | RL = 10K Ohms | | | | -12 | V | 4, 5, 6 |
| | | RL = 2K Ohms | | | | -10 | V | 4, 5, 6 |
| AVS+ | Open Loop Voltage Gain | RL = 2K Ohms, Vout = 0 to 10V | 2 | | 50 | | K | 4 |
| | | | 2 | | 25 | | K | 5, 6 |
| AVS- | Open Loop Voltage Gain | RL = 2K Ohms, Vout = 0 to -10V | 2 | | 50 | | K | 4 |
| | | | 2 | | 25 | | K | 5, 6 |
| AVS | Open Loop Voltage Gain | RL = 10K Ohms, Vout = ±2V, ±Vcc = ±5V | 2 | | 20 | | K | 4, 5, 6 |

# Electrical Characteristics

## AC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: ±Vcc = ±15V, Vcm = 0V

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|---|---|---|---|---|---|---|---|---|
| SR+ | Slew Rate | Vin = -5V to +5V | 3 | | 7 | | V/uS | 7 |
| | | | 3 | | 5 | | V/uS | 8A, 8B |
| SR- | Slew Rate | Vin = +5V to -5V | 3 | | 7 | | V/uS | 7 |
| | | | 3 | | 5 | | V/uS | 8A, 8B |
| TR(tr) | Transient Response Rise Time | AV = 1, Vin = 50mV, CL = 100pF, RL = 2K Ohms | 3 | | | 200 | nS | 7, 8A, 8B |
| TR(os) | Transient Response Overshoot | AV = 1, Vin = 50mV, CL = 100pF, RL = 2K Ohms | 3 | | | 40 | % | 7, 8A, 8B |
| NI(BB) | Noise Broadband | Bandwidth of 10Hz to 15KHz | 4 | | | 15 | uVrms | 7 |
| NI(PC) | Noise Popcorn | Bandwidth of 10Hz to 15KHz, RS = 100K Ohms | 4 | | | 80 | uVpk | 7 |
| ts(+) | Settling Time | AV = 1 | 3 | | | 1500 | nS | 12 |
| ts(-) | Settling Time | AV = 1 | 3 | | | 1500 | nS | 12 |

## DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V. "Delta calculations performed at group B-5".

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Vio | Input Offset Voltage | | | | -1 | 1 | mV | 1 |
| +Iib | Input Bias Current | | | | -0.1 | 0.1 | nA | 1 |
| -Iib | Input Bias Current | | | | -0.1 | 0.1 | nA | 1 |

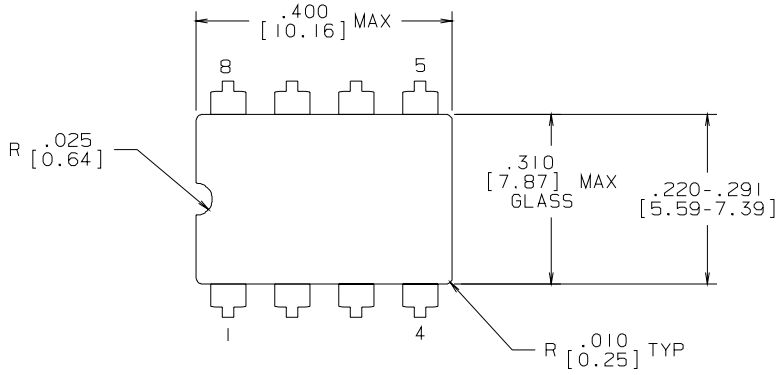
Note 1: Calculated parameter. For calculation use Vio test at ±Vcc = ±15V, Vcm = 0V.
Note 2: Datalog reading in K = V/mV.
Note 3: Bench test, refer to SP-16655.
Note 4: Bench test, refer to SP-16655 or test on J273.

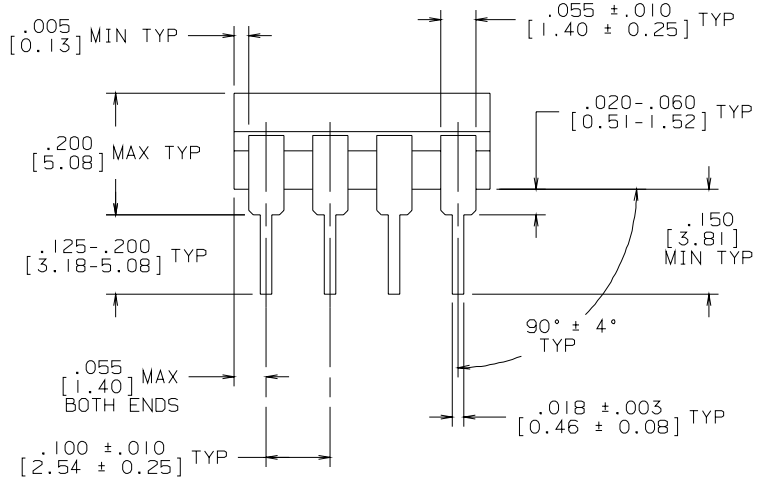
## Graphics and Diagrams

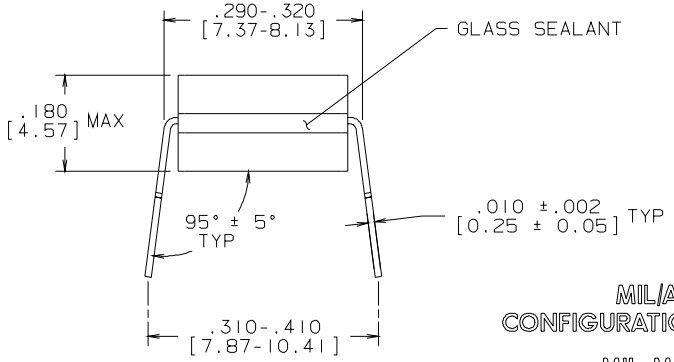
| GRAPHICS# | DESCRIPTION |
|---|---|
| H08CRE | (blank) |
| J08ARL | CERDIP (J), 8 LEAD (P/P DWG) |

**See attached graphics following this page.**

| REVISIONS | | | | |
|---|---|---|---|---|
| LTR | DESCRIPTION | E.C.N. | DATE | BY/APP'D |
| L | REVISE PER CURRENT STD; REDRAW | 10002 | 09/21/93 | TL/ |




MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

| APPROVALS | DATE |
|---|---|
| DRAWN T. LEQUANG | 09/21/93 |
| DFTG. CHK. | |
| ENGR. CHK. | |
| APPROVAL | |

PROJECTION

INCH
[MM]

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# CERDIP (J), 8 LEAD

| SCALE | SIZE | DRAWING NUMBER | REV |
|---|---|---|---|
| N/A | B | MKT-J08A | L |

DO NOT SCALE DRAWING | SHEET 1 OF 1