National Semiconductor

MICROCIRCUIT DATA SHEET

MNLPC660AM-X REV 0A0

Original Creation Date: 08/21/95
Last Update Date: 05/19/98
Last Major Revision Date: 04/23/96

LOW POWER CMOS QUAD OPERATIONAL AMPLIFIER

General Description

The LPC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It features a wide range of operating voltage from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input Vos, drift, and broadband noise as well as voltage gain (into 100k Ohm and 5k Ohm) are all equal to or better than widely accepted bipolar equivalents, while the powewer supply requirement is typically less than 1mW.

This chip is built with Nationals advanced Double-Poly Silicon-Gate CMOS process.

See the LPC662 datasheet for a Dual CMOS operational amplifer and LPC661 datasheet for a single CMOS operational amplifier with these same features.

Industry Part Number

LPC660AM

NS Part Numbers

LPC660AMJ/883*

Prime Die

LPC660

Controlling Document

5962-9202302MCA*

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Rail-to-rail output swing.
- Micropower operation. (1mW)
- Specified for 100k Ohm and 5k Ohm loads.
- High voltage gain. 120dB
- Low input offset voltage. 3mV
- Low offset voltage drift. 1.3uV/ C
- Ultra low input bias current. 2fA
- Input common-mode includes V-.
- Operation range fro +5V to +15V.
- Low distortion. 0.01% at 1kHz
- Slew rate. 0.11 V/uS
- Full military temperature range available.

Applications

- High-impedance buffer.
- Precision current-to-voltage converter.
- long-term integrator.
- High-impedance preamplifier.
- Active filter.
- Sample-and-hold circuit.
- Peak detector.

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage (V+ - V-)	16V
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V+)+0.3V,(V-)-0.3V
Current at Input Pin	±5mA
Current at Output Pin	±18mA
Current at Power Supply Pin	35mA
Maximum Junction Temperature	150 C
Power Dissipation (Note 2)	49mW
Output Short Circuit to V+ (Note 4)	
Output Short Circuit to V- (Note 3)	
Storage Temperature Range	-65 C to +150 C
Operating Temperature Range	-55 C ≤ TA ≤ +125 C
Thermal Resistance (Note 6)	
ThetaJA	
14-Pin CERAMIC DIP (Still Air)	TBD
(500LF/Min Air flow)	TBD
ThetaJC	
14-Pin CERAMIC DIP	TBD
Lead Temperature (Soldering, 10 seconds)	260 C
ESD Tolerance (Note 5)	
(C = 100pF, R = 1.5k Ohms)	1000V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150 C. Output currents in excess of ±30mA over long term may adversely affect reliability.

Note 4: Do not connect output to V+ when V+ is greater than 13V or reliability may be adversely affected.

Note 5: Human body model, 1.5k Ohms in series with 100pF.

Note 6: All numbers apply for packages soldered directly into a PC board.

Recommended Operating Conditions
(Note 1)

Supply Range 4.75V to 15.5V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = +5V, V- = 0V, Vcm = 1.5V, Vo = V+/2, Rl > 1M Ohm, Rs = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage				-3.0	3.0	mV	1
					-3.5	3.5	mV	2, 3
Iib	Input Bias Current				-20	20	pA	1
					-100	100	pA	2, 3
Iio	Input Offset Current				-20	20	pA	1
					-100	100	pA	2, 3
CMRR	Common Mode Rejection Ratio	Vcm = 0V and 12V, V+ = 15V			70		dB	1
					68		dB	2, 3
PSRR+	Positive Power Supply Rejection Ratio	V+ = 5V and 15V, Vo = 2.5V, V- = 0V			70		dB	1
					68		dB	2, 3
PSRR-	Negative Power Supply Rejection Ratio	V- = -10V and 0V, Vo = 2.5V, V+ = 5V			84		dB	1
					82		dB	2, 3
Vcm	Input Common Mode Voltage Range	V+ = 5V and 15V for CMRR $\geq$ 50dB			V+-2.3	-0.1	V	1
		V+ = 5V and 15V for CMRR $\geq$ 50dB			V+-2.6	0	V	2, 3
Icc	Supply Current	All Four Amplifiers Vo = 1.5V			0	200	uA	1
					0	250	uA	2, 3
		V+ = 15V, All Four Amps Vo = 1.5V			0	350	uA	1
					0	450	uA	2, 3
Iout	Output Current V+ = 5V	Sourcing, VO = 0V				-16	mA	1
						-12	mA	2, 3
		Sinking, Vo = 5V			16		mA	1
					12		mA	2, 3
Iout	Output Current V+ = 15V	Sourcing, Vo = 0V				-19	mA	1, 2, 3
		Sinking, Vo = 13V			19		mA	1, 2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = +5V, V- = 0V, Vcm = 1.5V, Vo = V+/2, Rl > 1M Ohm, Rs = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Avol	Large Signal Voltage Gain	Sourcing Vo = 7.5V to 11.5V, V+ = 15V, Rl = 100K Ohm	1		400		V/mV	4
			1		250		V/mV	5, 6
		Sourcing Vo = 7.5V to 11.5V, V+ = 15V, Rl = 5K Ohm	1		200		V/mV	4
			1		150		V/mV	5, 6
		Sinking Vo = 2.5V to 7.5V, V+ = 15V, Rl = 100K Ohm	1		180		V/mV	4
			1		70		V/mV	5, 6
		Sinking Vo = 2.5V to 7.5V, V+ = 15V, Rl = 5K Ohm	1		100		V/mV	4
			1		35		V/mV	5, 6
Vop	Output Swing	V+ = 5V, Rl = 100K Ohm to V+/2			4.97	0.03	V	4
					4.95	0.05	V	5, 6
		V+ = 5V, Rl = 5K Ohm to V+/2			4.85	0.15	V	4
					4.75	0.25	V	5, 6
		V+ = 15V, Rl = 100K Ohm to V+/2			14.92	0.03	V	4
					14.88	0.05	V	5, 6
		V+ = 15V, Rl = 5K Ohm to V+/2			14.68	0.22	V	4
					14.60	0.30	V	5, 6

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V+ = +5V, V- = 0V, Vcm = 1.5V, Vo = V+/2, Rl > 1M Ohm, Rs = 0

+Sr	Slew Rate	V+ = +15V	2		0.07		V/uS	7
			2		0.04		V/uS	8A, 8B
-Sr	Slew Rate	V+ = +15V	3		0.07		V/uS	7
			3		0.04		V/uS	8A, 8B
Gbw	Gain Bandwidth	f = 50KHz			0.1		MHz	7, 8A, 8B

Note 1: Vcm = 7.5V and Rl connected to 7.5V.
Note 2: Connected as Voltage Follower with 0-10V step input. Measurement taken from 4V to 8V.

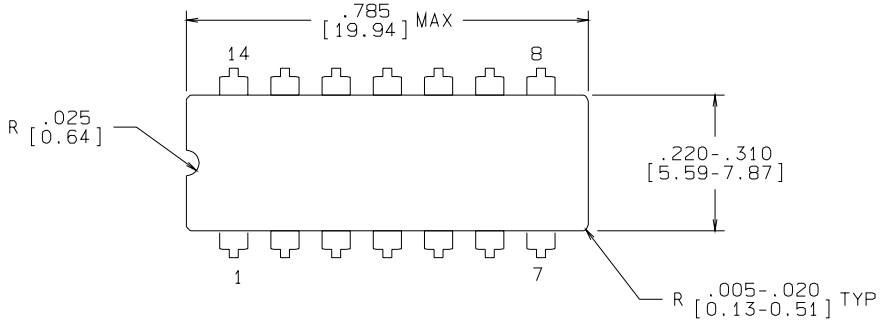
Note 3: Connected as Voltage Follower with 10-0V step input. Measurement taken from 6V to 2V.

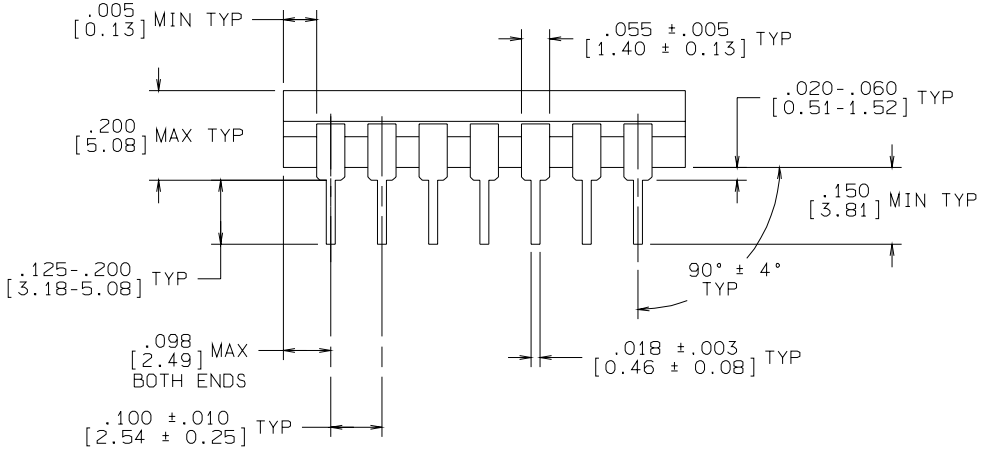
Graphics and Diagrams

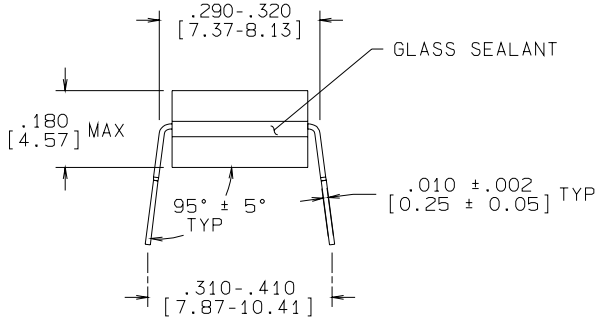
GRAPHICS#	DESCRIPTION
06087HRB4	CERDIP (J), 14 LEAD (B/I CKT)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000350A	CERDIP (J), 14 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

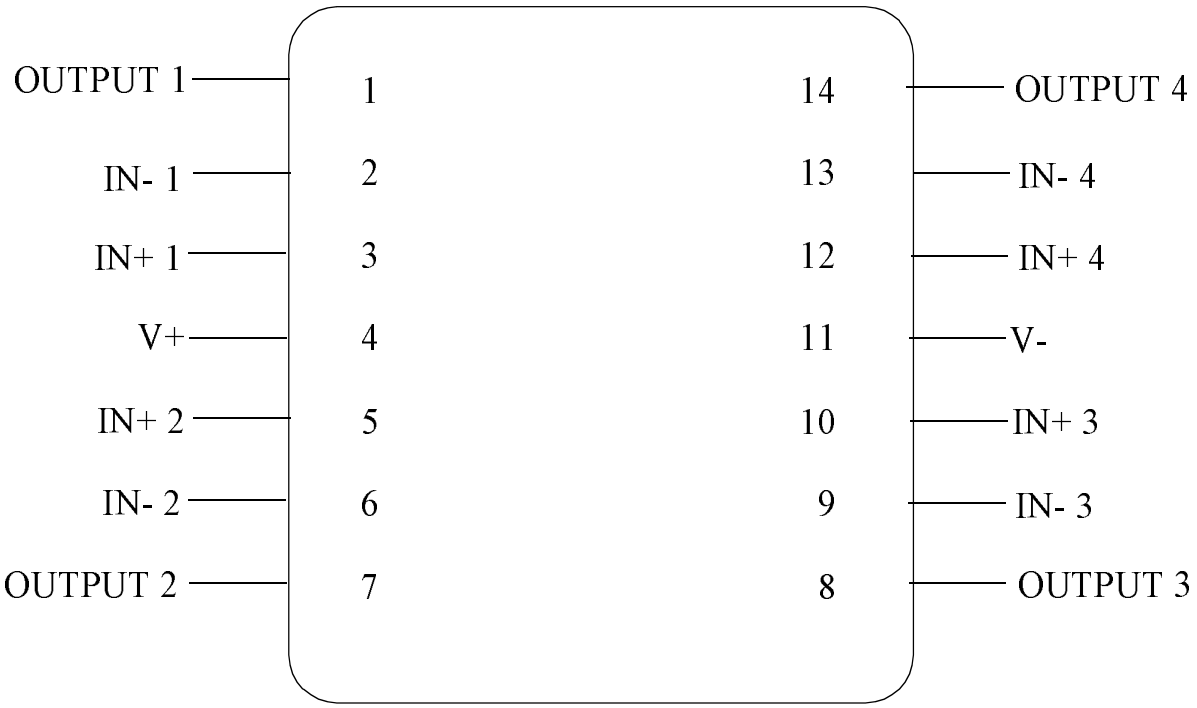
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



LPC660J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000350A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0000611	05/19/98	Barbara Lopez	Update MDS: MNLPC660AM-X Rev. 0AL to MNLPC660AM-X Rev. 0A0. Archive MDS: MNLPC660AM-X Rev. 0AL. Release for Lifetime Buy MDS: MNLPC660AM-X Rev. 0A0.