MC10EP57, MC100EP57

Product Preview

4:1 Differential Multiplexer

The MC10/100EP57 is a fully differential 4:1 multiplexer. By leaving the SEL1 line open (pulled LOW via the input pulldown resistors) the device can also be used as a differential 2:1 multiplexer with SEL0 input selecting between D0 and D1. The fully differential architecture of the EP57 makes it ideal for use in low skew applications such as clock distribution.

The SEL1 is the most significant select line. The binary number applied to the select inputs will select the same numbered data input (i.e., 00 selects D0).

Multiple V_{BB} outputs are provided for single-ended or AC coupled interfaces. In these scenarios, the V_{BB} output should be connected to the data bar inputs and bypassed via a 0.01μF capacitor to ground. Note that the V_{BB} output can source/sink up to 0.5mA of current without upsetting the voltage level. All V_{CC} and V_{EE} pins must be externally connected to power supply to guarantee proper operation

- 350ps Typical Propagation Delays
- Typical Frequency 3.0GHz
- 20–Lead TSSOP Package
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- Internal Input Resistors: Pulldown on D, $\overline{D}$
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >2KV HBM, >100V MM
- V_{BB} Outputs
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Useful as Either 4:1 or 2:1 Multiplexer
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 584 devices

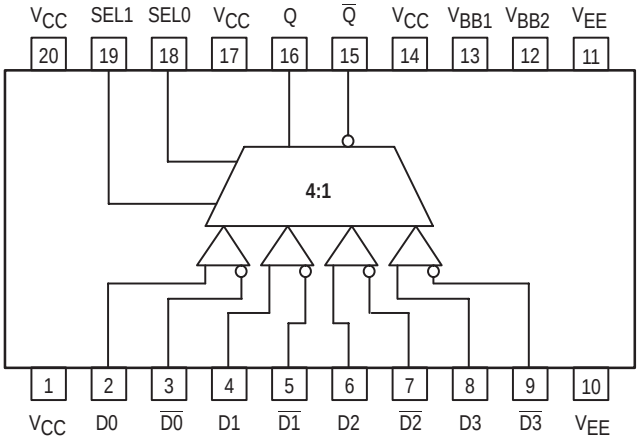

Figure 1. 20–Lead TSSOP (Top View) **and Logic Diagram**

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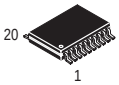
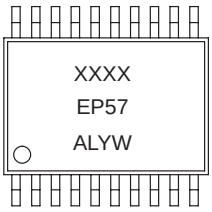


TSSOP–20
DT SUFFIX
CASE 948E

MARKING DIAGRAM



XXXX = MC10 or 100

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
D0–3, $\overline{D0–3}$	ECL Diff. Data Inputs
SEL0, 1	ECL Mux Select Inputs
V_{BB1}, V_{BB2}	ECL Reference Output Voltage
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative, 0 Supply

FUNCTION TABLE

SEL1	SEL0	DATA OUT
L	L	D0, $\overline{D0}$
L	H	D1, $\overline{D1}$
H	L	D2, $\overline{D2}$
H	H	D3, $\overline{D3}$

ORDERING INFORMATION

Device	Package	Shipping
MC10EP57DT	TSSOP	75 Units/Rail
MC10EP57DTR2	TSSOP	2500 Tape & Reel
MC100EP57DT	TSSOP	75 Units/Rail
MC100EP57DTR2	TSSOP	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	140 100	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	23 to 41 ±5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 4.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)					48					mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{BB}	Output Voltage Reference	–1510	–1410	–1310	–1445	–1345	–1245	–1385	–1285	–1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current — SEL, D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 8.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)					48					mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{BB}	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current SEL, D $\overline{D}$	 0.5 –150			 0.5 –150			 0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 12.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)					48					mA
V_{OH}	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
V_{BB}	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current SEL, D $\overline{D}$	 0.5 –150			 0.5 –150			 0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
10. All loading with 50 ohms to V_{CC}–2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}.

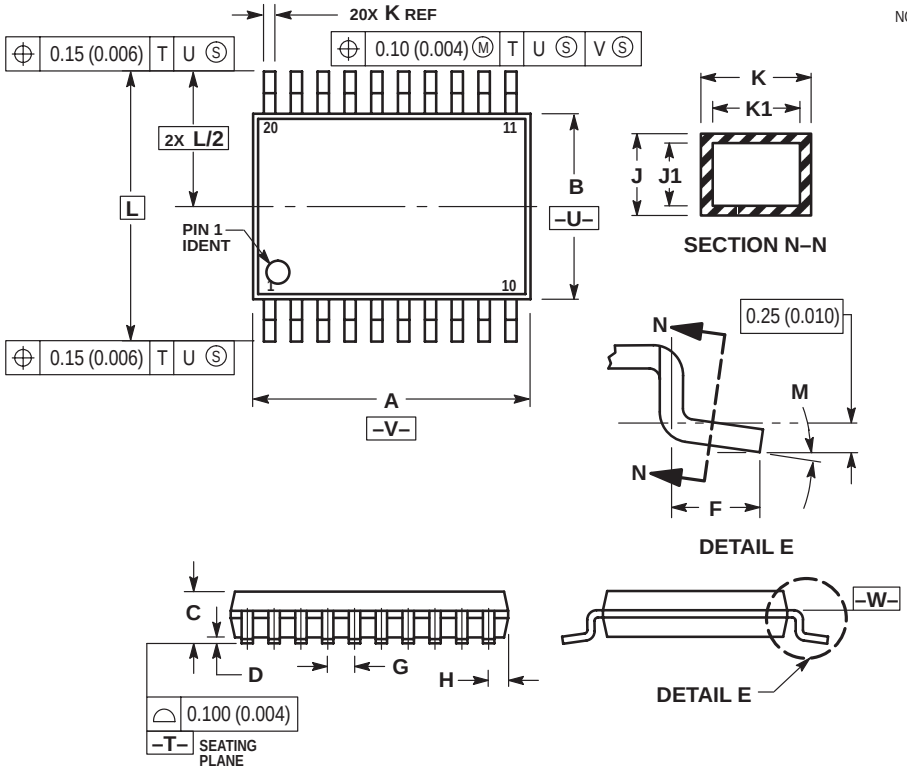
AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 13.)					3.0					GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential										ps
	D–>Q, $\overline{Q}$ (Diff)		TBD			350			TBD		
	D–>Q, $\overline{Q}$ (SE)		TBD			350			TBD		
	SEL–>Q, $\overline{Q}$		TBD			410			TBD		
	COM_SEL–>Q, $\overline{Q}$		TBD			410			TBD		
t_{SKEW}	Within–Device Skew (Note 14.)		TBD			TBD			TBD		ps
	Duty Cycle Skew (Note 15.)		TBD			TBD			TBD		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r	Output Rise/Fall Times Q, $\overline{Q}$		TBD			120			TBD		ps
t_f	(20% – 80%) Q, $\overline{Q}$		TBD			110			TBD		

13. F_{max} guaranteed for functionality only.
14. Within–Device Skew is defined as identical transitions on similar paths through a device.
15. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

PACKAGE DIMENSIONS

TSSOP–20
DT SUFFIX
20 PIN PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

Notes

Notes

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