Product Preview

Unbuffered Inverter

The MC74VHC1GU04 is an advanced high speed CMOS Unbuffered inverter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This device consists of a single unbuffered inverter. In combination with others, or in the MC74VHCU04 Hex Unbuffered Inverter, these devices are well suited for use as oscillators, pulse shapers, and in many other applications requiring a high–input impedance amplifier. For digital applications, the MC74VHC1G04 or the MC74VHC04 are recommended.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The MC74VHC1GU04 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1GU04 to be used to interface 5V circuits to 3V circuits.

- High Speed: tpD = 3.5ns (Typ) at VCC = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- · Balanced Propagation Delays
- · Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V
- · Chip Complexity: 2 FETs or 1 Equivalent Gates

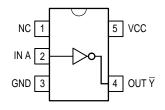
MC74VHC1GU04

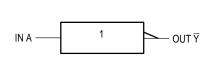


DF SUFFIX5-LEAD SOT-353 PACKAGE SC-88A CASE 419A-01

FUNCTION TABLE

A Input	∀ Output
L	Н
Н	L





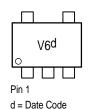


Figure 1. 5-Lead SOT-353 Pinout (Top View)

Figure 2. Logic Symbol

Marking Diagram

DEVICE ORDERING INFORMATION

			Device Nor	nenclature				
Device Order Number	Motorola Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape and Reel Suffix	Package Type	Tape and Reel Size
MC74VHC1GU04DFT1	MC	74	VHC1G	U04	DF	T1	SC-88A	7-Inch/3000 Unit

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS*

Characteristics	Symbol	Value	Unit
DC Supply Voltage	Vcс	−0.5 to +7.0	V
DC Input Voltage	V _{IN}	-0.5 to +7.0	V
DC Output Voltage $V_{CC} = 0$ High or Low State	Vout	-0.5 to 7.0 -0.5 to V _{CC} + 0.5	V
Input Diode Current	lικ	-20	mA
Output Diode Current (VOUT < GND; VOUT > VCC)	lok	+20	mA
DC Output Current, per Pin	lout	+25	mA
DC Supply Current, V _{CC} and GND	lcc	+50	mA
Power dissipation in still air, SC-88A †	PD	200	mW
Lead temperature, 1 mm from case for 10 s	TL	260	°C
Storage temperature	T _{stg}	-65 to +150	°C

^{*} Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute—maximum—rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	Vcc	2.0	5.5	V
DC Input Voltage	V _{IN}	0.0	5.5	V
DC Output Voltage	Vout	0.0	Vcc	V
Operating Temperature Range	T _A	– 55	+125	°C
Input Rise and Fall Time $ \begin{array}{c} \text{V}_{CC} = 3.3 \text{V} \pm 0.3 \text{V} \\ \text{V}_{CC} = 5.0 \text{V} \pm 0.5 \text{V} \\ \end{array} $	t _r , t _f	0 0	No Limit No Limit	ns/V

[†]Derating — SC-88A Package: -5 mW/°C from 65° to 125°C

DC ELECTRICAL CHARACTERISTICS

			VCC	T	A = 25°		T _A ≤	85°C	T _A ≤ 125°C		
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
VIH	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5		1.7 2.4 3.6 4.4			1.7 2.4 3.6 4.4		1.7 2.4 3.6 4.4	V
V _{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5		0.3 0.6 0.9 1.1		0.3 0.6 0.9 1.1		0.3 0.6 0.9 1.1		V
VOH	Minimum High-Level Output Voltage VIN = VIH or VIL	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4mA I _{OH} = -8mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
VOL	Maximum Low–Level Output Voltage VIN = VIH or VIL	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4mA I _{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
IN	Maximum Input Leakage Current	V _{IN} = 5.5V or GND	0 to 5.5			±0.1		±1.0		±1.0	μА
ICC	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5	·		2.0		20		40	μА

AC ELECTRICAL CHARACTERISTICS ($C_{load} = 50 \text{ pF}$, Input $t_r = t_f = 3.0 \text{ns}$)

				T _A = 25°C		T _A ≤ 85°C		TA ≤ '			
Symbol	Parameter	Test Condi	Test Conditions		Тур	Max	Min	Max	Min	Max	Unit
tPLH, tPHL	Maximum Propogation Delay,	$V_{CC} = 3.0 \pm 0.3 V$	C _L = 15 pF C _L = 50 pF		5.0 7.5	8.9 11.4		10.5 13.0		12.0 15.5	ns
	Input A to \overline{Y}	$V_{CC} = 5.0 \pm 0.5 V$	$C_L = 15 pF$ $C_L = 50 pF$		3.5 5.0	5.5 7.0		6.5 8.0		8.0 9.5	
C _{IN}	Maximum Input Capacitance				4	10		10		10	pF

		Typical @ 25°C, V _{CC} = 5.0V	
C _{PD}	Power Dissipation Capacitance (Note 1.)	15	pF

^{1.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no–load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

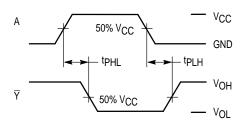
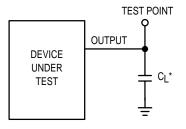


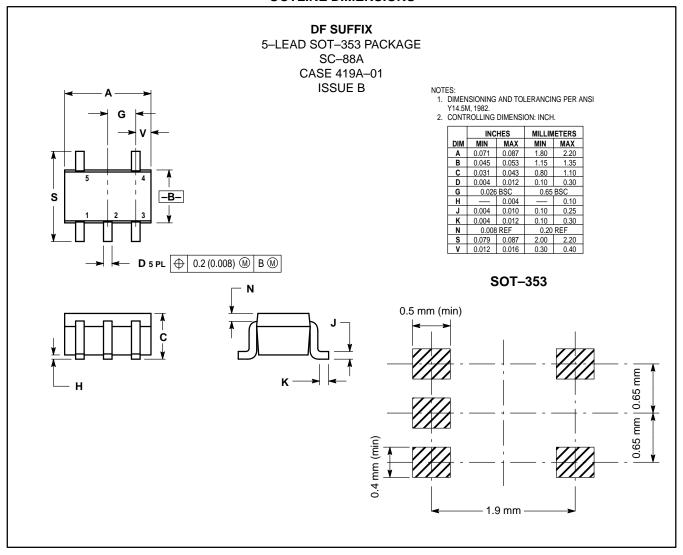
Figure 3. Switching Waveforms



* Includes all probe and jig capacitance

Figure 4. Test Circuit

OUTLINE DIMENSIONS



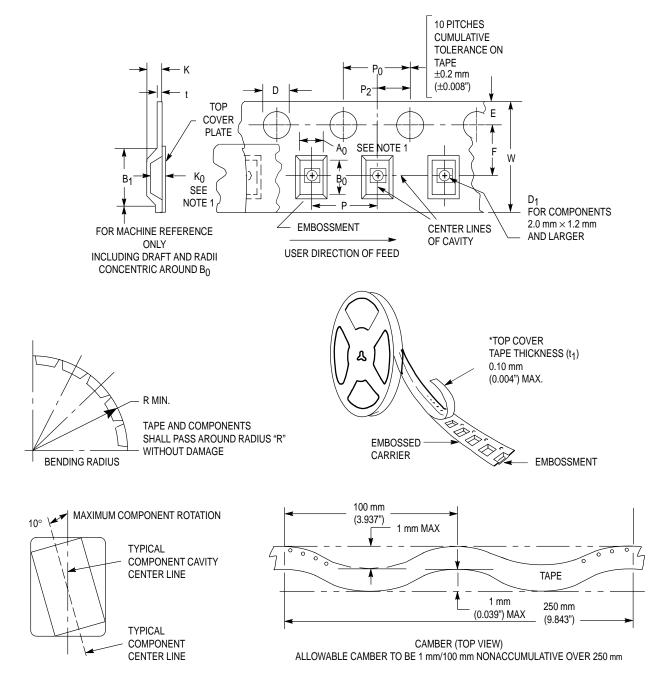


Figure 5. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 1 and 2)

Tape Size	B ₁ Max	D	D ₁	E	F	К	Р	P ₀	P ₂	R	Т	w
8 mm	4.55 mm (0.179")	1.5 +0.1/ -0.0 mm (0.059 +0.004/ -0.0")	1.0 mm Min (0.039")	1.75 ±0.1 mm (0.069 ±0.004")	3.5 ±0.5 mm (1.38 ±0.002")	2.4 mm (0.094")	4.0 ±0.10 mm (0.157 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.1 mm (0.079 ±0.002")	25 mm (0.98")	0.3 ±0.05 mm (0.01 +0.0038/ -0.0002")	8.0 ±0.3 mm (0.315 ±0.012")

^{1.} Metric Dimensions Govern-English are in parentheses for reference only.

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^{2.} A₀, B₀, and K₀ are determined by compnent size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

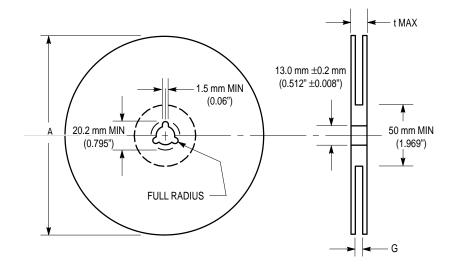


Figure 6. Reel Dimensions

REEL DIMIENSIONS

Tape Size	A Max	G	t Max
8 mm	330 mm	8.400 mm, +1.5 mm, -0.0	14.4 mm
	(14.1")	(0.33", +0.059", -0.00)	(0.56")

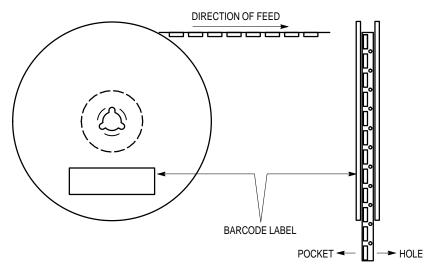


Figure 7. Reel Winding Direction

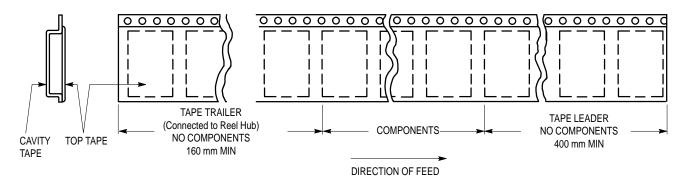


Figure 8. Tape Ends for Finished Goods

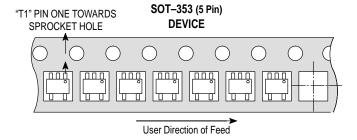


Figure 9. Reel Configuration

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