

SN74LS156

Dual 1-of-4 Decoder/ Demultiplexer

The SN74LS156 is a high speed Dual 1-of-4 Decoder/Demultiplexer. This device has two decoders with common 2-bit Address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs. The LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

The LS156 is fabricated with the Schottky barrier diode process for high speed and are completely compatible with all ON Semiconductor TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Common Address Inputs
- True or Complement Data Demultiplexing
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.75	5.0	5.25	V
T _A	Operating Ambient Temperature Range	0	25	70	°C
V _{OH}	Output Voltage – High			5.5	V
I _{OL}	Output Current – Low			8.0	mA

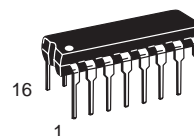


ON Semiconductor

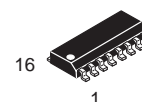
Formerly a Division of Motorola

<http://onsemi.com>

LS156–OPEN–COLLECTOR LOW POWER SCHOTTKY



**PLASTIC
N SUFFIX
CASE 648**



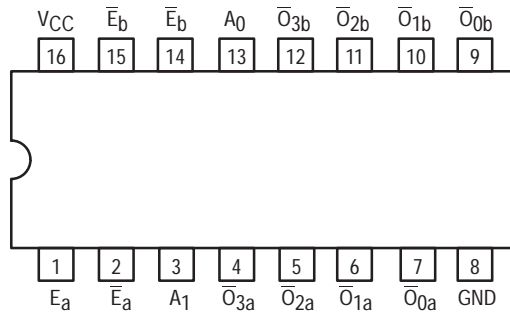
**SOIC
D SUFFIX
CASE 751B**

ORDERING INFORMATION

Device	Package	Shipping
SN74LS156N	16 Pin DIP	2000 Units/Box
SN74LS156D	16 Pin	2500/Tape & Reel

SN74LS156

CONNECTION DIAGRAM DIP (TOP VIEW)



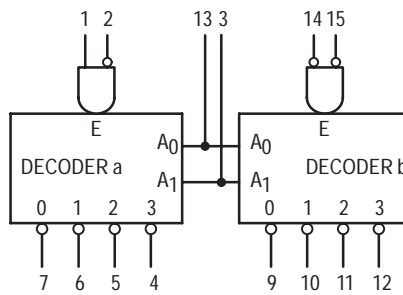
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a)	
		HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
\bar{E}_a, \bar{E}_b	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_a	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\bar{O}_0 - \bar{O}_3$	Active LOW Outputs	10 U.L.	5 U.L.

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

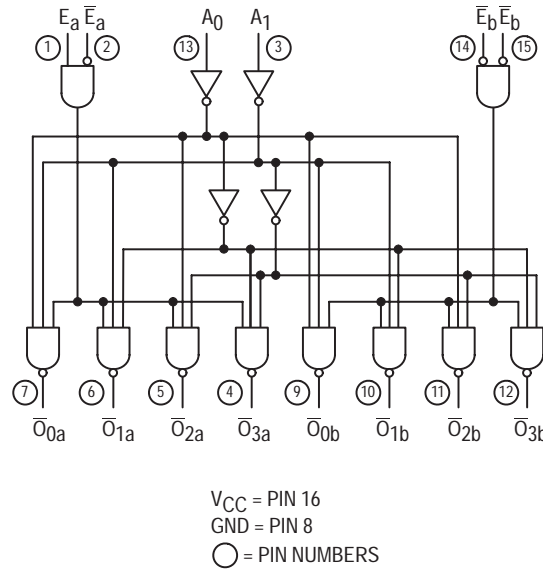
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN74LS156

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS156 is a Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs (A₀, A₁) and provides four mutually exclusive active LOW outputs (\bar{O}_0 – \bar{O}_3). If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Each decoder section has a 2-input enable gate. The enable gate for Decoder “a” requires one active HIGH input and one active LOW input ($E_a \bullet \bar{E}_a$). In demultiplexing applications, Decoder “a” can accept either true or complemented data by using the \bar{E}_a or E_a inputs respectively. The enable gate for Decoder “b” requires two active LOW inputs ($\bar{E}_b \bullet \bar{E}_b$). The LS155 or LS156 can be used as a 1-of-8 Decoder/Demultiplexer by tying E_a to \bar{E}_b and relabeling the common connection as (A₂). The other \bar{E}_b and \bar{E}_a are connected together to form the common enable.

The LS156 can be used to generate all four minterms of two variables. These four minterms are useful in some applications replacing multiple gate functions as shown in

Fig. a. The LS156 has the further advantage of being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (E + A_0 + A_1) \cdot (E + \bar{A}_0 + A_1) \cdot (E + A_0 + \bar{A}_1) \cdot (E + \bar{A}_0 + \bar{A}_1)$$

$$\text{where } E = E_a + \bar{E}_a; \bar{E} = E_b + \bar{E}_b$$

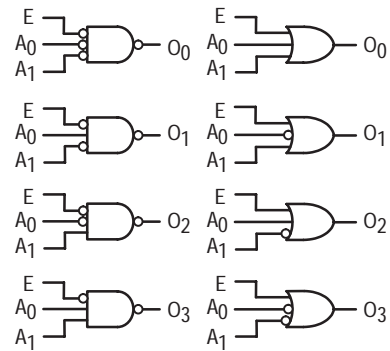


Figure a

TRUTH TABLE

ADDRESS		ENABLE “a”		OUTPUT “a”				ENABLE “b”		OUTPUT “b”			
A ₀	A ₁	E _a	\bar{E}_a	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3	\bar{E}_b	\bar{E}_b	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SN74LS156

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
I_{OH}	Output HIGH Current			100	μA	$V_{CC} = \text{MIN}$, $V_{OH} = \text{MAX}$
V_{OL}	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{CC}	Power Supply Current			10	mA	$V_{CC} = \text{MAX}$

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
t_{PLH} t_{PHL}	Propagation Delay Address, E_A or E_B to Output		25 34	40 51	ns	Figure 1	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$ $R_L = 2.0 \text{ k}\Omega$
t_{PLH} t_{PHL}	Propagation Delay Address to Output		31 34	46 51	ns	Figure 2	
t_{PLH} t_{PHL}	Propagation Delay E_A to Output		32 32	48 48	ns	Figure 1	

AC WAVEFORMS

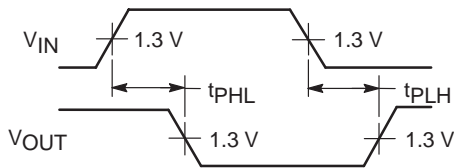


Figure 1.

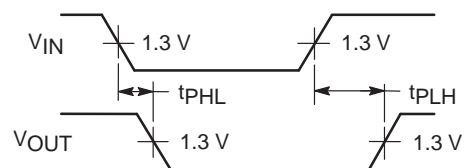
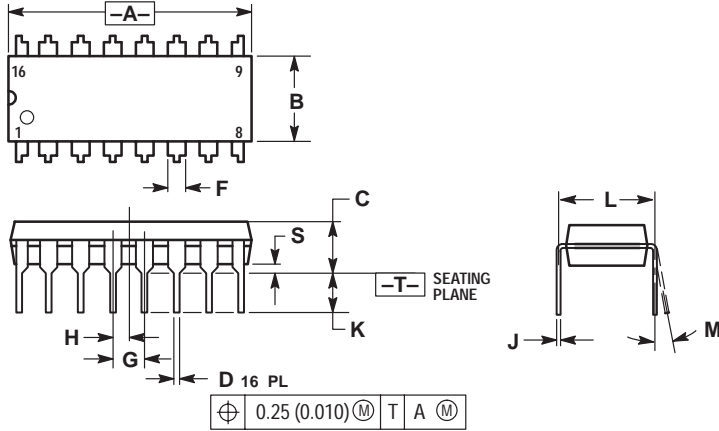


Figure 2.

SN74LS156

PACKAGE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 648-08
ISSUE R



NOTES:

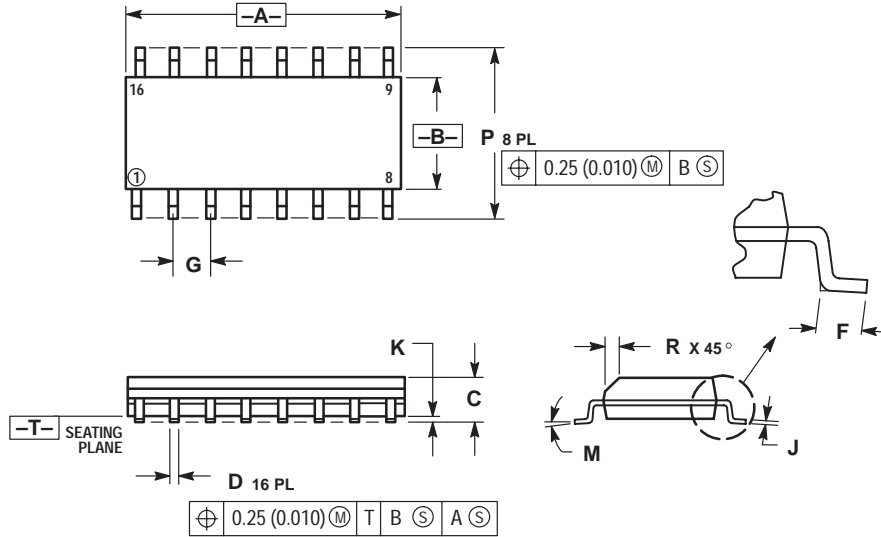
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SN74LS156

PACKAGE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Notes

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