

DATA SHEET

P82B96

Dual bi-directional bus buffer

Product data
Supersedes data of 2001 Mar 06

2003 Feb 20

Dual bi-directional bus buffer

P82B96

FEATURES

- Dual Interface handles both SCL and SDA signals
- Bi-directional data transfer
- Splits I²C signal into forward/reverse Tx, Ty, Rx and Ry signals
- Low power supply current
- Wide supply voltage range (I²C logic levels at Sx Sy independent of IC supply voltage)
- Inhibits data transfer (releases bus) if supply fails.
- Supports 100 kHz clock speed on short busses
- System speeds to 400 kHz where delays permit
- EDS protection exceeds 3500 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up free by design

TYPICAL INTERFACES

- Provides interface between I²C busses operating at different logic levels (e.g., 5 V and 3 V)
- Provides interface between I²C and SMB (350 μ A) bus standard.
- Simple conversion of I²C SDA or SCL signals to multi-drop differential bus hardware, e.g., via compatible PCA82C250.
- Interfaces with Opto-couplers to provide Opto isolation between I²C bus nodes.

DESCRIPTION

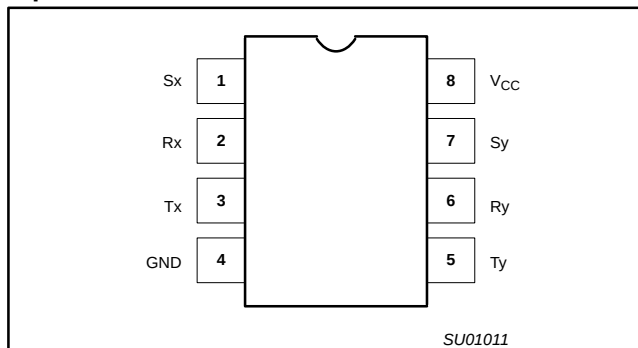
The P82B96 is a bipolar IC which creates a non-latching, bi-directional, logic interface between the normal I²C bus and a range of other bus configurations. It can interface I²C bus logic signals to similar busses having different voltage and current levels.

For example it can interface to the 350 μ A SMB bus, to 3.3 V logic devices, and to 15 V levels and/or low impedance lines to improve noise immunity on longer bus lengths.

It achieves this interface without any restrictions on the normal I²C protocols or 100 kHz clock speed. The IC adds minimal loading to the I²C node, and loadings of the new bus or remote I²C nodes are not transmitted or transformed to the local node. Restrictions on the number of I²C devices in a system, or the physical separation between them, are virtually eliminated. Transmitting SDA/SCL signals via balanced transmission lines (twisted pairs) or with galvanic isolation (opto-coupling) is simple because separate directional Tx and Rx signals are provided. The Tx and Rx signals may be directly connected, without causing latching, to provide an alternative bi-directional signal line with I²C properties.

PIN CONFIGURATIONS

8-pin dual in-line or SO



PINNING

SYMBOL	PIN	DESCRIPTION
Sx	1	I ² C Bus (SDA or SCL)
Rx	2	Receive signal
Tx	3	Transmit signal
GND	4	Negative Supply
Ty	5	Transmit signal
Ry	6	Receive signal
Sy	7	I ² C Bus (SDA or SCL)
V _{CC}	8	Positive supply

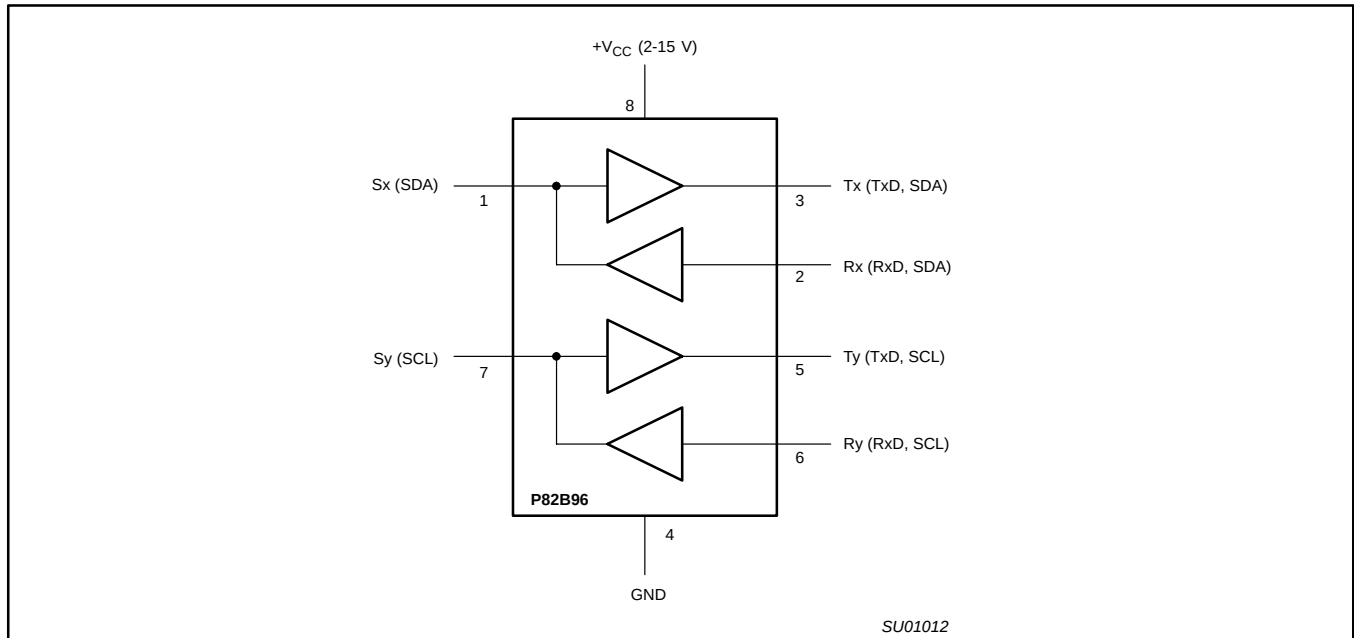
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
P82B96PN	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
P82B96TD	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

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BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The P82B96 has two identical buffers allowing buffering of both of the I²C (SDA and SCL) signals. Each buffer is made up of two logic signal paths, a forward path from the I²C interface pin which drives the buffered bus, and a reverse signal path from the buffered bus input to drive the I²C bus interface.

Thus these paths are:

1. Sense the voltage state of the I²C pin Sx (or Sy) and transmit this state to the pin Tx (Ty resp.), and
2. Sense the state of the pin Rx (Ry) and pull the I²C pin low whenever Rx (Ry) is low.

The rest of this discussion will address only the "x" side of the buffer: the "y" side is identical.

The I²C pin (Sx) is designed to interface with a normal I²C bus.

The logic threshold voltage levels on the I²C bus are independent of the IC supply V_{CC}. The maximum I²C bus supply voltage is 15 V and the guaranteed static sink current is 3 mA.

The logic level of Rx is determined from the power supply voltage V_{CC} of the chip. Logic LOW is below 42 % of V_{CC} and logic HIGH is above 58 % of V_{CC}: with a typical switching threshold of half V_{CC}.

Tx is an open collector output without ESD protection diodes to V_{CC}. It may be connected via a pull-up resistor to a supply voltage in excess of V_{CC}, as long as the 15 V rating is not exceeded. It has a larger current sinking capability than a normal I²C device, being able to sink a static current of greater than 30 mA, and typical 100 mA dynamic pull-down capability as well.

A logic LOW is only transmitted to Tx when the voltage at the I²C pin (Sx) is below 0.6 V. A logic LOW at Rx will cause the I²C bus (Sx) to be pulled to a logic LOW level in accordance with I²C requirements (max. 1.5 V in 5 V applications) but not low enough to be looped back to the Tx output and cause the buffer to latch low.

The minimum LOW level this chip can achieve on the I²C bus by a LOW at Rx is typically 0.8 V.

If the supply voltage V_{CC} fails then neither the I²C nor the Tx output will be held low. Their open collector configuration allows them to be pulled up to the rated maximum of 15 V even without V_{CC} present. The input configuration on Sx and Rx also present no loading of external signals even when V_{CC} is not present.

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MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages with respect to pin GND (pin 4).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC} to GND	Supply voltage range V_{CC}	-0.3	+18	V
V_{bus}	Voltage range on I ² C Bus, SDA or SCL	-0.3	+18	V
V_{Tx}	Voltage range on buffered output	-0.3	+18	V
V_{Rx}	Voltage range on receive input	-0.3	+18	V
I	DC current (any pin)	—	250	mA
R_{tot}	Power dissipation	—	300	mW
T_{stg}	Storage temperature range	-55	+125	°C
T_{amb}	Operating ambient temperature range	-40	+85	°C

CHARACTERISTICSAt $T_{amb} = 25\text{ °C}$; Voltages are specified with respect to GND with $V_{CC} = 5\text{ V}$ unless otherwise stated.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Power Supply					
V_{CC}	Supply voltage (operating)	2.0	—	15	V
I_{CC}	Supply current, busses HIGH	—	0.9	1.8	mA
I_{CC}	Supply current at $V_{CC} = 15\text{ V}$, busses HIGH	—	1.1	2.5	mA
I_{CC}	Additional supply current per Tx or Ty LOW	—	1.7	3.5	mA
Bus pull-up (load) voltages and currents					
V_{Sx}, V_{Sy}	Maximum input/output voltage level Open collector I ² C bus and $V_{Rx}, V_{Ry} = \text{HIGH}$	—	—	15	V
I_{Sx}, I_{Sy}	Static output loading on I ² C bus $V_{Sx}, V_{Sy} = 1.2\text{ V}$ $V_{Rx}, V_{Ry} = \text{LOW}$	0.2	—	3	mA
I_{Sx}, I_{Sy}	Dynamic output sink capability on I ² C bus $V_{Sx}, V_{Sy} > 2\text{ V}$ $V_{Rx}, V_{Ry} = \text{LOW}$	7	18	—	mA
I_{Sx}, I_{Sy}	Leakage current on I ² C bus $V_{Sx}, V_{Sy} = 5\text{ V}$, and $V_{Rx}, V_{Ry} = \text{HIGH}$	—	—	1	μA
I_{Sx}, I_{Sy}	Leakage current on I ² C bus $V_{Sx}, V_{Sy} = 15\text{ V}$, and $V_{Rx}, V_{Ry} = \text{HIGH}$	—	1	—	μA
V_{Tx}, V_{Ty}	Maximum output voltage level Open collector	—	—	15	V
I_{Tx}, I_{Ty}	Static output loading on buffered bus $V_{Tx}, V_{Ty} = 0.4\text{ V}$ $V_{Sx}, V_{Sy} = \text{LOW}$ on I ² C bus = 0.4V	—	—	30	mA
I_{Tx}, I_{Ty}	Dynamic output sink capability, buffered bus: $V_{Tx}, V_{Ty} > 1\text{ V}$ $V_{Sx}, V_{Sy} = \text{LOW}$ on I ² C bus = 0.4V	60	100	—	mA
I_{Tx}, I_{Ty}	Leakage current on buffered bus $V_{Tx}, V_{Ty} = V_{CC} = 15\text{ V}$, and $V_{Sx}, V_{Sy} = \text{HIGH}$	—	1	—	μA

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SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Input Currents					
I_{Sx}, I_{Sy}	Input current from I ² C bus, bus LOW $V_{Rx}, V_{Ry} = \text{HIGH}$	—	-1	—	μA
I_{Rx}, I_{Ry}	Input current from buffered bus, bus LOW $V_{Rx}, V_{Ry} = 0.4 \text{ V}$	—	-1	—	μA
I_{Rx}, I_{Ry}	Leakage current on buffered bus input $V_{Rx}, V_{Ry} = V_{CC}$	—	1	—	μA
Input Thresholds					
V_{Sx}, V_{Sy}	Output logic level LOW, on normal I ² C bus $I_{Sx}, I_{Sy} = 3 \text{ mA}$	0.8	0.9	1.0	V
V_{Sx}, V_{Sy}	Output logic level LOW, on normal I ² C bus $I_{Sx}, I_{Sy} = 0.2 \text{ mA}$	—	750	—	mV
V_{Sx}, V_{Sy}	Input logic level LOW threshold On normal I ² C bus	600	650	—	mV
$dV_{Sx}/dT, dV_{Sy}/dT$	Temperature coefficient of thresholds	—	-2	—	mV/K
V_{Rx}, V_{Ry}	Input logic HIGH level Fraction of applied V_{CC}	0.58	—	—	
V_{Rx}, V_{Ry}	Input threshold Fraction of applied V_{CC}	—	0.5	—	
V_{Rx}, V_{Ry}	Input logic LOW level Fraction of applied V_{CC}	—	—	0.42	
Bus Release on V_{CC} Failure					
$V_{Sx}, V_{Sy}, V_{Tx}, V_{Ty}$	V_{CC} voltage at which all busses are guaranteed to be released	—	—	1	V
dV/dT	Temperature coefficient of guaranteed release voltage	—	-4	—	mV/K
Buffer response time					
$T_{\text{fall delay}}$ V_{Sx} to V_{Tx} V_{Sy} to V_{Ty}	Buffer time delay on FALLING input between V_{Sx} = input switching threshold: and V_{Tx} output falling 50%. R_{Tx} pull up = 160 Ω , no capacitive load, $V_{CC} = 5 \text{ V}$	—	100	—	ns
$T_{\text{rise delay}}$ V_{Sx} to V_{Tx} V_{Sy} to V_{Ty}	Buffer time delay on RISING input between V_{Sx} = input switching threshold, and V_{Tx} output reaching 50%. R_{Tx} pull up = 160 Ω , no capacitive load, $V_{CC} = 5 \text{ V}$	—	100	—	ns
$T_{\text{fall delay}}$ V_{Rx} to V_{Sx} V_{Ry} to V_{Sy}	Buffer time delay on FALLING input between V_{Rx} = input switching threshold, and V_{Sx} output falling 50%. R_{Sx} pull up = 1600 Ω , no capacitive load, $V_{CC} = 5 \text{ V}$	—	300	—	ns
$T_{\text{rise delay}}$ V_{Rx} to V_{Sx} V_{Ry} to V_{Sy}	Buffer time delay on RISING input between V_{Rx} = input switching threshold, and V_{Sx} output reaching 50%. R_{Sx} pull up = 1600 Ω , no capacitive load, $V_{CC} = 5 \text{ V}$	—	300	—	ns

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TYPICAL APPLICATIONS

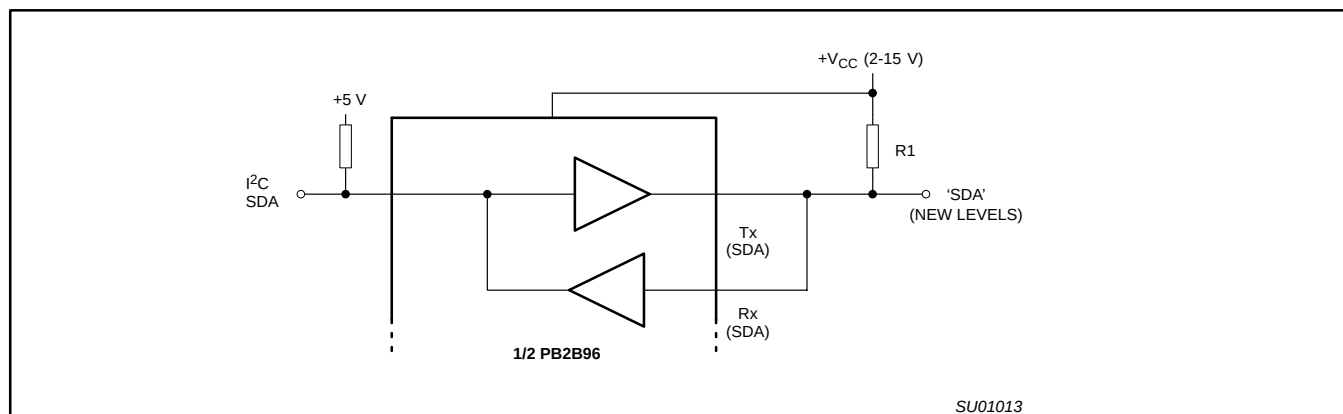
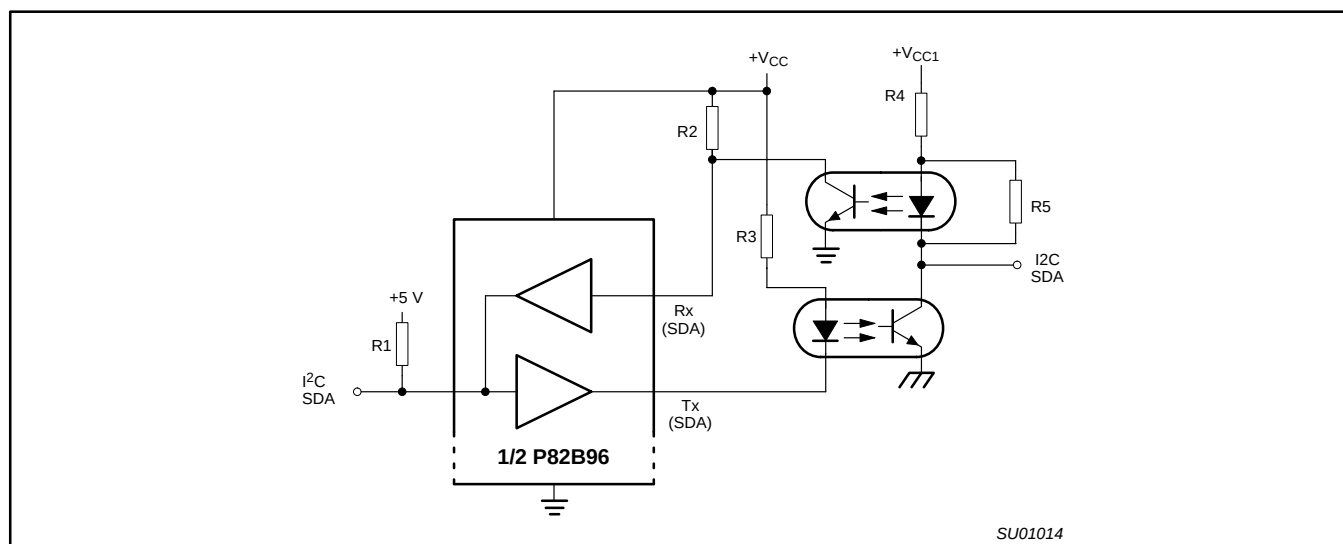


Figure 1. Interfacing an 'I²C' type of bus with different logic levels.

Figure 2. Galvanic isolation of I²C nodes via opto-couplers
(See AN460 and AN255 for more application detail.)

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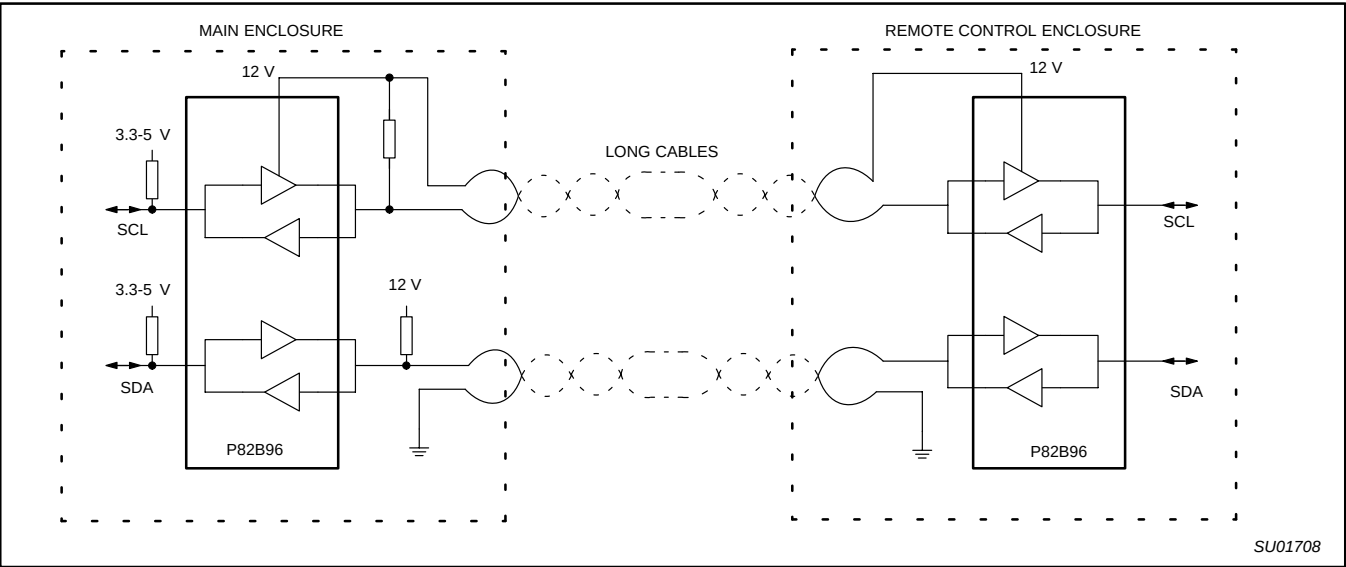


Figure 3. Long distance I²C communications

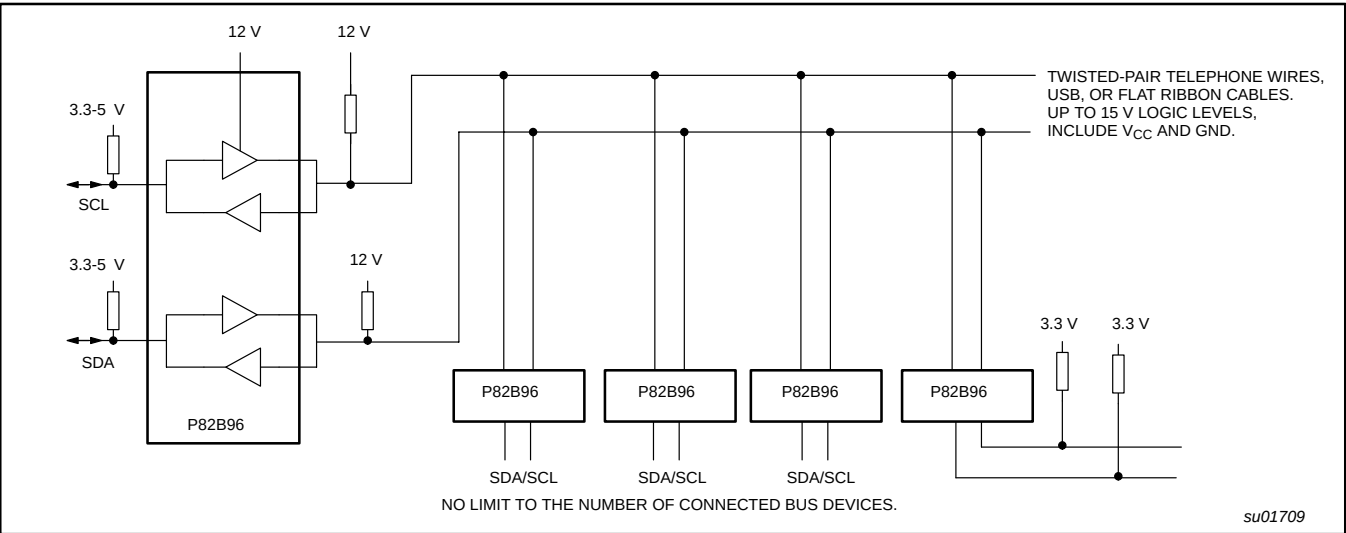


Figure 4. I²C multi-point applications

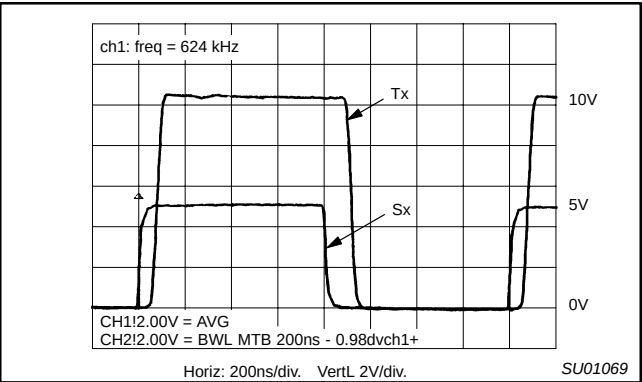


Figure 5. Propagation Sx to Tx — Sx pull-up to 5V, Tx pull-up to V_{CC} = 10 V

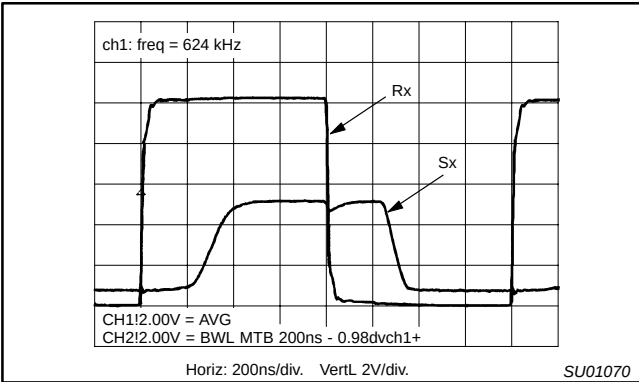


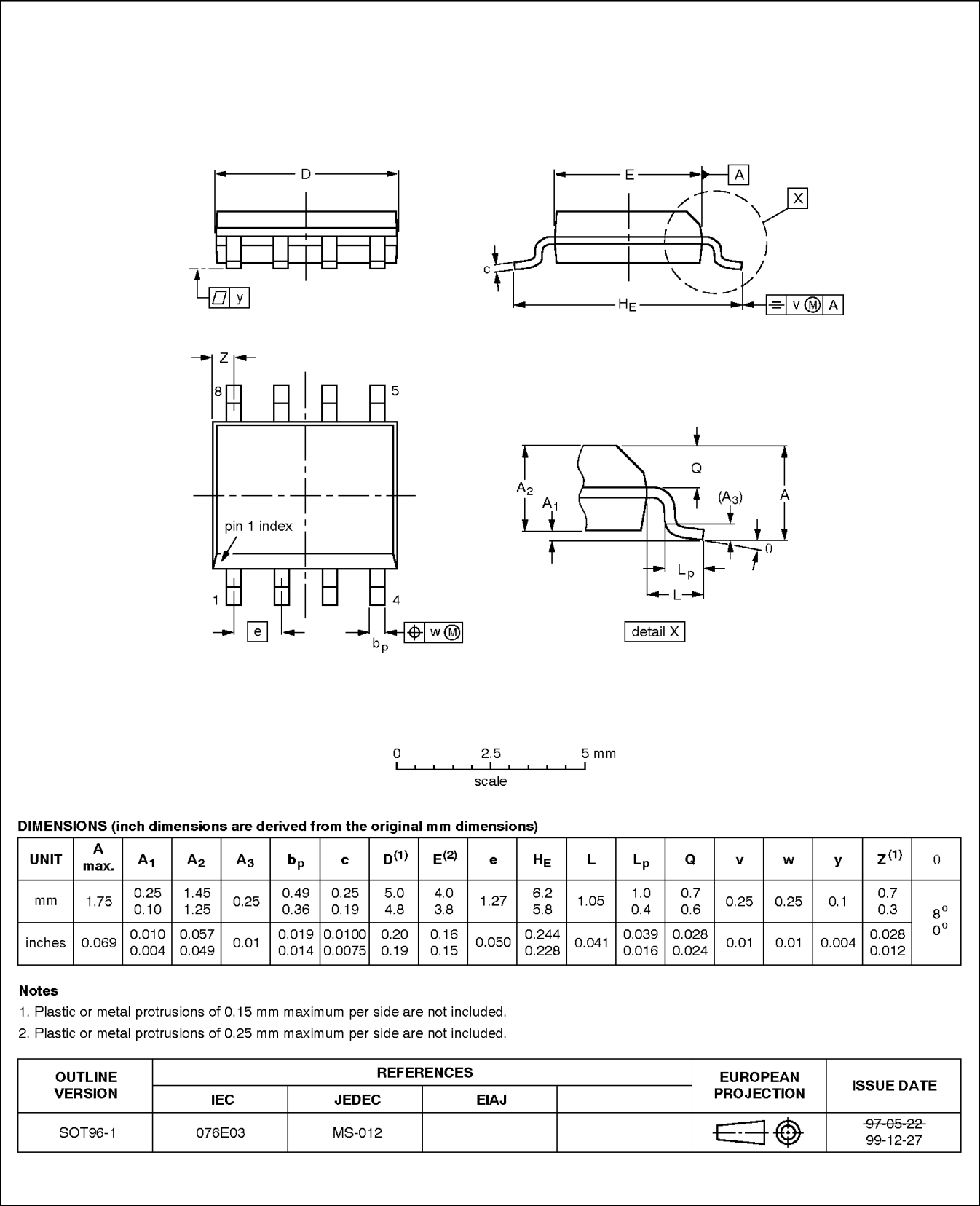
Figure 6. Propagation Rx to Sx — Sx pull-up to 5V, Rx pull-up to V_{CC} = 10 V

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SO8: plastic small outline package; 8 leads; body width 3.9 mm

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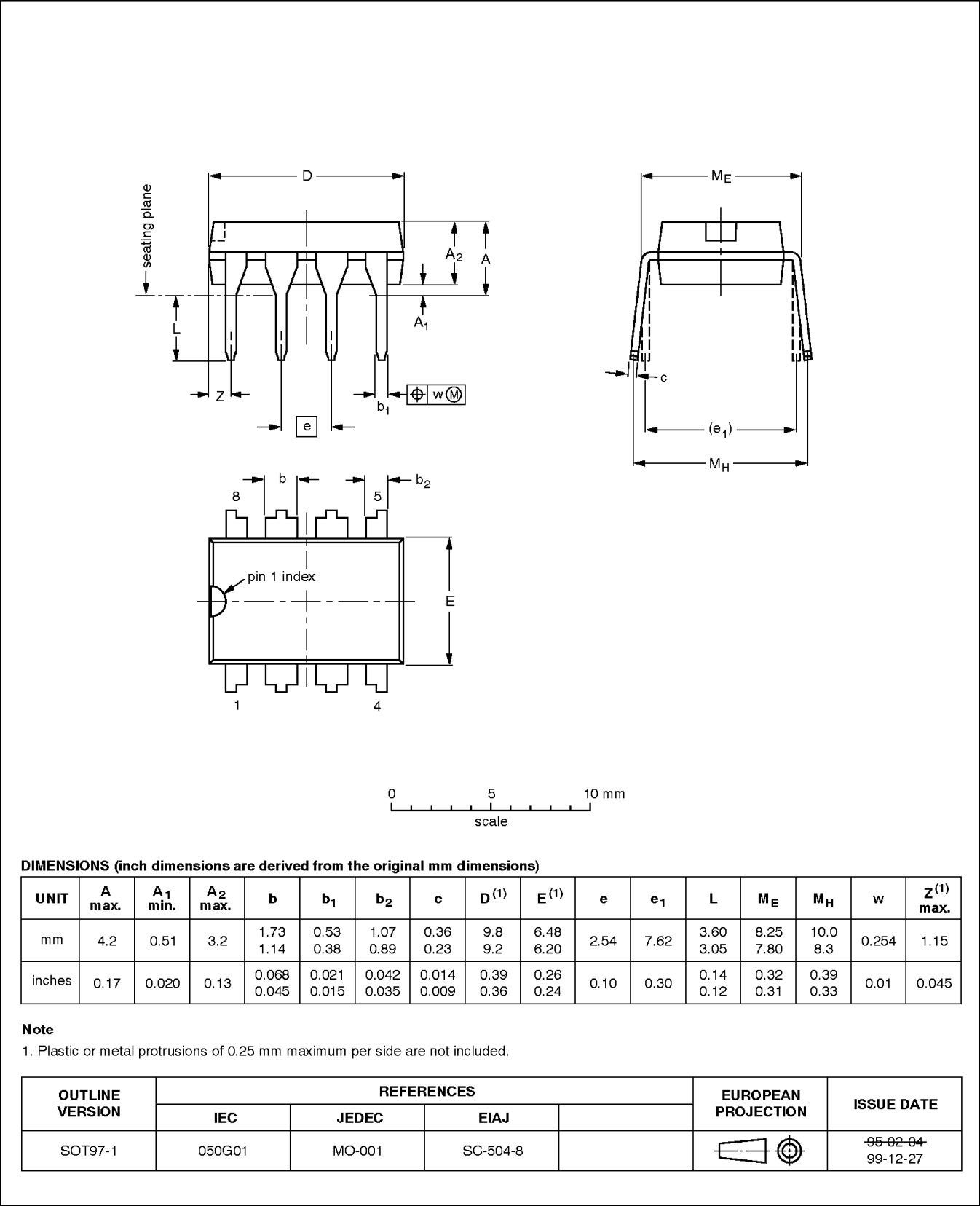


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DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1



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REVISION HISTORY

Rev	Date	Description
_2	20030220	Product data (9397 750 11093); ECN 853-2241 29410 of 22 January 2003; supersedes data of 2001 Mar 06 (9397 750 08122) Modifications: • Pin capacitance added
_1	20010306	Product data (9397 750 08122); ECN 853-2241 25758 of 2001 Mar 06.

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Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
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