

System Reset Monolithic IC PST623

Outline

This low reset type IC functions in CPU and other logic systems to detect input voltage and reset the system accurately when power is turned on or interrupted.

Features

1. Detection voltage can be set easily (2 external resistors)
2. High precision voltage detection Internal reference voltage 1.25±2%
3. Enables high voltage check (at stage before Reg)
4. Low operating limit voltage 0.65V typ.
5. High output current during ON 10mA min.
6. Low current consumption 40µA typ.
7. Built-in delay circuit (1 external capacitor)

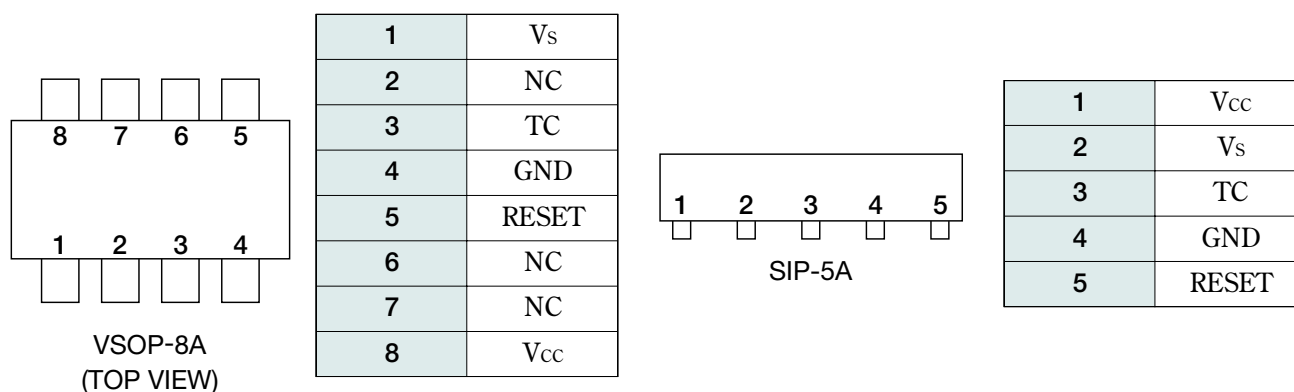
Applications

1. Reset circuits in microcomputers, CPUs and MPUs
2. Logic circuit reset circuits
3. Level detection circuits

Package

VSOP-8A (PST623XW)
 SIP-5A (PST623XS)

Pin Assignment



Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Units
Storage temperature	T _{STG}	-40~+125	°C
Maximum power supply voltage	V _{CC} max.	10	V
Allowable power consumption	P _d max.	300	mW
Input pin voltage	V _{ID}	-0.3~V _{CC}	V

Recommended Operating Conditions

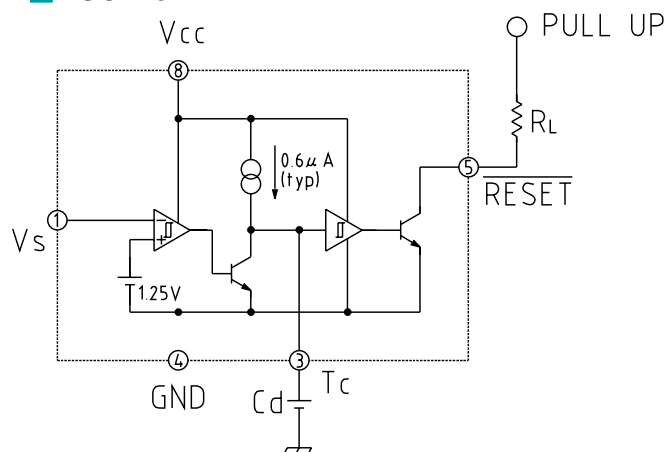
Item	Symbol	Rating	Units
Power supply voltage	V _{CCOP}	2.0~10.0	V
Operating temperature	T _{OPG}	-25~+75	°C

Electrical Characteristics (V_{CC}=5V, Ta=25°C) (Except where noted otherwise, resistance unit is Ω)

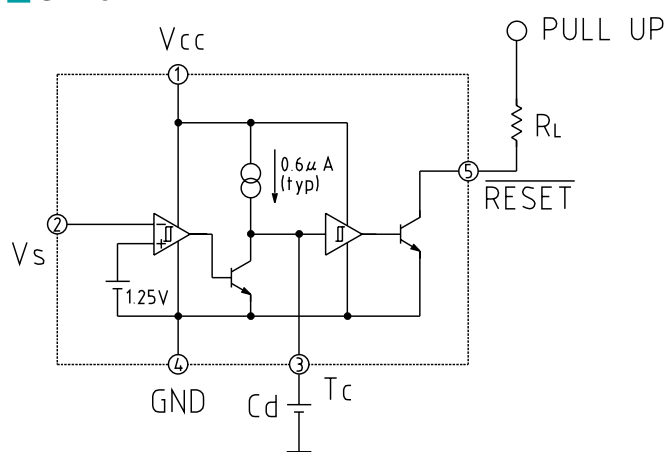
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Detection reference voltage	V _S	R _L =470, V _{IN} =H→L	1.225	1.250	1.275	V
Hysteresis voltage	ΔV _S	R _L =470, V _{IN} =L→H→L	12	25	50	mV
Detection reference voltage temperature coefficient	$\frac{V_S}{\Delta T}$	R _L =470, Ta=-25~+75°C		±0.01		%/°C
Low level output voltage	V _{OL}	V _{IN} =1.0V, R _L =470		0.3	0.45	V
Output leakage current	I _{OH}	V _{IN} =1.5V, V _{OUT} =10V			±0.1	μA
Circuit current while on	I _{CCL}	V _{IN} =1.0V, R _L =∞		50	90	μA
Circuit current while off	I _{CCH}	V _{IN} =1.5V, R _L =∞		42	70	μA
"H" transport delay time	tp _{LH}	R _L =4.7k, C _d =0.047μF		110		ms
"L" transport delay time	tp _{HL}	R _L =4.7k, C _d =0.047μF		15		μs
Operation limit voltage	V _{OPL}	R _L =4.7k, V _{OL} ≤ 0.4V Minimum power supply voltage for which output can maintain Lo.		0.65	0.85	V
Output current while on	I _{OL}	V _{IN} =1.0V, R _L =0	10			mA
Delay time setting comparator Threshold level	V _{tsh}	R _L =470, V _{TC} =L→H	1.25	1.4	1.55	V
Capacitor charging current	I _{TC}	V _{IN} =1.5V, V _{TC} =0.2V	0.39	0.60	0.81	μA
V _S input current	I _{IN}	V _{IN} =1.35V		40		nA

Equivalent Circuit Diagram

■ VSOP-8A

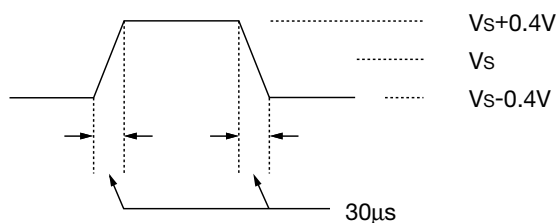


■ SIP-5A



Notes on Using PST623

1. Input voltage rise and fall



Be sure to give an incline of more than 30μs to rise and fall for input with varied power supply voltage (V_{CC}) and bleeder resistance.

Also, when setting input bleeder resistance, VS pin input current is affected and the detection voltage setting will differ from the set value if current on the bleeder resistor is too low.

Use input bleeder resistor R2 at 250kΩ or less.

2. Delay time setting

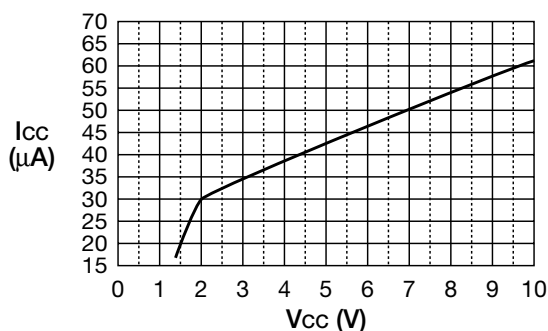
H transmission delay time can be set easily as follows from the TC pin, using the external capacitor.

$$T = Cd \times (2.33 \times 106) [s]$$

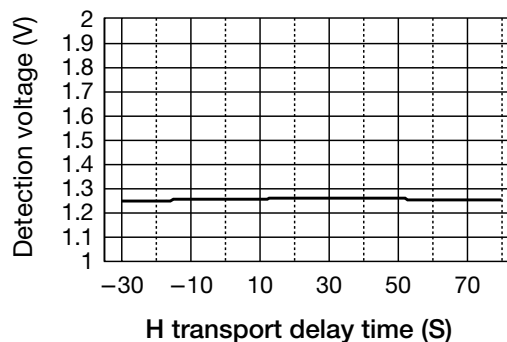
Use the external capacitor at 1μF (approx. 2.33s) or less.

Characteristics

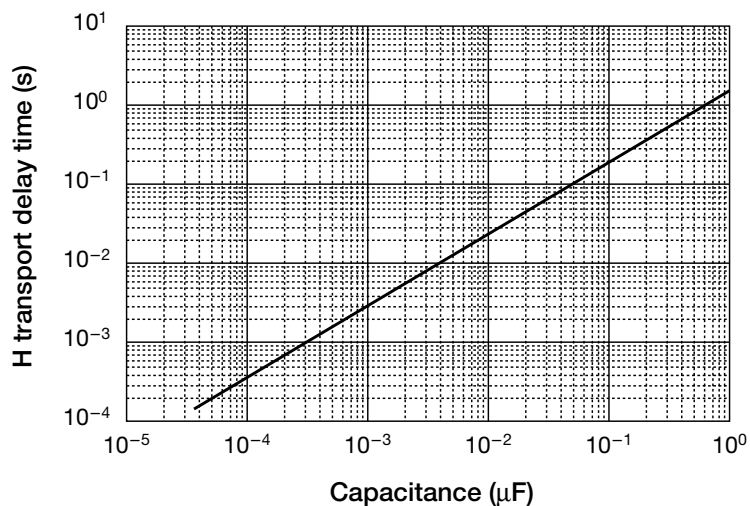
Current consumption for OFF



Detection voltage

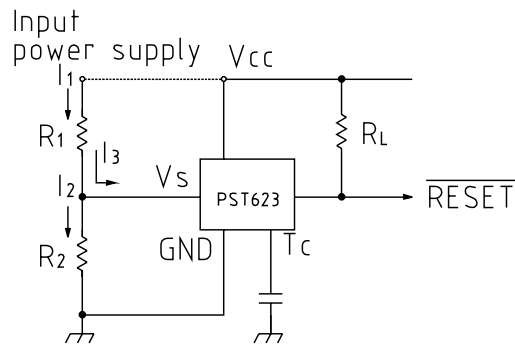


H transport delay time



Application Circuits

1. Circuit Diagram



2. Detection Voltage Setting

$$V_s \approx 1.25 \cdot \frac{R_1 + R_2}{R_2}$$

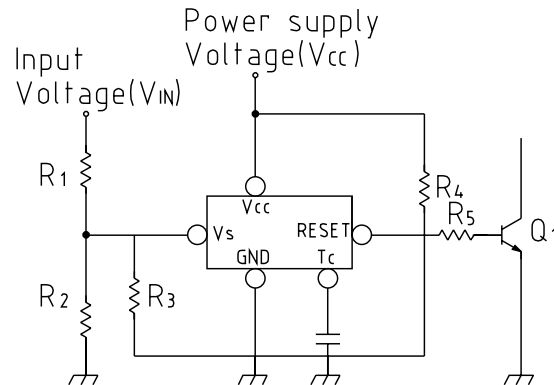
*** Note**

The value of I2 should be sufficient to ignore I3.

Make I2 > 5μA.

R2 < 250kΩ

3. How to widen hysteresis



Voltage VIN1 so that Q1 ON goes OFF.

$$V_{IN1} = \frac{(R_1 + R_2)}{R_2 \cdot (R_3 + R_4 // R_5)} [1.25 (V) \cdot (R_3 + R_1 // R_2 + R_4 // R_5) - \frac{R_1 // R_2}{R_4 + R_5} (R_4 \cdot V_{BE} + R_5 \cdot V_{CC})]$$

Voltage VIN2 so that Q1 OFF goes ON.

$$V_{IN2} = \frac{(R_1 + R_2)}{R_2 \cdot R_3} [1.275 (V) \cdot (R_1 // R_2 + R_3) - V_{OL} \cdot (R_1 // R_2)]$$

VOL: Low level output voltage

VBE: Base-emitter voltage of transistor Q1

$$R_1 // R_2 \equiv \frac{R_1 \cdot R_2}{R_1 + R_2}$$

$$R_4 // R_5 \equiv \frac{R_4 \cdot R_5}{R_4 + R_5}$$