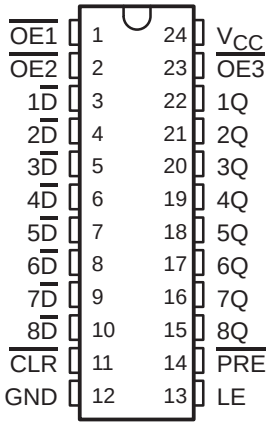
- **BiCMOS Process With CMOS Inputs and TTL Outputs Substantially Reduces Standby Current**
- **Input Has 50-Ω Pullup Resister**
- **Bus-Structured Pinout**
- **Functionally Equivalent to SN74ALS29846 and AMD Am29846**
- **Provides Extra Data Width Necessary For Wider Address/Data Paths or Buses With Parity**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Packaged in Standard Plastic 300-mil DIP (NT)**

NT PACKAGE
(TOP VIEW)



description

The SN74BCT29846 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the SN74BCT29846 are transparent D-type latches. The SN74BCT29846 has inverting data ($\overline{D}$) inputs. Since clear ($\overline{CLR}$) and preset ($\overline{PRE}$) are independent of the clock, taking the $\overline{CLR}$ input low will cause the eight Q outputs to go low. Taking the $\overline{PRE}$ input low will cause the eight Q outputs to go high. When both $\overline{PRE}$ and $\overline{CLR}$ are taken low, the outputs will follow the preset condition.

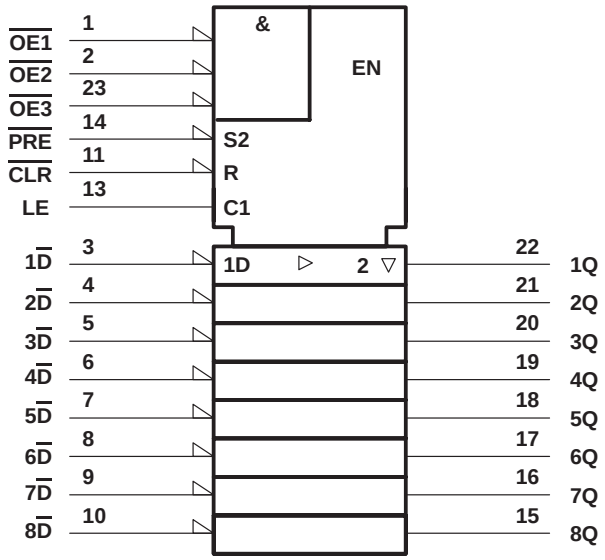
The buffered output-enable ($\overline{OE1}$, $\overline{OE2}$, and $\overline{OE3}$) inputs can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output enables do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74BCT29846 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

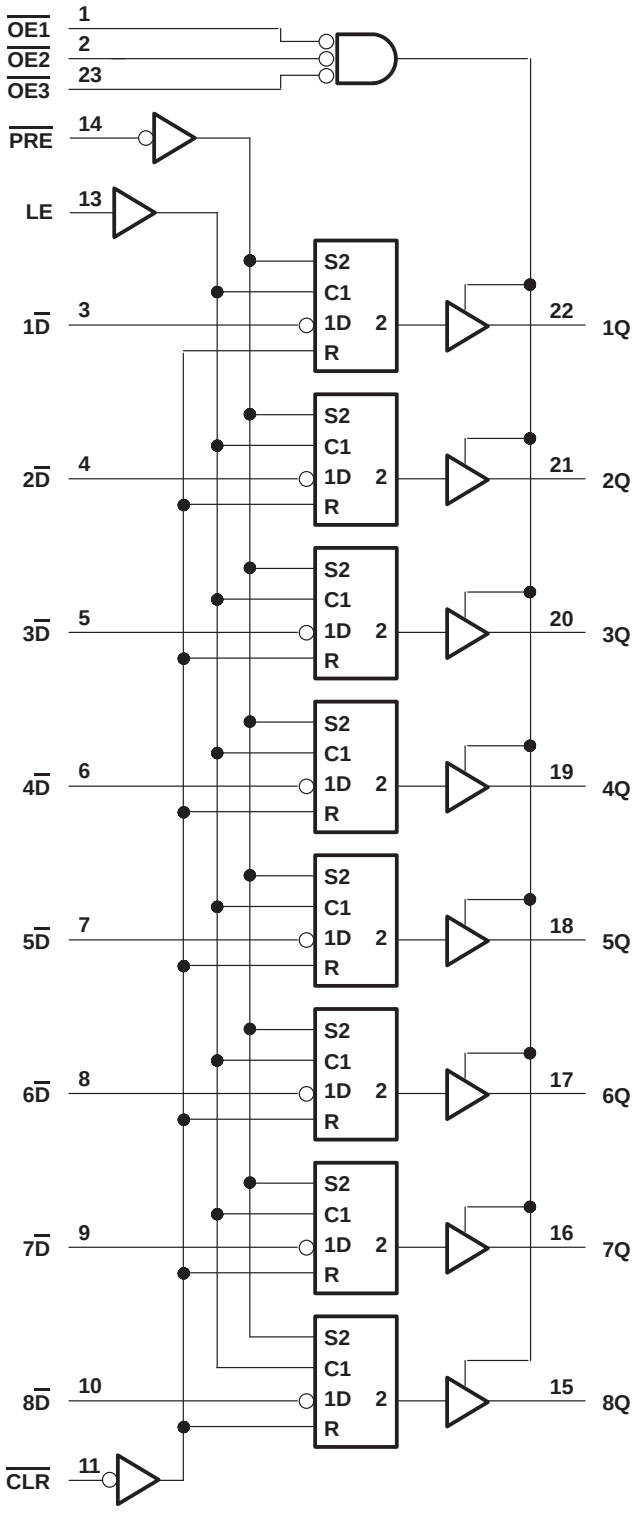
INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OE1}$	$\overline{OE2}$	$\overline{OE3}$	LE	$\overline{D}$	Q
L	X	L	L	L	X	X	H
H	L	L	L	L	X	X	L
H	H	L	L	L	H	L	H
H	H	L	L	L	H	H	L
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage range . . . . . –0.5 V to 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . – 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		48	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = –15 mA	2.4	3.2		V
		I_{OH} = –24 mA	2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	mA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			–20	mA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V	–10		–75	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	–75		–275	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		3	7	mA
		Outputs low		24	35	
		Outputs disabled		3	7	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
t_w	Pulse duration	$\overline{PRE}$ low	7		ns
		$\overline{CLR}$ low	5		
		LE high	4		
t_{su}	Setup time before LE↓	Data	1.5		ns
		$\overline{PRE}$ or $\overline{CLR}$, inactive state	2		
t_h	Hold time, data after LE↓		3.5		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	$\overline{D}$	Any Q	1.5	5.7	8	1.5	9	ns
t_{PHL}			1.5	4.5	7	1.5	8	
t_{PLH}	LE	Any Q	1.5	6	8	1.5	10	ns
t_{PHL}			1.5	6	8	1.5	10	
t_{PLH}	$\overline{PRE}$	Any Q	1.5	6	11	1.5	12	ns
t_{PHL}			1.5	6	11	1.5	12	
t_{PLH}	$\overline{CLR}$	Any Q	1.5	6	11	1.5	12	ns
t_{PHL}			1.5	6	11	1.5	12	
t_{PZH}	$\overline{OE}$	Any Q	2	10	13	2	15	ns
t_{PZL}			2	10	13	2	15	
t_{PHZ}	$\overline{OE}$	Any Q	2	6	8	2	10	ns
t_{PLZ}			2	6	8	2	10	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

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