

SN54ABT16540, SN74ABT16540 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS208A – FEBRUARY 1991 – REVISED JULY 1994

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

These 16-bit buffers and bus drivers provide a high-performance bus interface for wide data paths.

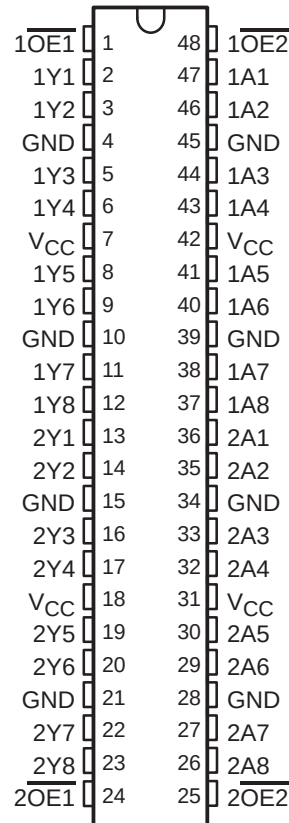
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16540 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16540 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16540 is characterized for operation from -40°C to 85°C .

SN54ABT16540 . . . WD PACKAGE
SN74ABT16540 . . . DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

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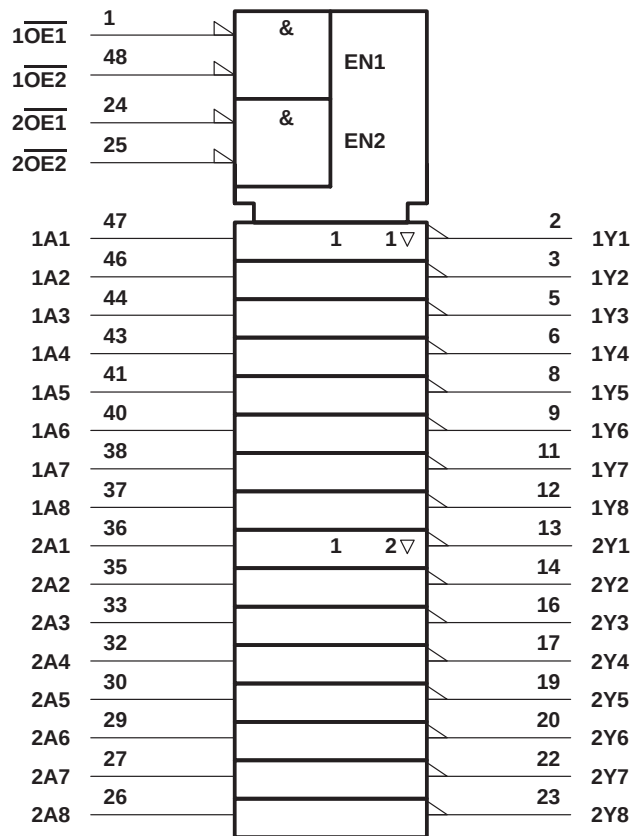
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 **TEXAS
INSTRUMENTS**

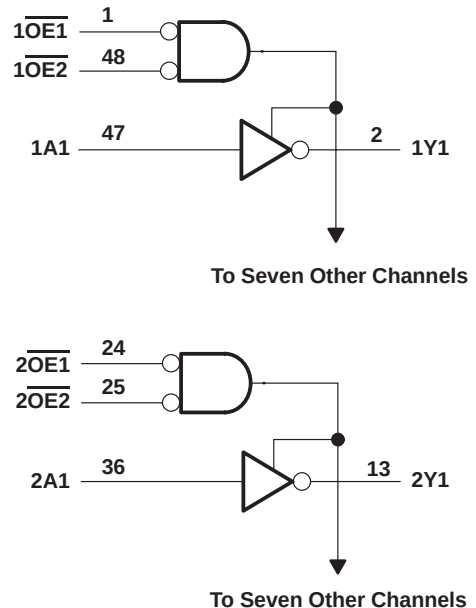
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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16540	96 mA
SN74ABT16540	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DGG package	0.85 W
DL package	1.2 W
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

			SN54ABT16540		SN74ABT16540		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage			0.8		0.8	V
V _I	Input voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current			–24		–32	mA
I _{OL}	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = 25°C			SN54ABT16540		SN74ABT16540		UNIT
			MIN	TYP [†]	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA			–1.2		–1.2		–1.2	V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = –3 mA	2.5			2.5		2.5		V
		V _{CC} = 5 V, I _{OH} = –3 mA	3			3		3		
		V _{CC} = 4.5 V			2	2				
					2*			2		
V _{OL}		V _{CC} = 4.5 V			0.55	0.55				V
					0.55*			0.55		
I _I		V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1	±1		±1		μA
I _{OZH}		V _{CC} = 5.5 V, V _O = 2.7 V			50	50		50		μA
I _{OZL}		V _{CC} = 5.5 V, V _O = 0.5 V			–50	–50		–50		μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100			±100		μA
I _{CEX}	Outputs high	V _{CC} = 5.5 V, V _O = 5.5 V			50	50		50		μA
I _O [‡]		V _{CC} = 5.5 V, V _O = 2.5 V	–50	–100	–180	–50	–180	–50	–180	mA
I _{CC}	Outputs high	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND			2	2		2		mA
	Outputs low				32	32		32		
	Outputs disabled				2	2		2		
ΔI _{CC} [§]	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1	1		1		mA
					0.05	0.05		0.05		
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5	1.5		1.5		
C _i		V _I = 2.5 V or 0.5 V			7					pF
C _O		V _O = 2.5 V or 0.5 V			7					pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

[†] All typical values are at V_{CC} = 5 V.

[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

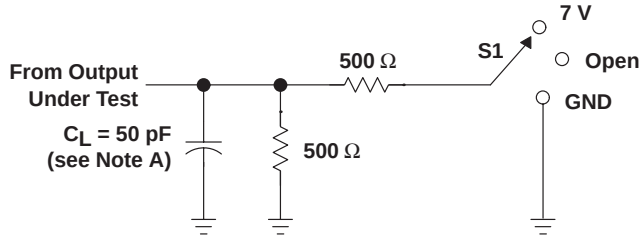
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT16540		SN74ABT16540		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.3	3.3	1	4.2	1	4.1	ns
t_{PHL}			1.1	2.5	4.1	1.1	4.4	1.1	4.3	
t_{PZH}	$\overline{OE}$	Y	1.1	3.1	4.2	1.1	5.2	1.1	5.1	ns
t_{PZL}			1.6	3.7	4.8	1.6	6	1.6	5.9	
t_{PHZ}	$\overline{OE}$	Y	1.6	3.4	4.6	1.6	5.4	1.6	5.3	ns
t_{PLZ}			1.4	2.9	4.1	1.4	4.7	1.4	4.4	

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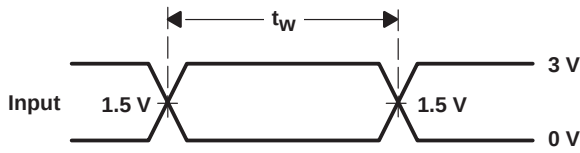
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PARAMETER MEASUREMENT INFORMATION

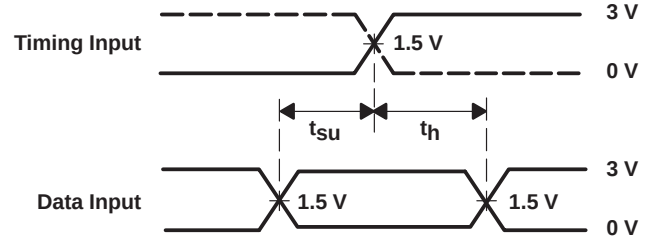


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

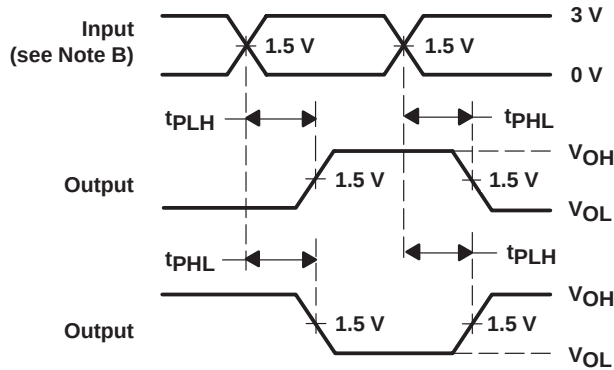
LOAD CIRCUIT FOR OUTPUTS



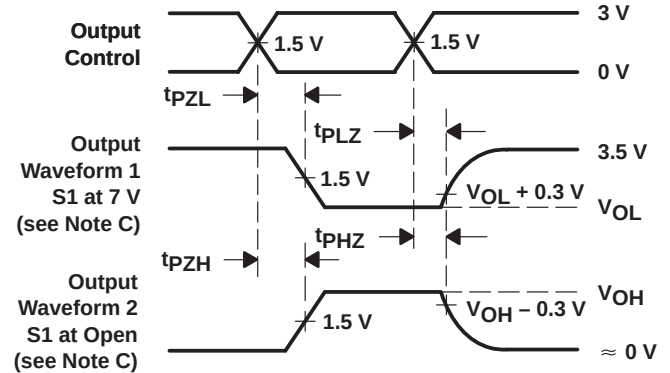
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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