SN74SSTL32867
26-BIT REGISTERED BUFFER WITH SSTL_2 INPUTS AND LVCMOS OUTPUTS

SCES240A – APRIL 1999 – REVISED MAY 1999

- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports SSTL_2 Signal Data Inputs**
- **Supports LVTTL Switching Levels on the $\overline{\text{RESET}}$ Pin**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Differential CLK Signal**
- **Advanced ULTTL Output Circuitry Eliminates Switching Noise in Unterminated Line**
- **Packaged in Plastic Fine-Pitch Ball-Grid-Array Package**

description

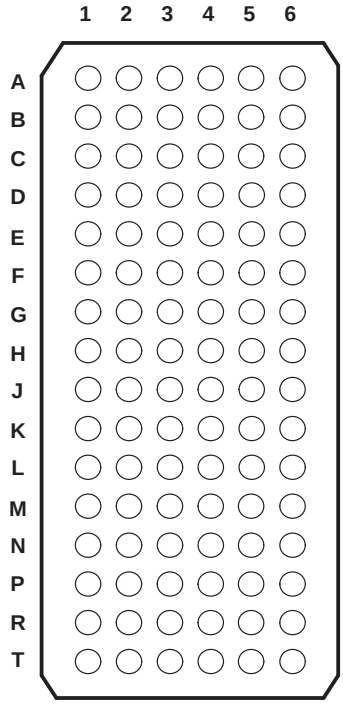
This 26-bit registered buffer is designed for 2.3-V to 2.7-V V_{CC} operation and SSTL_2 input and unterminated LVCMOS-output applications.

Data flow from A to Y is controlled by differential clock (CLK, $\overline{\text{CLK}}$) inputs and the LVTTL reset ($\overline{\text{RESET}}$) input. Data are triggered on the positive edge of the positive clock (CLK). The negative clock ($\overline{\text{CLK}}$) is used to maintain noise margins. When $\overline{\text{RESET}}$ is low, all registers are reset, and all outputs are low.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

The SN74SSTL32867 is characterized for operation from 0°C to 70°C.

GKE PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	A1	V_{CC}	GND	V_{DDQ}	Y1	Y2
B	A3	A2	V_{REF}	GND	Y3	Y4
C	A5	A4	NC	GND	Y5	Y6
D	A7	A6	GND	V_{DDQ}	Y7	Y8
E	A9	A8	V_{CC}	GND	Y9	V_{DDQ}
F	A11	A10	GND	V_{DDQ}	Y10	GND
G	A13	A12	V_{CC}	V_{DDQ}	Y12	Y11
H	A15	A14	GND	GND	GND	Y13
J	CLK	NC	GND	GND	GND	Y14
K	$\overline{\text{CLK}}$	$\overline{\text{RESET}}$	V_{CC}	V_{DDQ}	Y15	Y16
L	A16	A17	GND	V_{DDQ}	Y17	GND
M	A18	A19	V_{CC}	GND	Y18	V_{DDQ}
N	A20	A21	GND	V_{DDQ}	Y20	Y19
P	A22	A23	NC	GND	Y22	Y21
R	A24	A25	NC	GND	Y24	Y23
T	A26	V_{CC}	GND	V_{DDQ}	Y26	Y25

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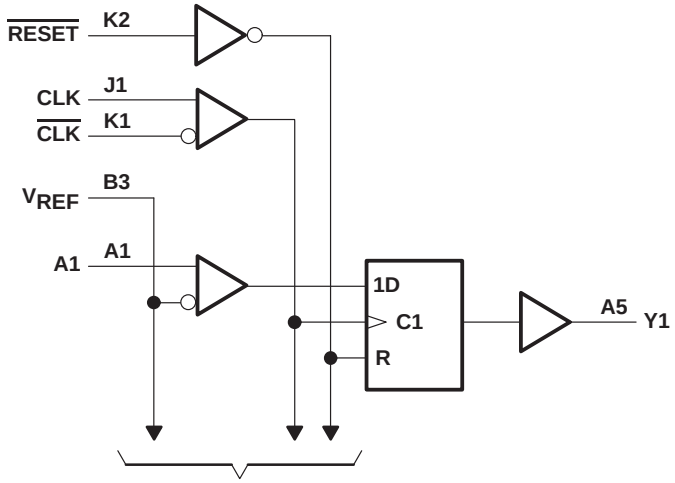
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	A	Y
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Y_0
L	X	X	X	L

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} or V_{DDQ} . . . . . –0.5 V to 3.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Continuous output current, I_O (V_O = 0 to V_{DDQ}) . . . . . ±50 mA
Continuous current through each V_{CC}, V_{DDQ}, or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 40°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. Current flows only when the output is in the high state and $V_O > V_{DDQ}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		V_{DDQ}		2.7	V
V_{DDQ}	Output supply voltage		2.3		2.7	V
V_{REF}	Reference voltage ($V_{REF} = V_{DDQ}/2$)		1.15	1.25	1.35	V
V_{TT}	Termination voltage		V_{REF}–40mV	V_{REF}	V_{REF}+40mV	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	AC high-level input voltage	Data input	V_{REF}+350mV			V
V_{IL}	AC low-level input voltage	Data input			V_{REF}–350mV	V
V_{IH}	DC high-level input voltage	Data input	V_{REF}+180mV			V
V_{IL}	DC low-level input voltage	Data input			V_{REF}–180mV	V
V_{IH}	High-level input voltage	$\overline{\text{RESET}}$	1.7			V
V_{IL}	Low-level input voltage	$\overline{\text{RESET}}$			0.7	V
V_{ICR}	Common-mode input voltage range	CLK, $\overline{\text{CLK}}$	0.97		1.53	V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, $\overline{\text{CLK}}$	360			mV
I_{OH}	High-level output current				–8	mA
I_{OL}	Low-level output current				8	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{IK}		I_I = –18 mA		2.3 V			–1.2	V
V_{OH}		I_{OH} = –100 μA		2.3 V to 2.7 V	V_{CC}–0.2			V
		I_{OH} = –4 mA		2.3 V	2			
		I_{OH} = –8 mA			1.7			
V_{OL}		I_{OL} = 100 μA		2.3 V to 2.7 V			0.2	V
		I_{OL} = 4 mA		2.3 V			0.3	
		I_{OL} = 8 mA					0.6	
I_I	Data inputs	V_I = 1.7 V or 0.8V	V_{REF} = 1.15 V or 1.35 V	2.7 V			±5	μA
	$\overline{\text{RESET}}$ input	V_I = 2.7 V or 0					±5	
	CLK, $\overline{\text{CLK}}$	V_I = 1.7 V or 0.8V	V_{REF} = 1.15 V or 1.35 V	2.7 V			±5	
		V_I = 2.7 V or 0					±5	
	V_{REF}	V_{REF} = 1.15 V or 1.35 V		2.7 V			±5	
I_{CC}		V_I = 1.7 V or 0.8 V	I_O = 0	2.7 V				mA
		V_I = 2.7 V or 0						
C_i	$\overline{\text{RESET}}$ input	V_I = 1.7 V or 0.8 V		2.5 V†				pF
	Data inputs							
C_o	Outputs	V_O = 1.7 V or 0.8 V		2.5 V†				pF

† All typical values are at V_{CC} = 2.5 V, T_A = 25°C.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V_{CC} = 2.5 V ± 0.2 V			UNIT
			MIN	TYP	MAX	
f_{clock}	Clock frequency		200			MHz
t_w	Pulse duration, CLK, $\overline{CLK}$ high or low		1.6	0.8		ns
t_{su}	Setup time	Data before CLK↑, $\overline{CLK}$↓	1.1	0.5		ns
		$\overline{RESET}$ high before CLK↑, $\overline{CLK}$↓	1.1	0.5		
t_h	Hold time, data after CLK↑, $\overline{CLK}$↓		0.5	0		ns

switching characteristics over recommended operating free-air temperature range, $V_{REF} = V_{DDQ}/2$ and C_L = 10 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V			UNIT
			MIN	TYP	MAX	
f_{max}					200	MHz
t_{pd}	CLK and $\overline{CLK}$	Y		1.9	2.8	ns
t_{PHL}	$\overline{RESET}$	Y		2.2	3.2	ns

switching characteristics over recommended operating free-air temperature range, $V_{REF} = V_{DDQ}/2$ and C_L = 30 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V			UNIT
			MIN	TYP	MAX	
f_{max}					200	MHz
t_{pd}	CLK and $\overline{CLK}$	Y		2.6	3.8	ns
t_{PHL}	$\overline{RESET}$	Y		2.9	4.4	ns

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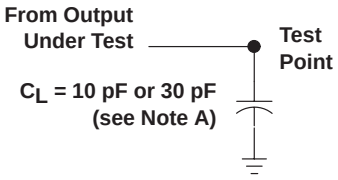
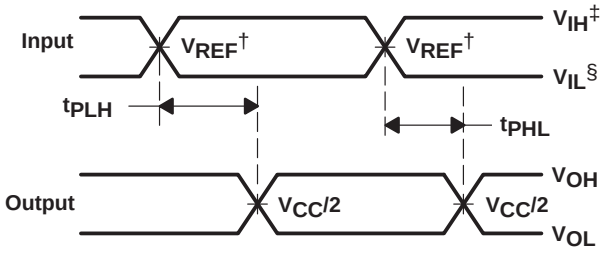
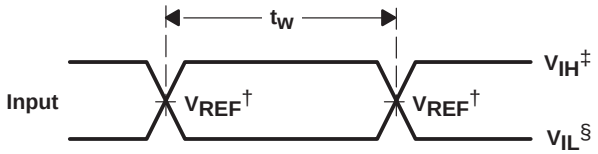
PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V



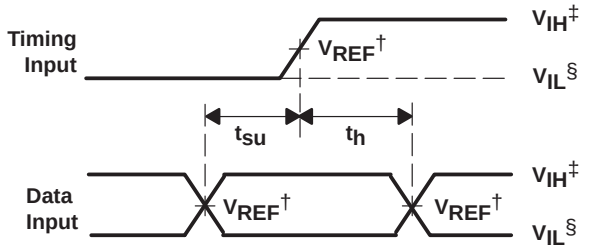
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

† $V_{REF} = V_{DDQ}/2$
‡ $V_{IH} = V_{REF}$+350mV (ac voltage levels) for SSTL inputs. $V_{IH} = V_{CC}$ for LVTTL inputs.
§ $V_{IL} = V_{REF}$–350mV (ac voltage levels) for SSTL inputs. V_{IL} = GND for LVTTL inputs.

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1.25 ns/V, t_f ≤ 1.25 ns/V.
C. The outputs are measured one at a time with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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