

SN54LS352, SN74LS352

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SDLS162 – OCTOBER 1976 – REVISED MARCH 1988

- Inverting Versions of SN54LS153, SN74LS153
- Schottky-Diode-Clamped Transistors
- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Typical Average Propagation Delay Times:
 - Data Input to Output . . . 15 ns
 - Strobe Input to Output . . . 19 ns
 - Select Input to Output . . . 22 ns
- Fully Compatible with most TTL Circuits
- Low Power Dissipation . . . 31 mW Typical (Enabled)

description

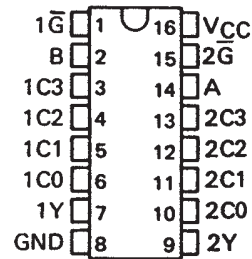
Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

FUNCTION TABLE

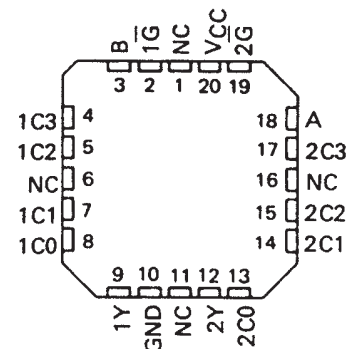
SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	\bar{G}	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.
 H = high level, L = low level, X = irrelevant

SN54LS352 . . . J OR W PACKAGE
 SN74LS352 . . . D OR N PACKAGE
 (TOP VIEW)

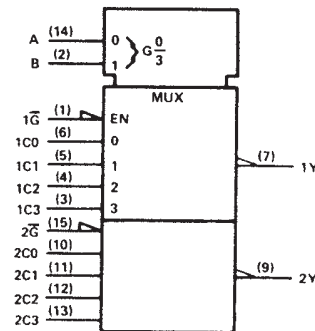


SN54LS352 . . . FK PACKAGE
 (TOP VIEW)



NC – No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS352	–55°C to 125°C
SN74LS352	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



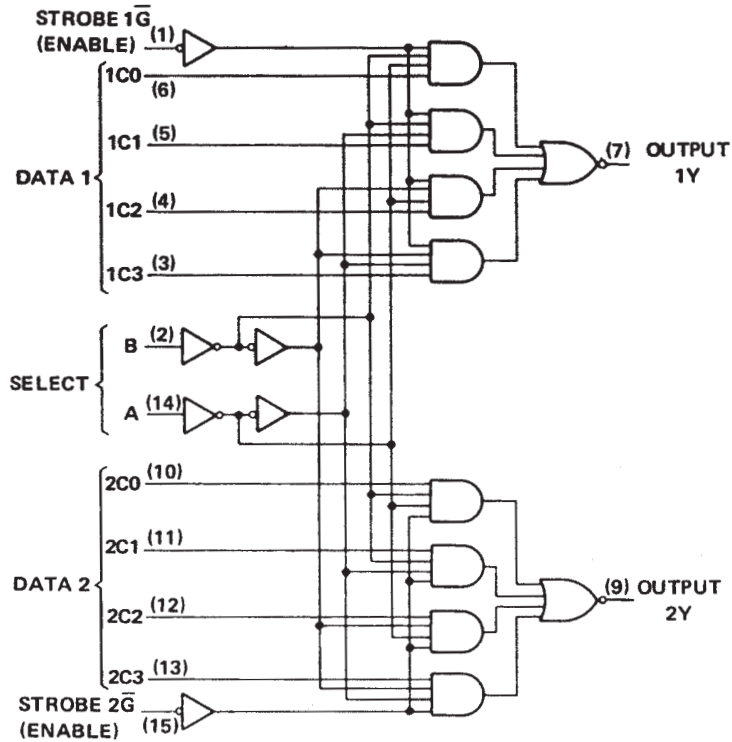
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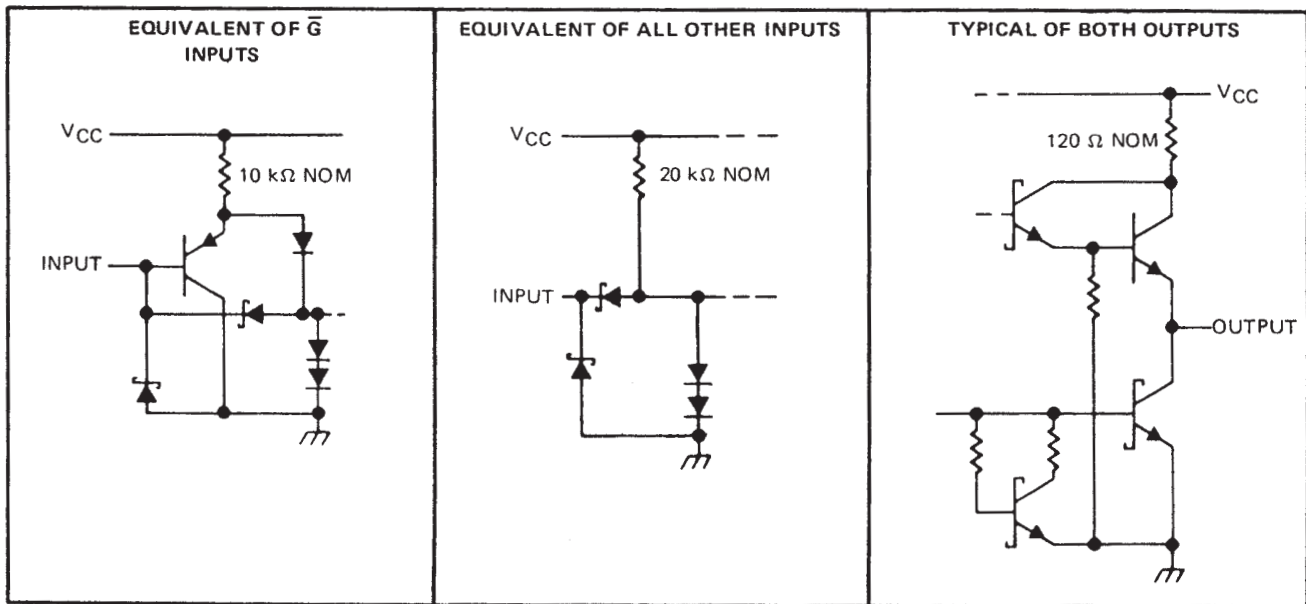
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logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs



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recommended operating conditions

	SN54LS352			SN74LS352			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage	0.7			0.8			V
I_{OH} High-level output current	-0.4			-0.4			mA
I_{OL} Low-level output current	4			8			mA
T_A Operating free-air temperature	-55 125			0 70			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS352		SN74LS352		UNIT
		MIN	TYP‡	MAX	MIN	
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$	-1.5		-1.5		V
V_{OH}	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = \text{MAX}$, $I_{OH} = -0.4 \text{ mA}$	2.5	3.4	2.7	3.4	V
V_{OL}	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = \text{MAX}$	0.25 0.4		0.25 0.4		V
	$I_{OL} = 4 \text{ mA}$			0.35 0.5		
	$I_{OL} = 8 \text{ mA}$					
I_I	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$	0.1		0.1		mA
I_{IH}	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$	20		20		µA
I_{IL}	\bar{G}	-0.2		-0.2		mA
	All other	-0.4		-0.4		
$I_{OS}§$	$V_{CC} = \text{MAX}$	-20	-100	-20	-100	mA
I_{CCL}	$V_{CC} = \text{MAX}$, See Note 2	6.2	10	6.2	10	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CCL} is measured with the outputs open and all inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	$R_L = 2 \text{ k}\Omega$, See Note 3	$C_L = 15 \text{ pF}$,	13	20	20	ns
t_{PHL}	Data	Y			17	26	26	ns
t_{PLH}	A or B	Y			19	29	29	ns
t_{PHL}	A or B	Y			25	38	38	ns
t_{PLH}	\bar{G}	Y			16	24	24	ns
t_{PHL}	\bar{G}	Y			21	32	32	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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