TEXAS INSTRUMENTS

TLV1504/1508/1544/2544/2548, TLC1514/1518/2554/2558 10-Bit and 12-Bit ADC EVM

User's Guide

May 1999 – Revised May 2000

Mixed-Signal Products

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and use of the TLV1504/1508/1544/2544/2548/TLC1514/1518/2554/2558 EVM for the TLV1504, TLV1508, TLC1514, TLC1518, TLC2554, TLC2558, TLV1544, TLV2544, and TLV2548 10-bit/12-bit analog-to-digital converter (ADC).

The TLV1504/1508/1544/2544/2548/TLC1514/1518/2554/2558 EVM will be referred to as the ADC EVM throughout this manual.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1 Overview
- ❏ Chapter 2 Physical Description
- ❏ Chapter 3 Circuit Description
- ❏ Chapter 4 Operation

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This book may contain cautions and warnings.

This is an example of a caution statement.

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Data Sheets:	Literature Number
❑ TLC1514/18	SLAS252
❑ TLC2554/58	SLAS220A
❑ TLV1504/08	SLAS251
❑ TLV1544CPW	SLAS139C
❑ TLV2544/8CPW	SLAS198A
❑ TLC5618ACD	SLAS156E
❑ SN74AHC244IDW	SCLS226H
❑ TPS7101QD	SLVS092F
❑ TLE2142AID	SLOS183A
❑ TLV2772ACD	SLOS209D
❑ SN74AHC1G08DBVR	SCLS314G
❑ SN74AHC04D/ SN74HC04D	SCLS231J/ SCLS078B
❑ SN74HC164D	SCLS115B
❑ SN74HC74D/ SN74AHC74D	SCLS094B/ SCLS255G
❑ TL7726CD	SLAS078C
❑ SN74AHC08D/ SN74HC08D	SCLS236E/ SCLS081B
❑ SN74AHCIG32	SCLS317H
❑ SN74HC374DW/ SN74AHC374DW	SCLS141C/ SCLS240G

Application Reports:

- ❑ *Interfacing the TLVX544/TLVX548 Analog-to-Digital Converter to the TMS320C50 and TMS320C203 DSPs*, literature number SLAA025 and SLAA028A.

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Chapter 1

Overview

This chapter gives a general overview of the ADC EVM and describes some of the factors that must be considered in using the module.

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1.1 Purpose

The ADC EVM provides a platform for evaluating the TLV1504, TLV1508, TLV1544, TLC1514, and TLC1518 10-bit analog-to-digital converter (ADC), TLC2554, TLC2558, TLV2544 and TLV2548, 12-Bit ADCs under various signal, reference, and supply conditions.

1.2 EVM Basic Function

The TLV1504/1544/2544 and TLC1514/2554 has four analog inputs, while the TLV1508/2548 and TLC1518/2558 has eight analog inputs. All inputs are available for external signal inputs through SMA connectors. To perform testing without having to apply an external signal via the SMA inputs, an onboard DC signal, REF_CH3/7 is available via jumper W3 to channel A3/A7.

The internal dc input signal consists of a voltage reference with a potentiometer for adjusting the dc input voltage. The reference voltage is either 5 V or 3.3 V and is selected by operating switch, SW1.

If the ADC EVM board is built to evaluate the TLC series of ADC devices, then SW1 is not installed on the EVM board. Instead, switch1 (SW1), is replaced with a jumper wire connected directly to the output 5 V since the TLC devices only operate in a single 5-V supply.

Signal conditioning operational amplifiers are used to interface the input signal to channel A0 and A1. For use in the evaluation of the ADC, the EVM incorporates a 12-bit TLC5618A digital-to-analog converter (DAC), an SN74HC74, and a 74HC374, used during loopback testing, to format the serial word to the DAC.

An SN74AHC244 buffers the digital I/O signals to the output header and test connector. The SN74HC164 is used to convert the serial data stream from the ADC to parallel data for displaying on a logic analyser.

1.3 Power Requirements

The EVM dc supply voltage range is ±7 V to ±10 V. The power supply and externally-applied reference voltage should be supplied to the EVM through shielded twisted-pair wire for best performance. This type of power cabling minimizes any stray or transient pickup from the higher frequency digital circuitry.

Voltage Limits

Exceeding the ±10-volt maximum can damage EVM components. Under voltage may cause improper operation of the bipolar op amp channel A1, depending on the application. The positive supply can be lowered to 6 volts and the EVM will maintain the 5-V supply.

1.4 I/O CLK or SCLK Requirements

The TLV1544 has a maximum I/O CLK of 10 MHz at V_{CC} = 5 V and is limited to 2.8 MHz for a supply voltage of 2.7 V. The TLV2544/48 has a maximum SCLK of 20 MHz at V_{CC} = 5 V and 15 MHz at 2.7 V. Table 1–1 lists the maximum I/O CLK/SCLK frequencies for different supply ranges. This also depends on input source impedance. For example, I/O CLK speed faster than 2.39 MHz is achievable if the input source impedance is less than 1 kΩ.

Table 1–1. Maximum I/O CLK Frequency

	V_{CC}	Maximum Input Resistance (Max)	Source Impedance	I/O CLK/SCLK
TLV1544	2.7 V	5 K	1 kΩ	2.39 MHz
			100 Ω	2.81 MHz
	4.5 V	1 K	1 kΩ	7.18 MHz
			100 Ω	10 MHz
TLV2544 TLV2548	2.7 V	600	≤1 kΩ	15 MHz
	4.5 V	500	≤1 kΩ	20 MHz
TLV1504	2.7 V	600	≤1 kΩ	15 MHz
TLV1508	5.5 V	500	≤1 kΩ	20 MHz
TLC1514 TLC1518	5.5 V	500	≤1 kΩ	20 MHz
TLC2554 TLC2558	5.5 V	500	≤1 kΩ	20 MHz

1.5 I/O Interface Connector Provisions

The connector interface is versatile, allowing different connection arrangements depending on the user selected interface. A 20-position dual inline header connector, J11, is used to interface the TMS320C5x DSP and microcontroller devices to the EVM. It is hard-wired to the input/output signals of the ADC through the SN74AHC244. J12 is a dual row, 24-position header, used to interface both TMS320C2xx/TMS320C54x DSPs to the EVM. The headers are readily available 100-mil center connectors. A ribbon cable with the corresponding female plug, mates to the header the appropriate DSP or microcontroller EVM. Figure 3–1 shows the signal arrangement for J11 and J12.

Ideally, J12 should be arranged so that the clock lines have a ground line on either side in the ribbon cable to minimize crosstalk. If possible, every other conductor in the ribbon cable should be grounded. However, keep in mind that, many DSP/microcontroller EVM boards restrict the interface connector size, and signals going to the output connector are not routed for minimum crosstalk.

An isometric drawing showing the ADC EVM connected to the TMS320C54x DSKplus EVM can be found in literature number SLAU030 (*TMS320C54x DSKplus Adapter Kit*).

1.6 ADC EVM Operational Procedure

Some signal setup or software is required for the ADC EVM. The ADC data sheet (refer to section 4.3 for specific ADC data sheet information) provides the timing requirements and the application report (literature number SLAA025A and SLAA028A) supplies an example of software using the TMS320C50 DSP and TMS320C203 DSP. Once the input requirements are completed, the operating procedures for the ADC EVM are as follows.

- Connect ±7 to ±10 V and ground to the 10 V, –10 V, and GND terminals of J10. These terminals are marked on the top side of the EVM silkscreen. TP3–TP8 is shorted to establish zero volts as the operating point. When TP1 and TP2 are shorted, the output at both the TLV2772 and TLE2142 operational amplifiers, reads 2.5 V for an AVDD of 5 V.

  SW1 can select 5-V V_{CC} or 3.3-V V_{CC}, making it convenient to evaluate both 3.3-V and 5-V systems. Note that when evaluating the TLC version the switch, SW1, is not installed as discussed in section 1.2.

- For most DSP operation, JP1 is open, and for most microprocessor operation, JP1 is shorted. The device $\overline{\text{INV CLK}}$/ $\overline{\text{PWDN}}$ input is controlled by this jumper. The state of the inverted signal is used to control the I/O CLK edge used for sampling the input data. Applying a logic low signal to the $\overline{\text{PWDN}}$ causes both analog and digital circuits to go into the power-down mode.

- The analog input that is connected to the ADC is determined by software, and any input can be selected for testing. The TLV1544/2544 and TLC1514/2554 four channels are configured as follows:

  Analog Input

  A0 Interface to a buffer driven by a single supply input scaling operational amplifier
  Unbuffered external input is via W2 positions 1–2

  A1 Interface to a buffer driven by a dual supply, ±10 V used for input scaling
  Unbuffered external input is provided via W1 positions 1–2

  A2 Uses unbuffered external input

  A3 Uses unbuffered external input or dc REF_CH3/7

  A4–A7 Uses unbuffered external input

  Normally, through the software, or loopback testing via the TLC5618A, the ADC full-scale, mid-scale, and zero-scale values are first checked. Channel A3/A7 can be selected and checked with the dc signal REF_CH3/7 using jumper W3.

- An external reference voltage, derived from a MAX6250 precision voltage regulator, is used to provide the REF+ and REF– reference voltage for the ADC as well as the 2.5 V reference for the TLC5618A – when operating the ADC with ΔVref = 5 V.

  Designation Reference Voltage

  Onboard absolute reference = 5 V, at Vin = 7 V to 10 V

  When SW1 is changed the onboard absolute reference is automatically changed to the proper value for the DVdd/AVdd selected.

REF+, REF– and 2.5REF are automatically changed when SW1 is changed. However, some slight adjustment of individual potentiometer may be necessary.

- The I/O signals can be monitored at J7, J11 and J12.
- The additional analog inputs can be used for application of external signals that might be used to digitize signals for further processing. In short, select the desired analog input channel: implement the data loopback tests by shunting positions 2–3 of W5 and W7 positions 3–4 with a jumper connection. With the TMS320C5x DSP, positions 1–2 of W9 are shorted with a jumper connector or shunt. Positions 2–3 of W9 are shorted when using either the TMS320C203 or TMS320C54x DSP.

1.7 Functional Testing Without a DSP or Microcontroller EVM

With the aid of an arbitrary waveform generator, generating FS, $\overline{CS}$, and SCLK for the device is straight-forward. Configure the device by applying a DATA IN input waveform of A000h at the falling edge of FS while $\overline{CS}$ is LOW (refer to the device datasheet for more information). Then select channel A0 by grounding the DATA IN input, and activate both $\overline{CS}$ and FS high-to-low. Apply the ac analog or dc input to SMA connector J3 and set W2 appropriately. Simply shunt W5 positions 2–3 and W7 positions 3–4 to connect the ADC output to the TLC5618A DAC channel B (J14). Observe a replica of the input signal connected to A0.

Chapter 2

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

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2.1 PCB Layout

The EVM is constructed on a 4-layer, 12 cm (4.7-inch) × 10 cm (3.9-inch), 0.157 cm (0.062-inch) thick PCB using FR-4 material. Figures 2–1 through 2–5 show the individual layers.

Figure 2–1. PCB Layout

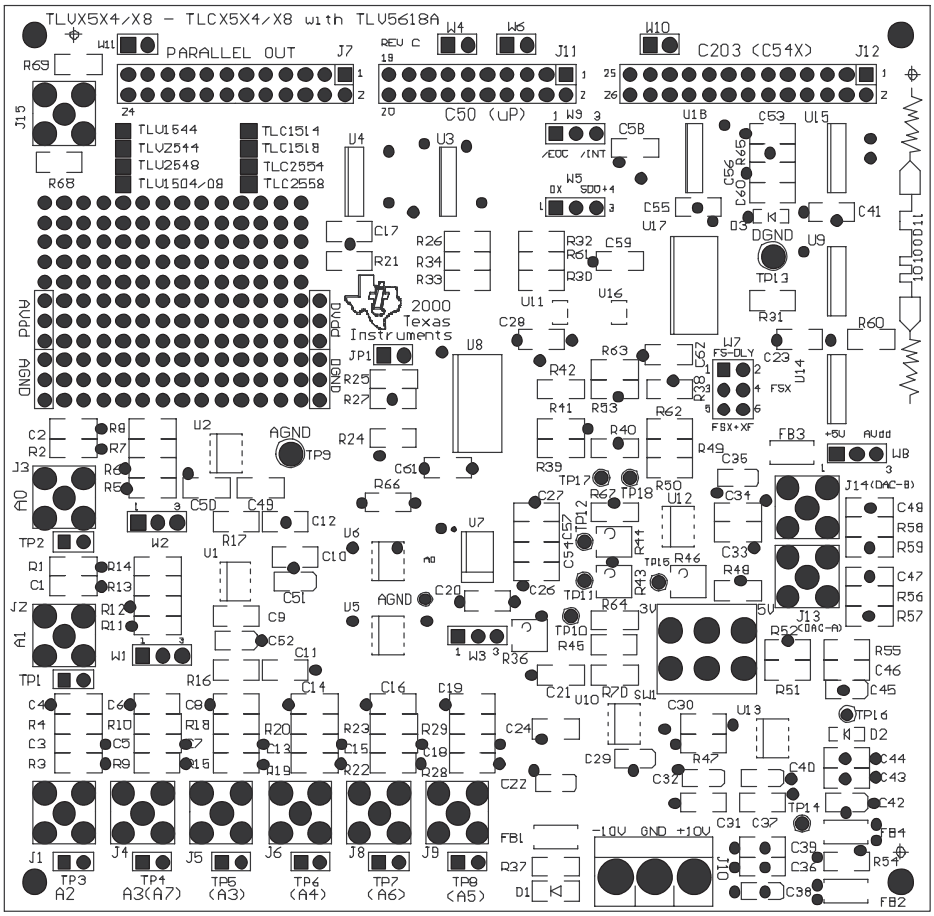


Figure 2–2. PCB Layout

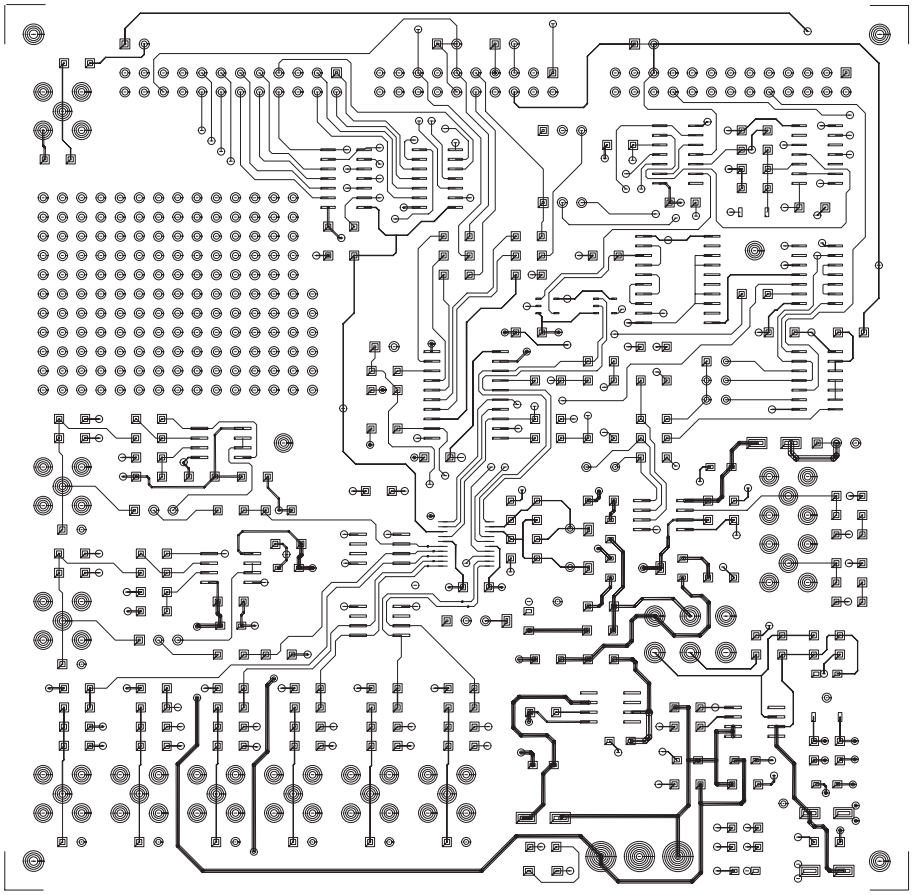


Figure 2–3. PCB Layout

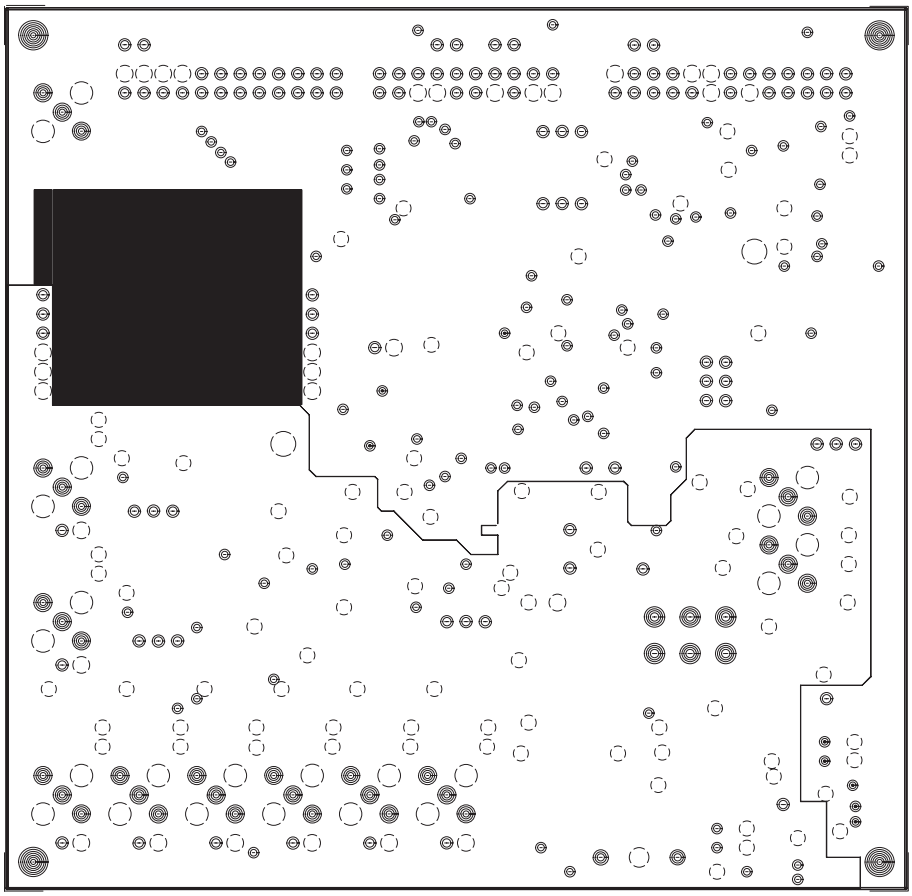


Figure 2–4. PCB Layout

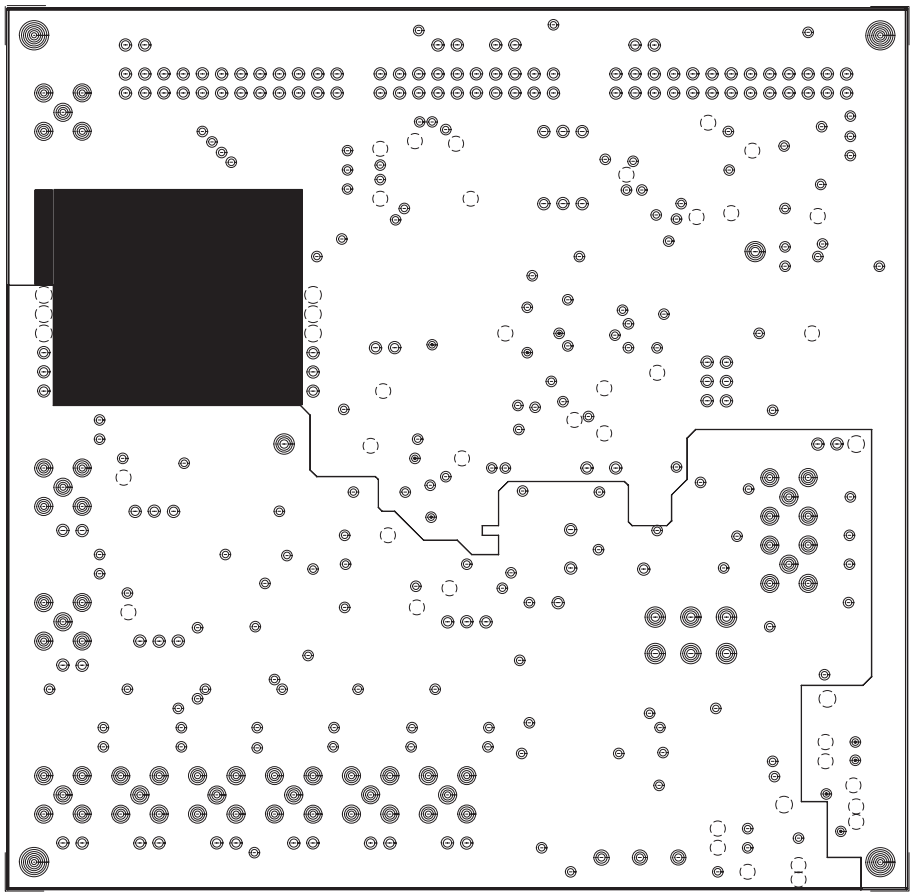
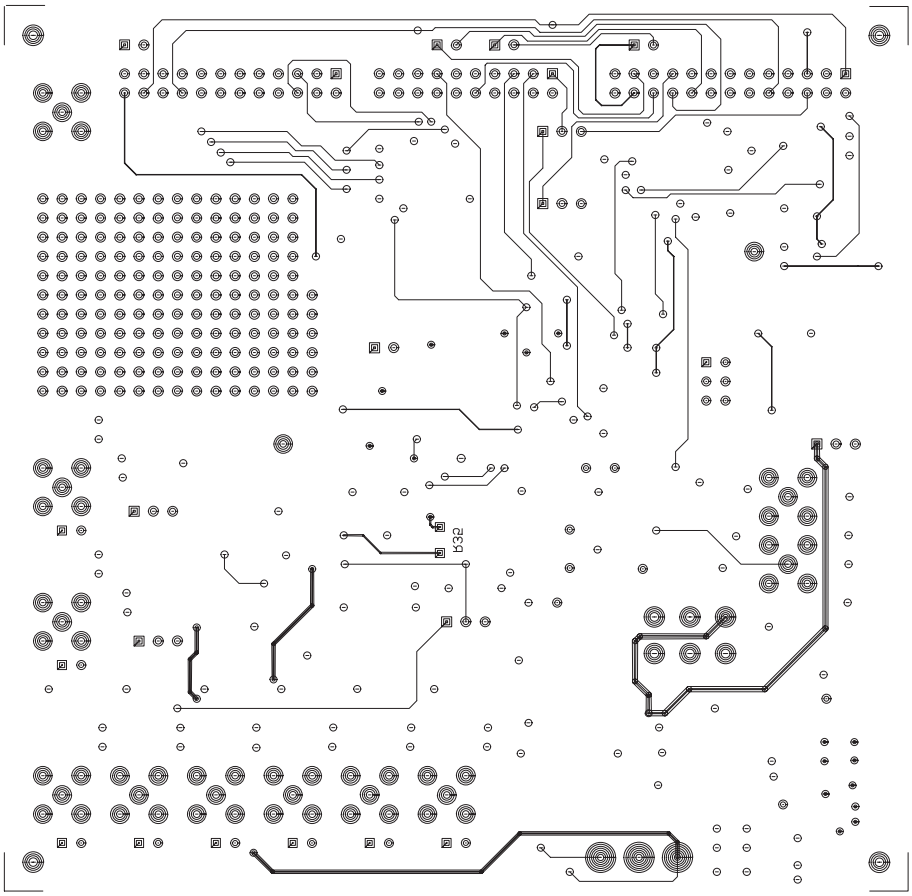


Figure 2–5. PCB Layout



2.2 Parts List

Table 2–1 lists the parts used in constructing the EVM.

Table 2–1. Parts List

Qty	Qty	Reference Description	Description	Manufacturer	Part Number
4–Ain	8–Ain				
1	1	NA	REV A PCB fabrication	Texas Instruments	TLVX544/X548
3	3	C39 C44 C50	Ceramic, X7R, 50 V, 10%	Kemet	C1206C103K5RAC
25	25	C10 C17 C20 C23 C26 C27 C28 C30 C31 C33 C34 C36 C37 C41 C43 C46 C49 C53 C54 C55 C56 C60 C61 C62 C9	Ceramic, X7R, 50 V, 10%	Kemet	C1206C104K5RAC
2	2	C47 C48	Ceramic, X7R, 50 V, 10%	Kemet	C1206C101K5GAC
1	1	C24	Ceramic, X7R, 16 V, 10%	Kemet	C1206C105K4RAC
2	2	C22 C29	2.2 µF, 16 V tantalum. capacitor	Kemet	T491A225K016AS
4		C11 C12 C4 C6	Ceramic, X7R, 50 V, 10%	Kemet	C1206C682K5RAC
	8	C11 C12 C4 C6 C8 C14 C16 C19	Ceramic, X7R, 50 V, 10%	Kemet	C1206C682K5RAC
8	8	C32 C35 C38 C40 C42 C45 C51 C52	4.7 µF, 16 V, tantalum capacitor	Kemet	T491A475K016AS
2	2	C57 C21	Ceramic, Y5V, 10 V, 20%	AVX	1206ZG106ZAT2A
1	1	D1	Green 1206 size chip LED	Chicago Miniature	CMD15-21VGC
1	1	D2	40 V, 400 mW Schottky	Diodes Inc.	LLSD101C
1	1	D3	Hi-speed switching diode	Edmar Electronics	DL4148
4	4	FB1 FB2 FB3 FB4	Surface-mount ferrite bead	Fair Rite	2744044447
2	2	JP1 W6	Single row 2-pin header	Samtec	TWS-102-07-L-S
1	1	W7	6-Pin dual row header	Samtec	TWS-103-07-L-D
1	1	J12	26-Pin dual row header	Samtec	TWS-113-07-L-D
	10	J1 J2 J3 J4 J5 J6 J8 J9 J13 J14	PCB mount SMA jack	Johnson Components	142-0701-206
6		J1 J2 J3 J4 J13 J14	PCB mount SMA jack	Johnson Components	142-0701-206
1	1	J10	3-terminal screw connector	Lumberg	KRMZ3
1	1	J11	20-pin dual row header	Samtec	TWS-110-07-L-D
4	4	R54 R57 R59 R66	1206 chip resistor., 5%	Bourns	CR1206-FX-000

Table 2–1. Component List (Continued)

Qty	Qty	Reference Description	Description	Manufacturer	Part Number
4		R10 R16 R17 R4	1206 chip resistor., 5%	Bourns	CR1206-FX-22R0
	8	R10 R16 R17 R4 R18 R20 R23 R29	1206 chip resistor., 5%	Bourns	CR1206-FX-22R0
15	15	R14 R24 R27 R38 R40 R41 R53 R6 R64 R65 R37 R56 R58 R63 R70	1206 chip resistor., 1%	Bourns	CR1206–FX–1002
4	4	R36 R43 R44 R46	4mm, 5T, SM potentiometer	Bourns	3214J–1–103–W
1	1	R48	9.09 kΩ	Bourns	CR1206–FX–9092
1	1	R7	1206 chip resistor., 1%	Bourns	CR1206–FX–1213
1	1	R5	1206 chip resistor., 1%	Bourns	CR1206–FX–1502
1	1	R52	1206 chip resistor., 1%	Bourns	CR1206–FX–1693
1	1	R45	1206 chip resistor., 5%	Bourns	CR1206–FX–1001
2	2	R12 R47	1206 chip resistor., 1%	Bourns	CR1206–FX–2002
1	1	R25	1206 chip resistor., 5%	Bourns	CR1206–FX–2001
1	1	R70	1206 chip resistor., 1%	Bourns	CR1206–FX–2261
2	2	R11 R8	1206 chip resistor., 1%	Bourns	CR1206–FX–3012
10	10	R31 R33 R49 R60 R61 R62 R69 R21 W4 W10, See Note 2	1206 chip resistor., 5%	Bourns	CR1206–FX–33R0
7	7	R26 R30 R32 R34 R39 R42 R50	1206 chip resistor., 5%	Bourns	CR1206–FX–3300
1	1	R51	1206 chip resistor., 1%	Bourns	CR1206–FX–5903
1	1	R13	1206 chip resistor., 1%	Bourns	CR1206–FX–4022
1	1	R67	1206 chip resistor., 1%	Bourns	CR1206–FX–4751
1	1	R55	1206 chip resistor., 1%	Bourns	CR1206–FX–6043
1	1	SW1†	PCB mount DPDT slide switch	C&K	1201M2S3CQE2
8	8	TP10 TP11 TP12 TP18 TP14 TP15 TP16 TP17	Test point – single .025” pin	Samtec	TWS–101–07–L–S
2	2	TP9 TP13	Turret type test pin	Cambion	180–7337–02–05
1	1	U11	Micro AND gate	Texas Instruments	SN74AHC1G08DBVR
1	1	U16	Micro OR gate	Texas Instruments	SN74AHC1G32DBVR
1	1	U10	Maxim precision voltage regulator	Maxim	MAX6250BCSA/ MAX6250BESA
2	2	U9 U15	Hex inverter	Texas Instruments	SN74AHCT04D
1	1	U17	Octal D type FF	Texas Instruments	SN74HC374DW
1	1	U18	Dual D–type FF	Texas Instruments	SN74HC74D
1	1	U14	Quad AND gate	Texas Instruments	SN74AHCT08D

† Not installed on ADC EVM board built to evaluate TLC series ADCs.

Table 2–1. Component List (Continued)

Qty	Qty	Reference Description	Description	Manufacturer	Part Number
1		U6	Clamp circuit	Texas Instruments	TL7726CD/TL7726ID/ TL7726QD
	2	U5 U6	Clamp circuit	Texas Instruments	TL7726CD/TL7726ID/ TL7726QD
1	1	U12	Programmable dual 12-bit DAC	Texas Instruments	TLC5618ACD/ TLC5618AID
1	1	U1	Dual op amp in 8-pin SOP package	Texas Instruments	TLE2142CD/ TLE2142ACD/ TLE2142ID/ TLE2142AID
1	1	U2	Dual op amp in 8-pin SOP package	Texas Instruments	TLV2772AID/ TLV2772AMD
1		U7	Serial ADC	Texas Instruments	TLC1514CPW
	1	U7	Serial ADC	Texas Instruments	TLC1518CPW
1		U7	Serial ADC	Texas Instruments	TLC2554CPW
	1	U7	Serial ADC	Texas Instruments	TLC2558CPW
1		U7	Serial ADC	Texas Instruments	TLV1504CPW
	1	U7	Serial ADC	Texas Instruments	TLV1508CPW
1		U7	Serial ADC	Texas Instruments	TLV1544CPW
1		U7	Serial ADC	Texas Instruments	TLV2544CPW
	1	U7	Serial ADC	Texas Instruments	TLV2548CPW
1	1	U13	Low dropout voltage regulator	Texas Instruments	TPS7101QD
1	1	U8	Octal buffer and line driver	Texas Instruments	SN74AHCT244DW
6	6	W1 W2 W3 W5 W8 W9	0.025” square, 3-pin header, 0.1” centers	Samtec	TWS-103-07-L-S
	Customer Installed Options				
4		C1 C2 C3 C5	Ceramic, X7R, 50 V, 10%	Kemet	C1206C101K5GAC
	8	C1 C2 C3 C5 C7 C13 C15 C18	Ceramic, X7R, 50 V, 10%	Kemet	C1206C101K5GAC
2	2	C58 C59	Ceramic, X7R, 50 V, 10%		
1	1	W11	Single row 2-pin header	Samtec	TWS-102-07-L-S
1	1	J7	24-pin dual row header	Samtec	TWS-112-07-L-D
1	1	J5	PCB mount SMA jack	Johnson Components	142-0701-206
1	1	R35	1206 chip resistor., 5%	Bourns	CR1206-FX-000
5		R1 R2 R3 R9 R68	1206 chip resistor., 1%	Bourns	CR1206-FX-49R9
	9	R1 R2 R3 R9 R15 R19 R22 R28 R68	1206 chip resistor., 1%	Bourns	CR1206-FX-49R9
4		TP1 TP2 TP3 TP4	Test point – dual .025” pin	Samtec	TWS-102-07-L-S

Table 2–1. Component List (Continued)

Qty	Qty	Reference Description	Description	Manufacturer	Part Number
	8	TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8	Test point – dual .025” pin	Samtec	TWS-102-07-L-S
2	2	U3 U4	8-Bit parallel out shift register	Texas Instruments	SN74HC164D

Note: MFG/PN for reference only. Substitutions permissable on all parts except integrated circuits.

Chapter 3

Circuit Description

This chapter contains the EVM schematic diagram and discusses the various functions on the EVM.

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3.1 Schematic Diagram

Figure 3–1 shows the schematic diagram for the EVM. The following paragraphs describe the EVM circuits.

Figure 3–1. EVM Schematic Diagram

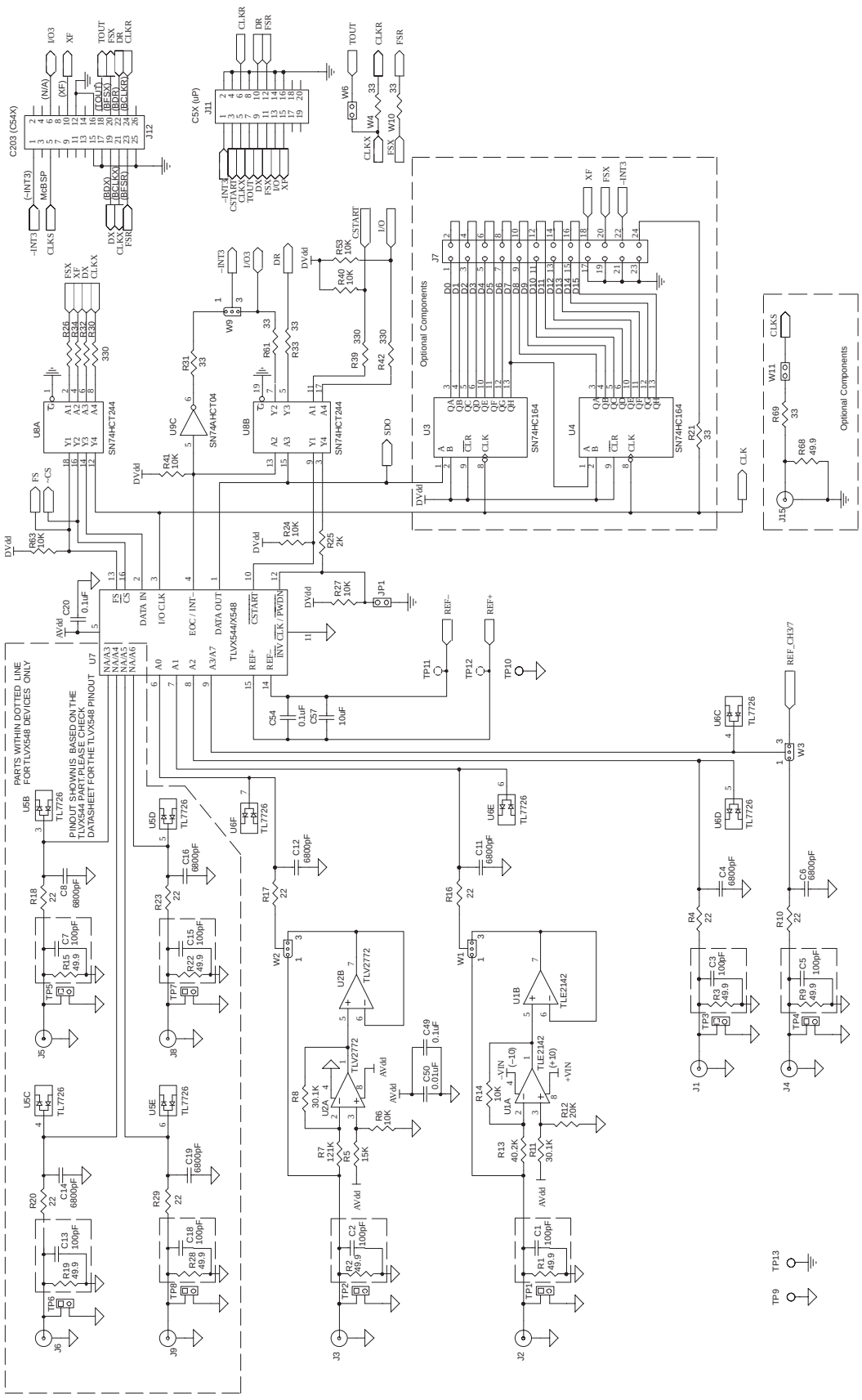
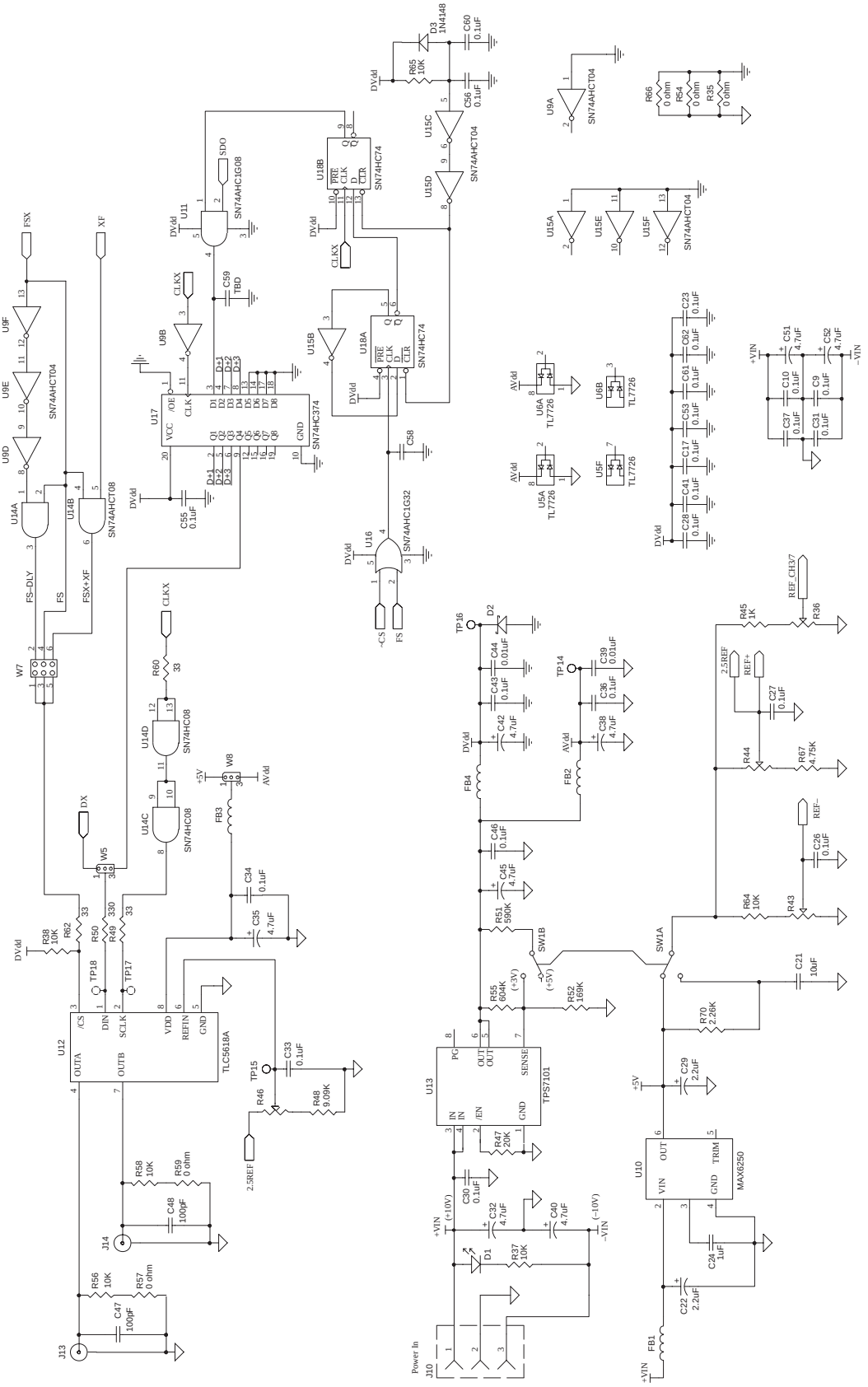


Figure 3–2. EVM Schematic Diagram



3.2 Circuit Function

The following paragraphs describe the function of individual circuits.

3.2.1 Inputs

The TLV1504/1544/2544/TLC1514/2554 has four analog inputs; A0, A1, A2, and A3. While the TLV1508/2548/TLC1518/2558 has eight input channels; A0–A7. The applied input signal connects to these inputs as follows:

- A0. One operational amplifier of a single-supply TLV2772 is used to scale the input analog signal and the dynamic range of the output is compressed to 0 V–5 V over a wide range of input levels (0 V – ±10 V and zero dc input offset). The second TLV2772 op amp is used to buffer the A0 input signal.
- A1. A TLE2142 dual-supply operational amplifier is used to scale the wide ranging(0 V– ±10 V) signal connected to the A1 input. The operational amplifier receives external input through J2.
- A2–A7. These inputs are available for user-defined inputs. The external inputs to these channels are applied through J1, J4 through J7, respectively. It is important to note that each input channel has a low-pass filter. The filter RC components can be adjusted to suit the application.

3.2.2 A0 – External Input via Input Scaling and Voltage Follower Operational Amplifiers

It should be noted that for AV_{DD} = 5 V there is a 2.5 V dc offset voltage, produced by the node voltage of the voltage divider (R5/R6) multiplied by the amplifier gain, at the input of channel A0. The offset is used to convert the bipolar input to a single-ended input needed by the ADC. It is assumed that the analog input signal is free of dc offset. If the incoming analog signal has a dc offset, then the ADC REF– voltage is typically adjusted to the same value as the input signal dc offset voltage and REF+ is raised by the same amount. Since REF+ max is 5 V, a sinusoid input signal of ±8Vpp and 0.5 V dc offset produces full-scale from the ADC. By ac-coupling the input to J3, the dynamic range of the input increases.

3.2.3 A1 – External Input via Dual Supply Operational Amplifiers Used for Input Scaling and Buffering

The inverting input of one TLE2142 operational amplifier is connected to J2 via a 40.2K resistor, and signal from this amplifier (gain = 0.25) is buffered by a second TLE2142 op amp used to drive input A1. This arrangement minimizes the interaction between A1 and the output of the first operational amplifier. With an input power supply of ±7 V or greater, this amplifier configuration produces a linear signal from 0 V to 5 V. This signal does not approach the amplified nonlinearity limits when operating close to the supply rail voltages. Input A1 is protected from voltages below and above the ADC supply by two diodes. Also input A1 is low-pass filtered and the filter 3 dB cutoff frequency should be set to pass the desired input signal.

The amplifier noninverting input signal has a quiescent value of AVDD/2 for proper midpoint biasing for the ADC. When using the amplifier with direct

coupling and an input with dc offset, full-scale ADC output code is achieved with less input amplitude. In this instance, reduce the dynamic range of the input and adjust REF+ and REF– as necessary. When capacitor coupling is used between the source and J2, an input range of 10 V to –10 V produces 0 V to 5 V at input channel A1.

The SMA connectors, J1, J4–J9, provide unbuffered inputs to the ADC. These inputs are protected by diodes to prevent damage to the ADC from voltages in excess of the supply rail voltages. Each channel has RC components used for band limiting the input signal. The dc signal REF_CH3/7, via W3 pins 2–3, is made available at channel A3 (TLV1504/1514/2544/TLC1514/2554) and channel A7 (TLV1508/2548/TLC1518/2558). In this configuration the ADC operation can be checked without having to apply an external input to the EVM.

When using the unbuffered inputs, the driving source impedance must be less than 1 kΩ for proper slew rate of the input signal. The source must provide enough current into 50 pF to arrive at a final voltage value within the device-specified sampling time. Also, if the source noise is not below the 10-bit or 12-bit level, this noise could cause jitter in the output least significant bit (LSB).

3.2.4 Power

A balanced voltage input of ±10 V maximum (±7 V minimum) and ground should be supplied to the EVM through connector J10 with the positive supply voltage applied to J10-1, the negative supply to J10-3, and ground to J10-2. The operational amplifier, U1, uses the bipolar power supplies. The remainder of the EVM uses regulated 5 V from the positive supply through the TPS7101 low dropout regulator. Switch SW1 can switch the output voltage of the regulator from nominally 5-V to 3.3-V operation. The regulator output voltage is divided into the digital supply (DVdd) and analog supply (AVdd) through ferrite beads and individual filter capacitors. The 5-V or 3.3-V output powers the following devices: U2, U3, U4, U5, U6, U7, U8, U9, U11, U12, U14, U15, U16, U17, and U18.

The ±7 V to ±10 V is applied to the TLE2142 while only the positive supply voltage is applied to the TPS7101 low-dropout regulator. The TPS7101 regulates for a 5-V or 3.3-V V_{CC} such that ADC evaluation can be done at either V_{CC} through switch SW1. SW1 changes the ADC/TLC5618A DAC voltage reference to accommodate the change in V_{CC}; SW1 also changes V_{CC} to the SN74AHC244. The microinverter can be used to accommodate inversion for software interrupt processing.

3.2.5 Voltage Reference Generation

A nominal 5 V reference is supplied by the MAX6250 precision reference. When switch SW1 is in the 5 V supply position the REF+ can be adjusted from 1.62 V – 5 V and REF– from 0 V – 2.50 V, and with 3.30 V V_{CC} supply selected REF+ ranges from 0.97 V – 3 V and REF– ranges from 0 V – 1.50 V. The voltage differential between REF+ and REF– should always be equal to, or greater than, 2.5 V for proper operation within the TLV1544, TLV2544, TLV2548, TLV1504, TLV1508, TLC1514, TLC2554, TLC1518, and TLC2558 specified limits.

Ratiometric measurements are the signals that vary with the supply voltage. If an input signal voltage is used that varies proportionately with the supply

voltage, such as the potentiometer input to A3/A7 (REF_CH3/7), the signal is a ratio of the absolute value of the supply. Also it should be remarked that the input conversion result is independent of supply voltage variations.

The reference voltage for the TLC5618A, 12-bit DAC is generated from the same source as the ADC, therefore, both devices will track together once the voltages are set.

3.2.6 Test and Interfacing Connectors

Test connector J7 provides a convenient point for measuring the ADC device signal with a logic analyser. The device test points as listed in Table 3–1.

Table 3–1. Test Connector J7

J7 Pin	U3 and U4	Function
1	D0	DATA
2	D1	DATA
3	D2	DATA
4	D3	DATA
5	D4	DATA
6	D5	DATA
7	D6	DATA
8	D7	DATA
9	D8	DATA
10	D9	DATA
11	D10	DATA
12	D11	DATA
13	D12	DATA
14	D13	DATA
15	D14	DATA
16	D15	DATA
17		GND
18		XF
19		GND
20		FSX
21		GND
22		$\overline{\text{INT3}}$
23		GND
24		CLKX(I/OCLK)

U3 and U4 are not part of the ADC EVM and must be added. J12 is a 26-way, 100-mil spacing, male 2-row header that interfaces the TMS320C203 DSP EVM board from Wyle Electronics or the TMS320C54X DSKplus EVM. In order to minimize crosstalk introduced in the ribbon cable by the CLKOUT signal, the pin carrying the CLKOUT should be disconnected at Wyle's TMS320C203 DSP EVM board. J11 is used to interface the TMS320C50 DSP EVM from Texas Instruments.

3.2.7 Jumper Arrangement

The EVM evaluation can begin with the following shorting plug arrangement.

Device	Jumper Configuration
TLV1544	W1 pins 2–3 shorted
TLV1504	W2 pins 2–3 shorted
TLC1514	W3 pins 1–2 shorted
TLC1518	W5 pins 1–2 shorted (during loopback testing W5 pins 2–3 shorted)
TLV1508	W6 shorted (when using the DSP timer)
	W7 pins 3–4 shorted (W7 pins 5–6 shorted for real-time DSP captured data to the DAC)
	W8 pins 1–2 shorted
	W9 pins 1–2 shorted
	W11 open
	JP1 open
TLV2544	W1 pins 2–3 shorted
TLV2548	W2 pins 2–3 shorted
TLC2554	W3 pins 1–2 shorted
TLC2558	W5 pins 1–2 shorted (during loopback testing W5 pins 2–3 shorted)
	W6 shorted (when using the DSP timer)
	W7 pins 3–4 shorted (W7 pins 5–6 shorted for real-time DSP captured data to the DAC)
	W8 pins 1–2 shorted
	W9 pins 2–3 shorted
	W11 open
	JP1 open

3.2.8 Breadboard Area

The breadboard area on the EVM board is an arrangement which is most convenient for a discrete component filter stage/adding functions to the EVM. The voltages AVDD and DVDD, and GND are conveniently provided at the periphery of the breadboard area.

3.2.9 TLC5618A, 12-Bit Serial DAC

A 12-bit serial DAC is provided on the EVM for evaluating the output from the ADC. The serial digital input value applied to the converter, is converted into an analog value. The reference voltage for the DAC is set to $\frac{(\text{REF}+)-(\text{REF}-)}{2}$ since the DAC output has a X2 op amp. Monitoring the output from the DAC at J13 gives a very sensitive measure of the analog input applied to the ADC.

3.2.10 LOOPBACK Testing

LOOPBACK testing is a convenient way for checking how well the ADC is performing, without having to store the ADC output in memory. Additional circuitry is provided on the EVM for doing just that. The ADC output data is formatted, using D-type flip flops, to directly drive the TLC5618A, 12-bit serial DAC. With jumper W5 pins 2–3 shorted, the ADC output applied to the DAC is converted to an analog replica of the ADC input. The DAC output is monitored at OUTB (J14). Setting up the ADC for conversion is simple – see Section 1.7.

Chapter 4

Operation

This chapter describes the basic operation of the EVM with a host DSP or processor.

Topic **Page**

4.1 ADC Overview

The following paragraphs describe the TLV1504, TLV1508, TLV1544, TLV2544, TLV2548, TLC1514, TLC2554, and TLC2558 ADCs in general.

4.1.1 General Description

As discussed earlier in Chapter 1, this evaluation module (EVM) provides a platform for evaluating the following 10-bit ADCs: TLV1504, TLV1508, TLV1544, TLC1514, and TLC1518, and the following 12-bit ADCs: TLV2544, TLV2548, TLC2554, and TLC2558.

These are CMOS devices where the TLV version operates from a wide range of voltage ranging from 2.7 V to 5.5 V supply voltage while the TLC version is fixed 5-V supply. The converter uses an n-bit (n = 10-bit or 12-bit resolution), switched-capacitor successive approximation (SAR) ADC and a 2-bit resistor string. The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1 of SLAS139C). In the first phase of the conversion process, the analog input is sampled by closing the SC switch and all ST switches simultaneously. This action charges all the capacitors to the input voltage. In the following phase of the conversion process switches are manipulated allowing the threshold detector to begin identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. This process is repeated until all n-bits are counted.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.

4.1.2 Timing Diagrams

Refer to each specific data sheet for the system signal timing diagrams which are listed below as follows:

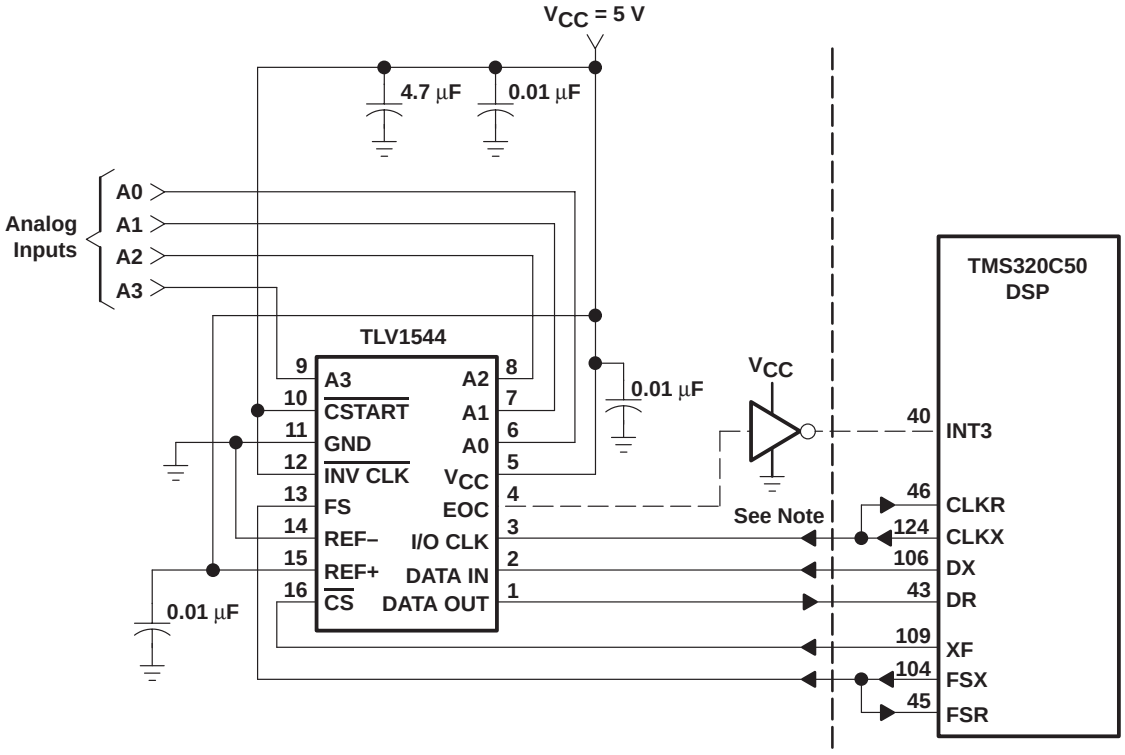
- Figures 16 through 19 of the device datasheet (SLAS139C) for TLV1544
- Figures 2 through 14 of the device datasheet (SLAS198A) for TLV2544/2548)
- Figures 2 through 14 of the device datasheet (SLAS251) for TLV1504/1508.
- Figures 2 through 14 of the device datasheet (SLAS252) for TLC1514/1518)
- Figures 2 through 14 of the device datasheet (SLAS220A) for TLC2554/2558

The timing diagrams show the four basic I/O signal sets required for microprocessor and DSP timing.

4.2 TLV1544/2544/2548 Hardware Interfacing to the TMS320 DSP

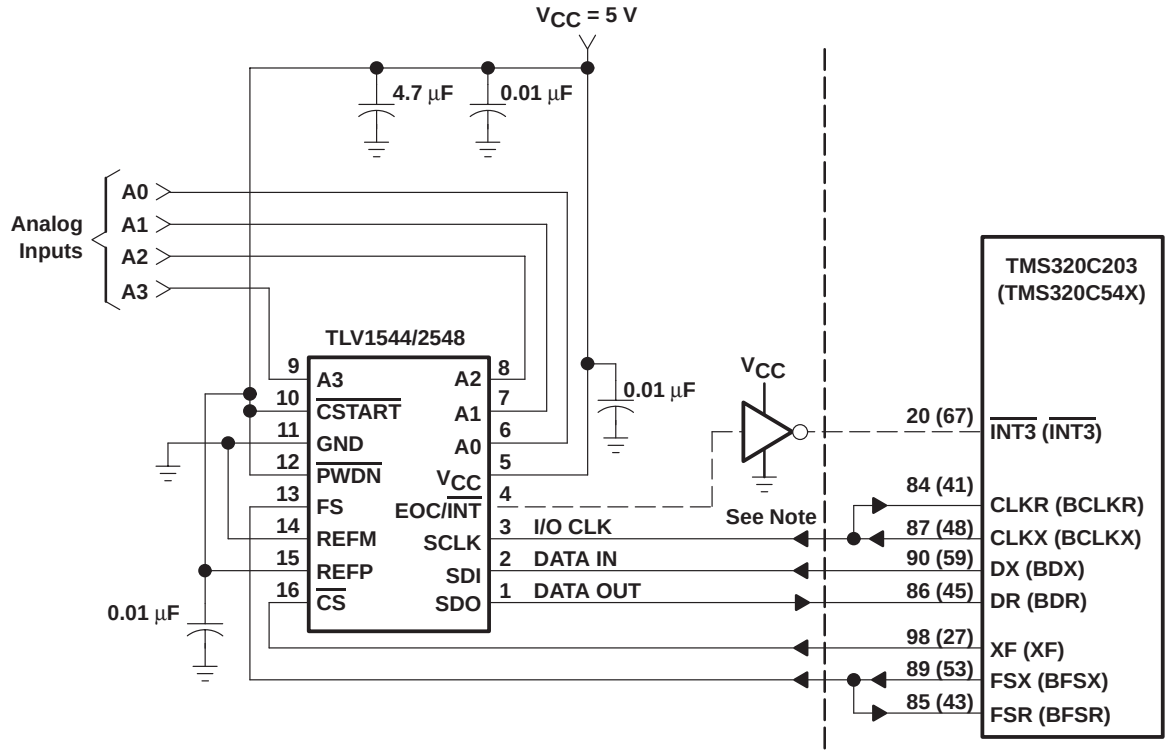
Figures 4–1 and 4–2 are the schematic diagram showing the hardware connections between the TLV1544 to the TMS320C50 and the TLV25448 and the TMS320C203/54X DSP respectively. Refer to Figure 4–1 to interface TLC1514/8 and TLV1504/8 to the TMS320C DSP and Figure 4–2 to interface TLC2554/8 to the TMS320C DSP.

Figure 4–1. Schematic Diagram



NOTE: Software programs using interrupt processing may need the inverter and the connection shown in dotted lines. In programs using wait states, EOC is not required.

Figure 4–2. Schematic Diagram



NOTE: Software programs using interrupt processing may need the inverter and the connection shown in dotted lines. In programs using wait states, EOC is not required.

4.3 Data Sheet Information

Further information for a specific device can be obtained through their data-sheet by accessing the TI website at htt://www.ti.com/. A list of the device data-sheet and their respective literature number are as follows:

- ❑ TLV1504/8CPW Literature Number SLAS251
- ❑ TLV1544CPW Literature Number SLAS139C
- ❑ TLV2544/8CPW Literature Number SLAS198A
- ❑ TLC1514/8CPW Literature Number SLAS252
- ❑ TLC2554/8CPW Literature Number SLAS220A

The literature number can change anytime due to revisions and may cause a miss when searching the TI website. In this case the device part number can be used to narrow down the search.

To order a copy of the above literature, or any literature for each of the devices mentioned in this manual, refer to the Preface section of this manual. All related data sheets and their corresponding literature numbers are listed under the Related Documentation from Texas Instruments section.

Appendix A

Grounding Considerations

This appendix contains general information on grounding techniques for a printed-circuit board using the TLV1544/2544/2548 devices.

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A.1 Printed Circuit Board Grounding Considerations

When designing analog circuits that share a ground with digital and high current power supplies, the voltage drop along the high current paths must be considered. This voltage drop is a result of the current flowing through the greater than zero resistance of the current path, or high frequency current transients flowing through a greater than zero inductance of a current path.

If the signal ground is connected to the power supply ground at an improper location, an excessive voltage drop may occur in the signal ground and appears as part of the signal, causing an error.

The solution for low frequency analog signals is to establish a single ground point on the PC board and connect all low frequency grounds to that point. By using this method, currents flowing along any one path to ground do not produce error voltages in any other ground path.

Analyzing the current flow paths within the analog section gives an indication of which components can be lumped together to a common ground path and which should be separate. One half LSB error with a reference of 4.1 volts would be approximately 0.5 mV, so the ground trace resistance would have to be no greater than 0.5 ohms with 1 mA of ground current.

When input source signals are low current, a common ground trace may be appropriate. Higher input current sources, however, should always have a separate ground trace to the most robust ground point location, usually at the ground entrance to the PCB.

Even though the TLV1544/2544/2548 operating current is low, some high speed current transients are present, usually caused by output digital switching requiring a ground plane or wide ground return trace to the central board entry ground for these signals. All signal paths and their respective ground returns must be examined to minimize signal loop area.

The power inputs and V_{CC} lines must also be analyzed in the same manner and detail that the ground returns are.