

TPIC5601 3-PHASE BRIDGE POWER DMOS ARRAY

SLIS022B – MARCH 1994 – REVISED OCTOBER 1995

- Low $r_{DS(on)}$. . . 0.3 Ω Typ
- High-Voltage Output . . . 60 V
- Pulsed Current . . . 8 A Per Channel
- Fast Commutation Speed

description

The TPIC5601 is a monolithic power DMOS array that consists of six electrically isolated N-channel enhancement-mode DMOS transistors, three of which are configured with a common source. The TPIC5601 is offered in a 20-pin wide-body surface-mount (DW) package.

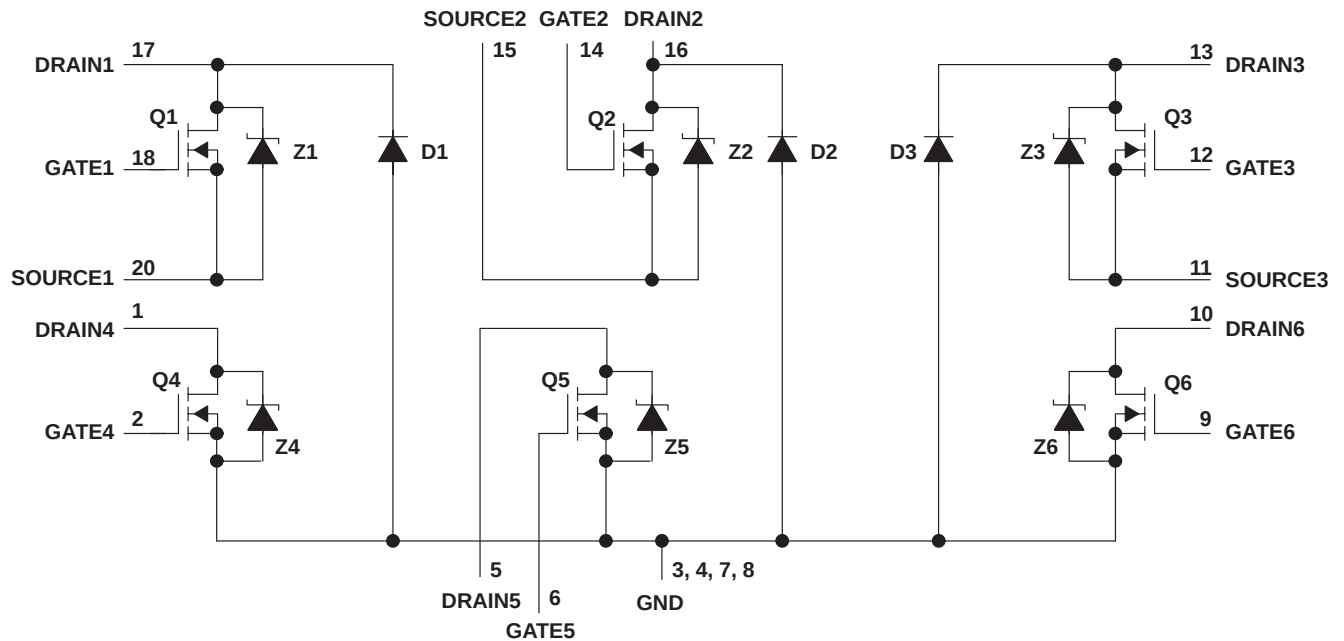
The TPIC5601 is characterized for operation over the case temperature range of -40°C to 125°C .

DW PACKAGE (TOP VIEW)

DRAIN4	1	20	SOURCE1
GATE4	2	19	NC
GND	3	18	GATE1
GND	4	17	DRAIN1
DRAIN5	5	16	DRAIN2
GATE5	6	15	SOURCE2
GND	7	14	GATE2
GND	8	13	DRAIN3
GATE6	9	12	GATE3
DRAIN6	10	11	SOURCE3

NC – No internal connection

schematic



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absolute maximum ratings over operating case temperature range (unless otherwise noted)[†]

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q2, and Q3)	100 V
Drain-to-GND voltage (Q1, Q2, and Q3)	100 V
Drain-to-GND voltage (Q4, Q5, and Q6)	60 V
Gate-to-source voltage range, V_{GS}	± 20 V
Continuous drain current, each output, $T_C = 25^\circ\text{C}$	1.7 A
Continuous source-to-drain diode current	1.7 A
Pulsed drain current, I_D , each output, $T_C = 25^\circ\text{C}$ (see Note 1 and Figure 15)	8 A
Single-pulse avalanche energy, E_A , $T_C = 25^\circ\text{C}$ (see Figures 4 and 16)	36 mJ
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	-40°C to 150°C
Operating case temperature range, T_C	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

DISSIPATION RATING TABLE

PACKAGE	$T_C \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$	$T_C = 125^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/ $^\circ\text{C}$	225 mW

electrical characteristics, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1\ \text{mA}$, $V_{DS} = V_{GS}$		1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, and D3)	Drain-to-GND current = $250\ \mu\text{A}$		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	$I_D = 1.7\ \text{A}$, See Notes 2 and 3 $V_{GS} = 10\ \text{V}$			0.51	0.6	V
V_F	Forward on-state voltage, GND-to-drain	$I_D = 1.7\ \text{A}$ (D1, D2, D3), See Notes 2 and 3			7.5		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	$I_S = 1.7\ \text{A}$, $V_{GS} = 0$ (Z1, Z2, Z3, Z4, Z5, Z6), See Notes 2 and 3			1	1.2	V
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = 48\ \text{V}$, $V_{GS} = 0$	$T_C = 25^\circ\text{C}$		0.05	1	μA
			$T_C = 125^\circ\text{C}$		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	$V_{GS} = 16\ \text{V}$, $V_{DS} = 0$			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	$V_{SG} = 16\ \text{V}$, $V_{DS} = 0$			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	$V_R = 48\ \text{V}$	$T_C = 25^\circ\text{C}$		0.05	1	μA
			$T_C = 125^\circ\text{C}$		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 10\ \text{V}$, $I_D = 1.7\ \text{A}$, See Notes 2 and 3 and Figures 6 and 7	$T_C = 25^\circ\text{C}$		0.3	0.35	Ω
			$T_C = 125^\circ\text{C}$		0.41	0.5	
g_{fs}	Forward transconductance	$V_{DS} = 15\ \text{V}$, See Notes 2 and 3 $I_D = 1\ \text{A}$		1.2	1.75		S
C_{iss}	Short-circuit input capacitance, common source	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$ $V_{GS} = 0$			190	240	pF
C_{oss}	Short-circuit output capacitance, common source				100	125	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				40	50	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum, pulse duration $\leq 5\ \text{ms}$.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{rr(SD)}$	Reverse-recovery time	$I_S = 1\ \text{A}$, $V_{GS} = 0$, $V_{DS} = 48\ \text{V}$, $di/dt = 100\ \text{A}/\mu\text{s}$, See Figure 1	(Z1, Z2, Z3),		65		ns
Q_{RR}	Total diode charge				0.12		μC
$t_{rr(SD)}$	Reverse-recovery time	$I_S = 1\ \text{A}$, $V_{GS} = 0$, $V_{DS} = 48\ \text{V}$, $di/dt = 100\ \text{A}/\mu\text{s}$, See Figure 1	(Z4, Z5, Z6),		240		ns
Q_{RR}	Total diode charge				0.9		μC

GND-to-drain diode characteristics, $T_C = 25^\circ\text{C}$ (see schematic, D1, D2, and D3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	$I_F = 1\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$, See Figure 1	$V_{DS} = 48\ \text{V}$,		260		ns
Q_{RR}	Total diode charge				2.2		μC

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resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$ Turn-on delay time	$V_{DD} = 25\text{ V}$, $R_L = 25\ \Omega$, $t_{r1} = 10\text{ ns}$, See Figure 2		32	65	ns
$t_{d(off)}$ Turn-off delay time			40	80	
t_{r2} Rise time			15	30	
t_{f2} Fall time			25	50	
Q_g Total gate charge	$V_{DS} = 48\text{ V}$, See Figure 3 $I_D = 1\text{ A}$, $V_{GS} = 10\text{ V}$		5	6	nC
Q_{GS} Threshold gate-to-source charge			0.5	0.6	
Q_{GD} Gate-to-drain charge			1.9	2.3	
$L_{(drain)}$ Internal drain inductance			5		nH
$L_{(source)}$ Internal source inductance			5		
R_g Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	All outputs with equal power, See Note 4		90		$^\circ\text{C/W}$
$R_{\theta JP}$ Junction-to-pin thermal resistance			27		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink.

PARAMETER MEASUREMENT INFORMATION

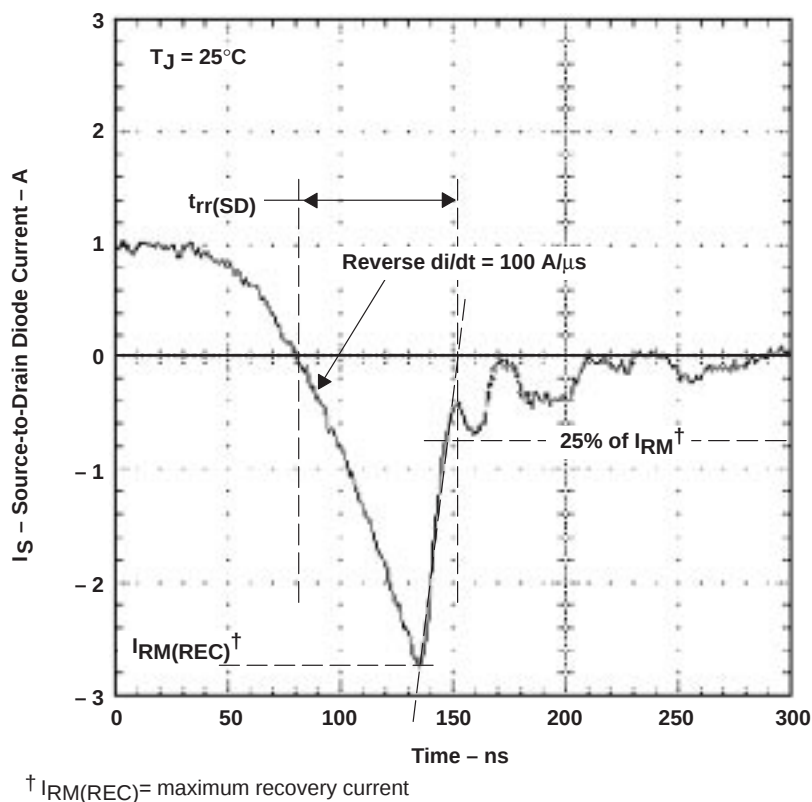


Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION

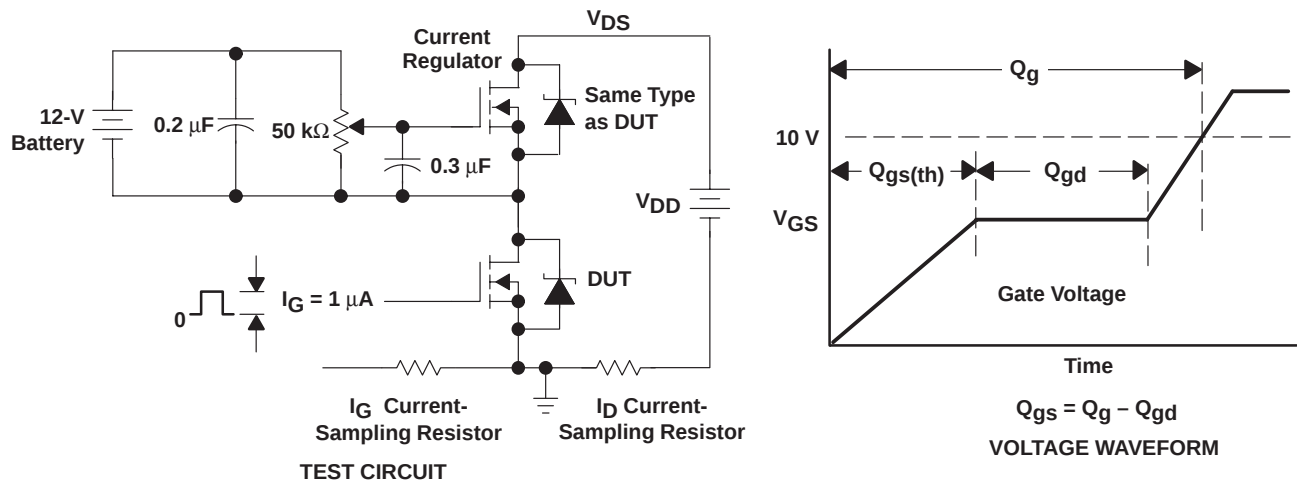
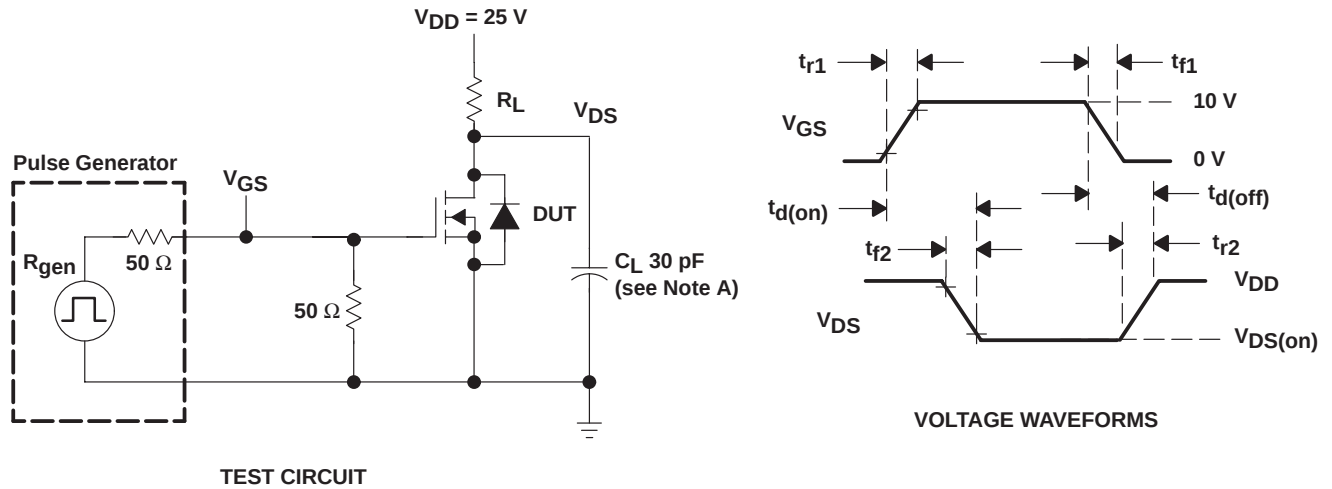


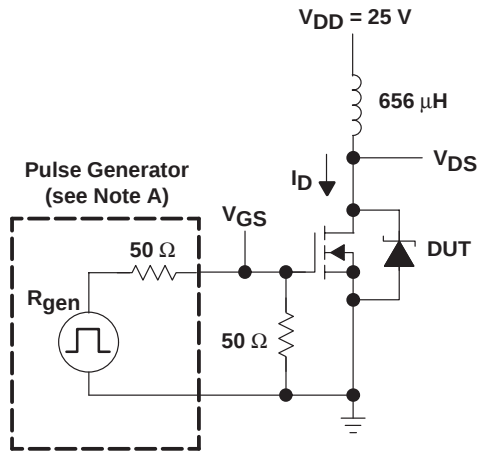
Figure 3. Gate-Charge Test Circuit and Voltage Waveform

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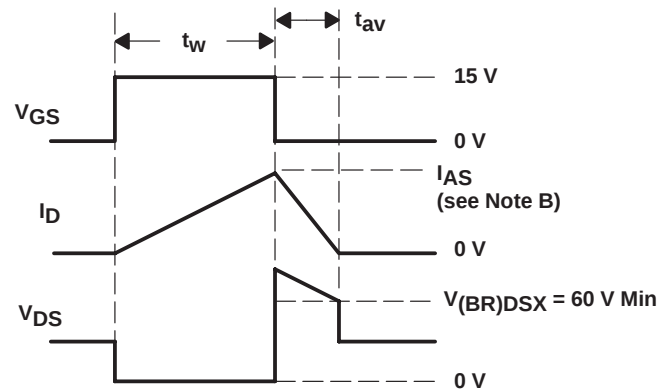
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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_0 = 50 \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 8$ A.

$$\text{Energy test level is defined as } E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 36 \text{ mJ, where}$$

t_{av} = Avalanche time

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

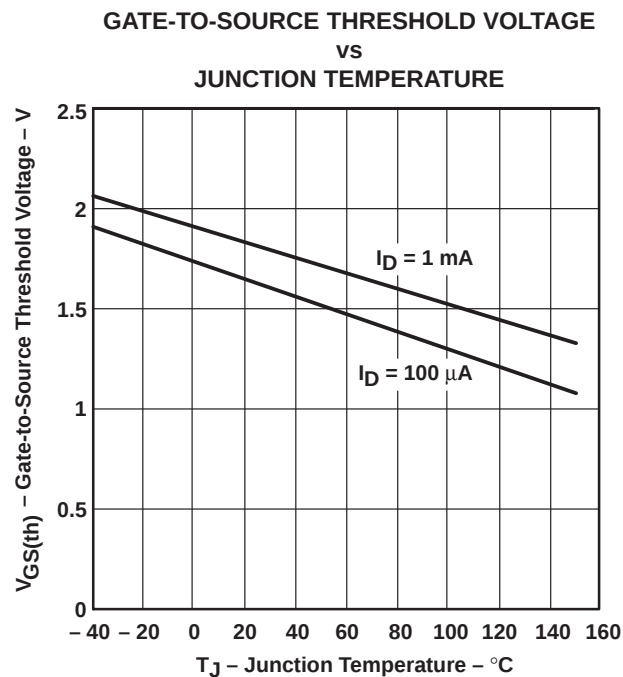


Figure 5

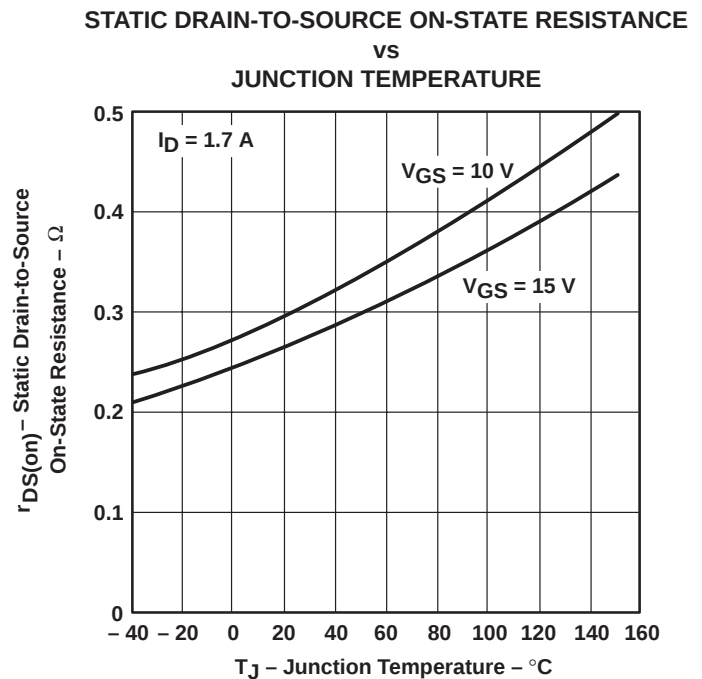


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

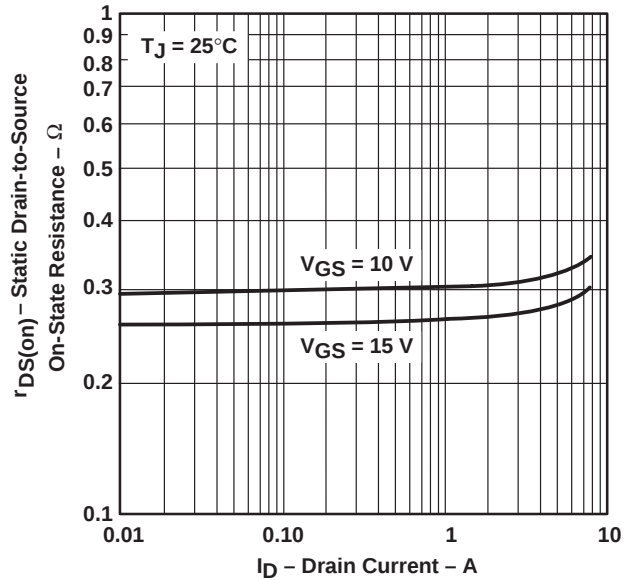


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

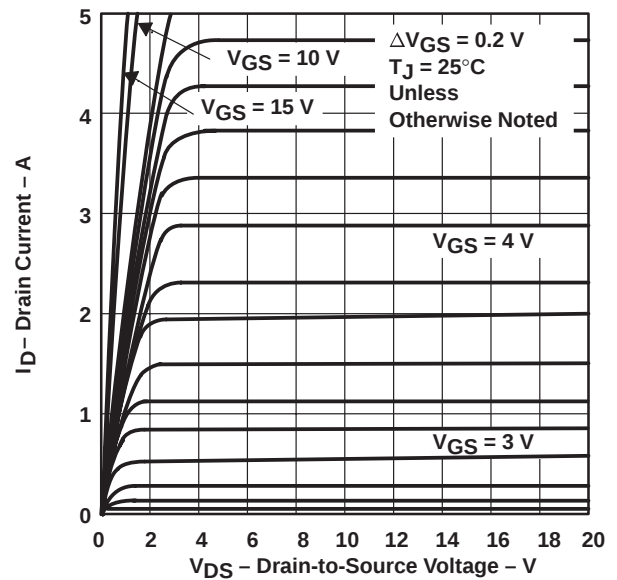


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

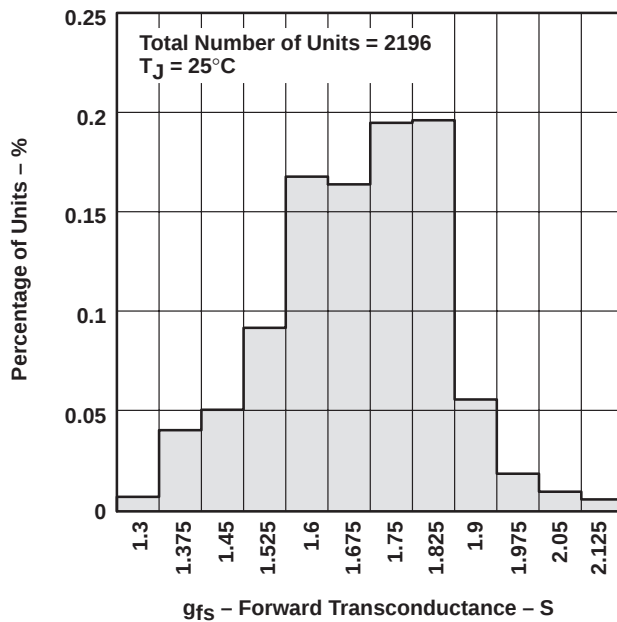


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

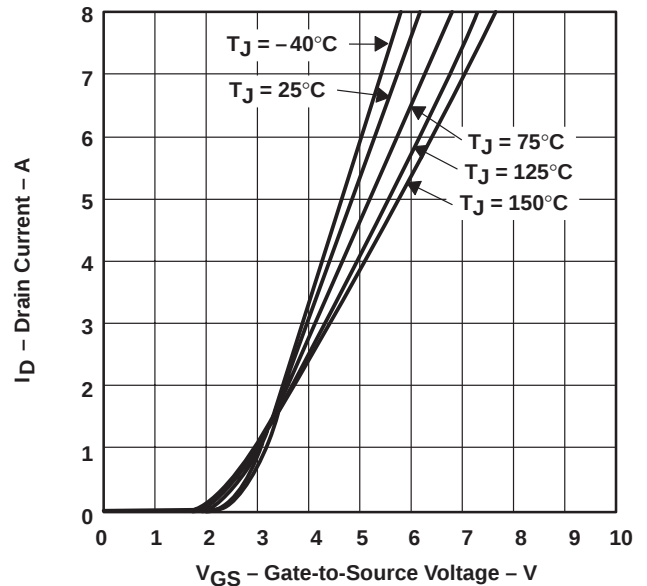


Figure 10

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TYPICAL CHARACTERISTICS

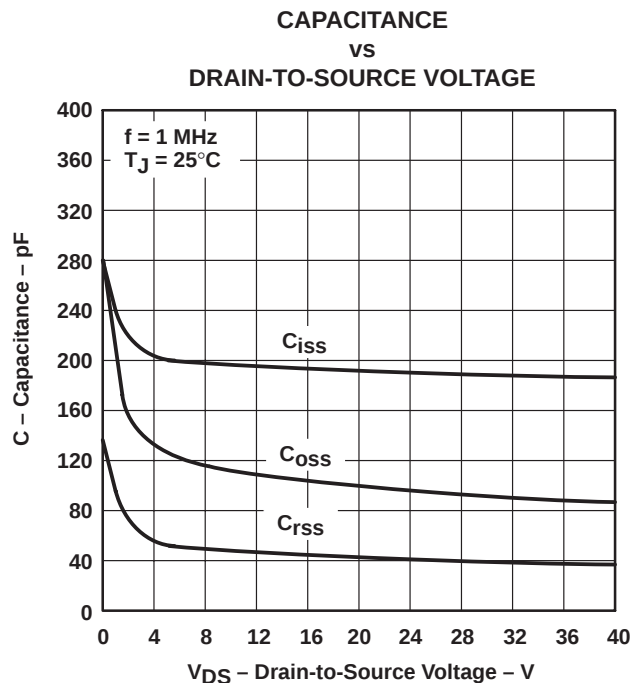


Figure 11

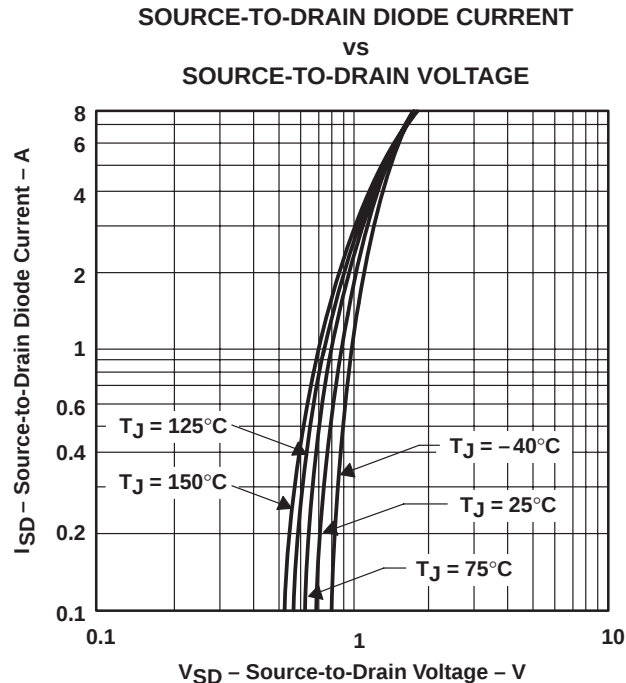


Figure 12

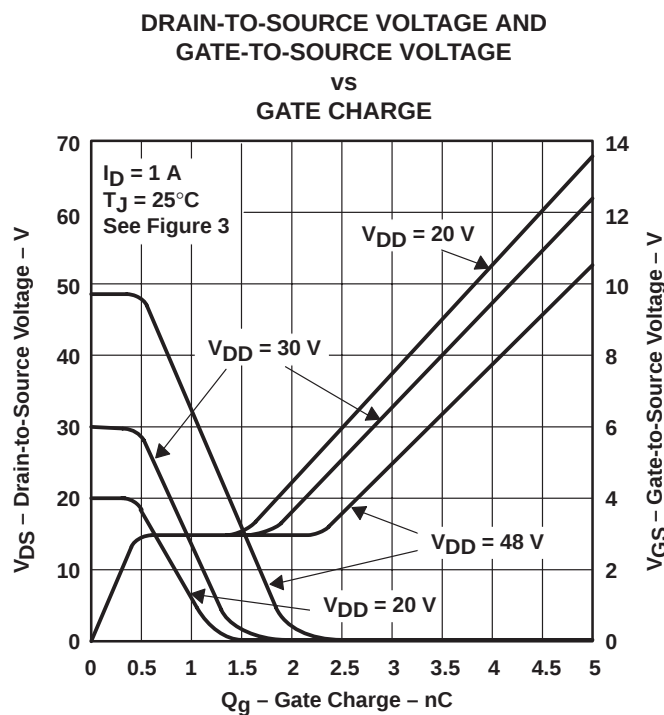


Figure 13

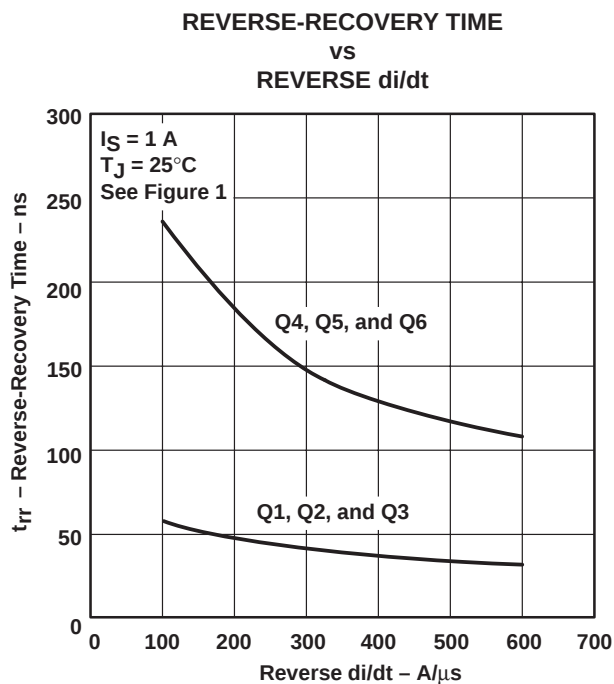
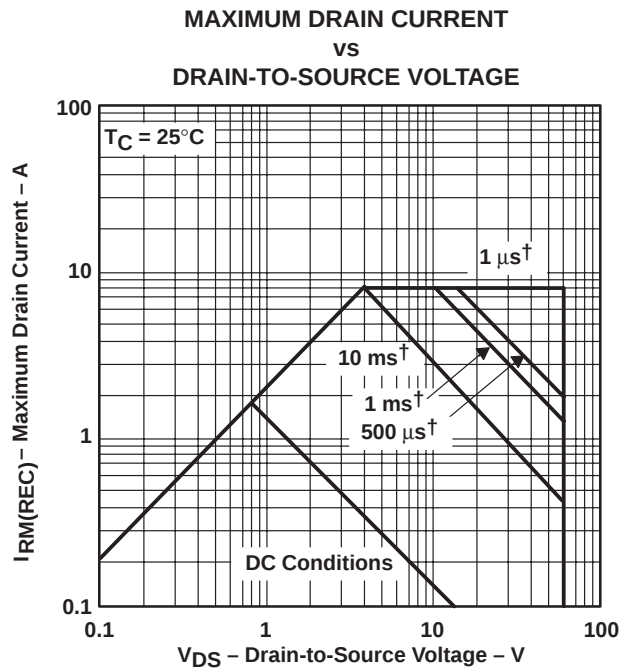


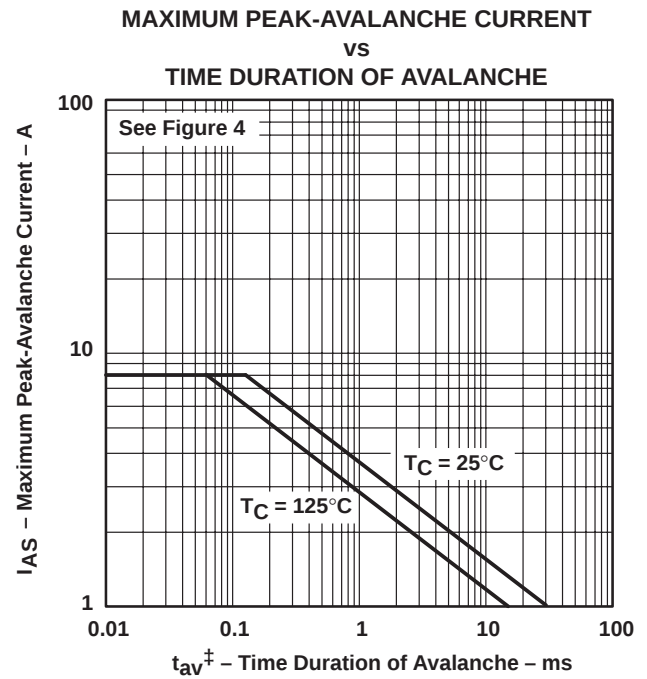
Figure 14

THERMAL INFORMATION



† Less than 0.1 duty cycle

Figure 15



‡ Non-JEDEC symbol for avalanche time.

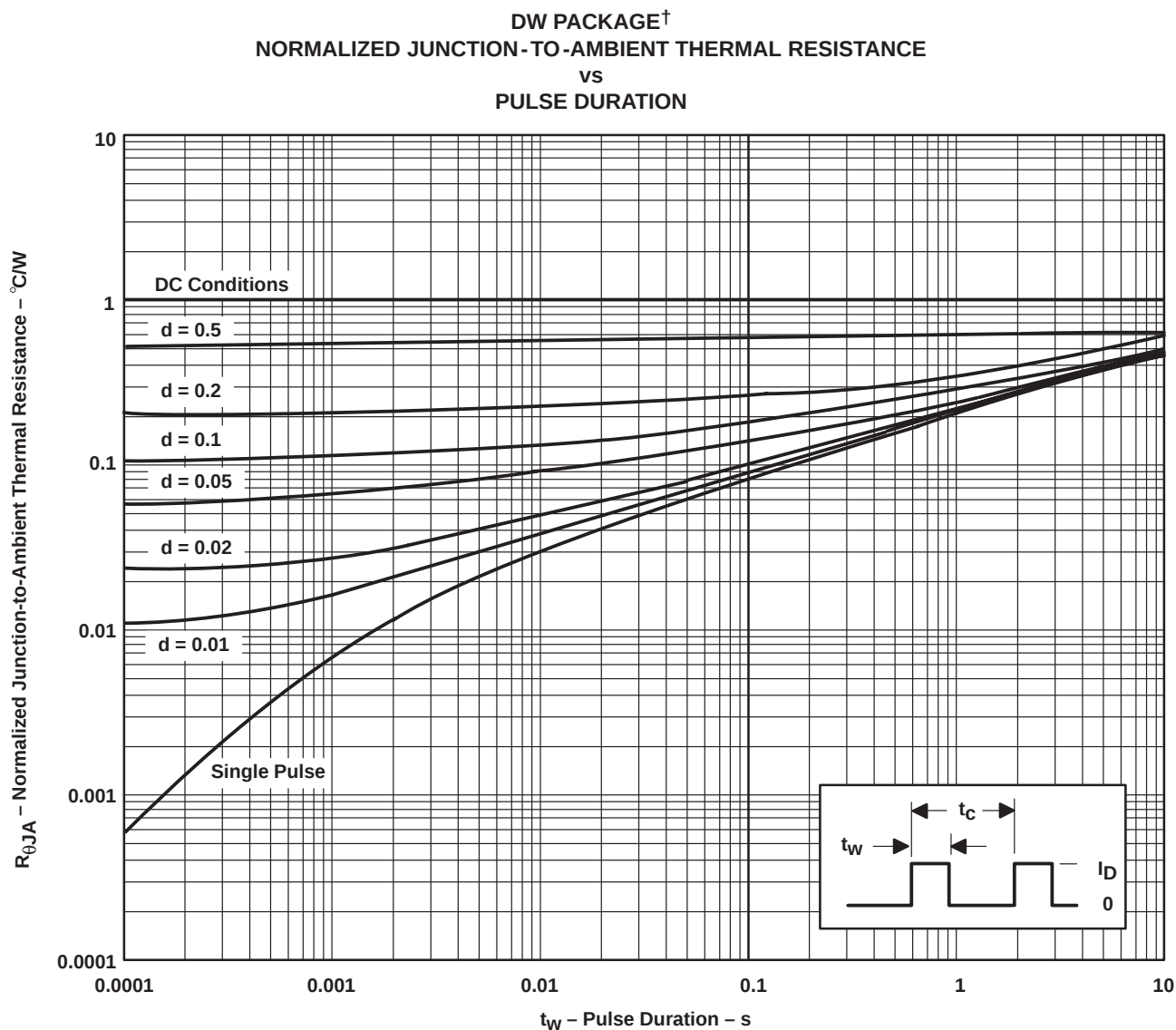
Figure 16

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THERMAL INFORMATION



[†] Device mounted on FR4 printed-circuit board with no heatsink

NOTE A: $Z_{\theta A}(t) = r(t) R_{\theta JA}$
 t_W = pulse duration
 t_C = cycle time
 d = duty cycle = t_W/t_C

Figure 17

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