

TPIC1321L 3-HALF H-BRIDGE GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

SLIS042 – NOVEMBER 1994

- Low $r_{DS(on)}$. . . 0.35 Ω Typ
- Voltage Output . . . 60 V
- Input Protection Circuitry . . . 18 V
- Pulsed Current . . . 4 A Per Channel
- Extended ESD Capability . . . 4000 V
- Direct Logic-Level Interface

description

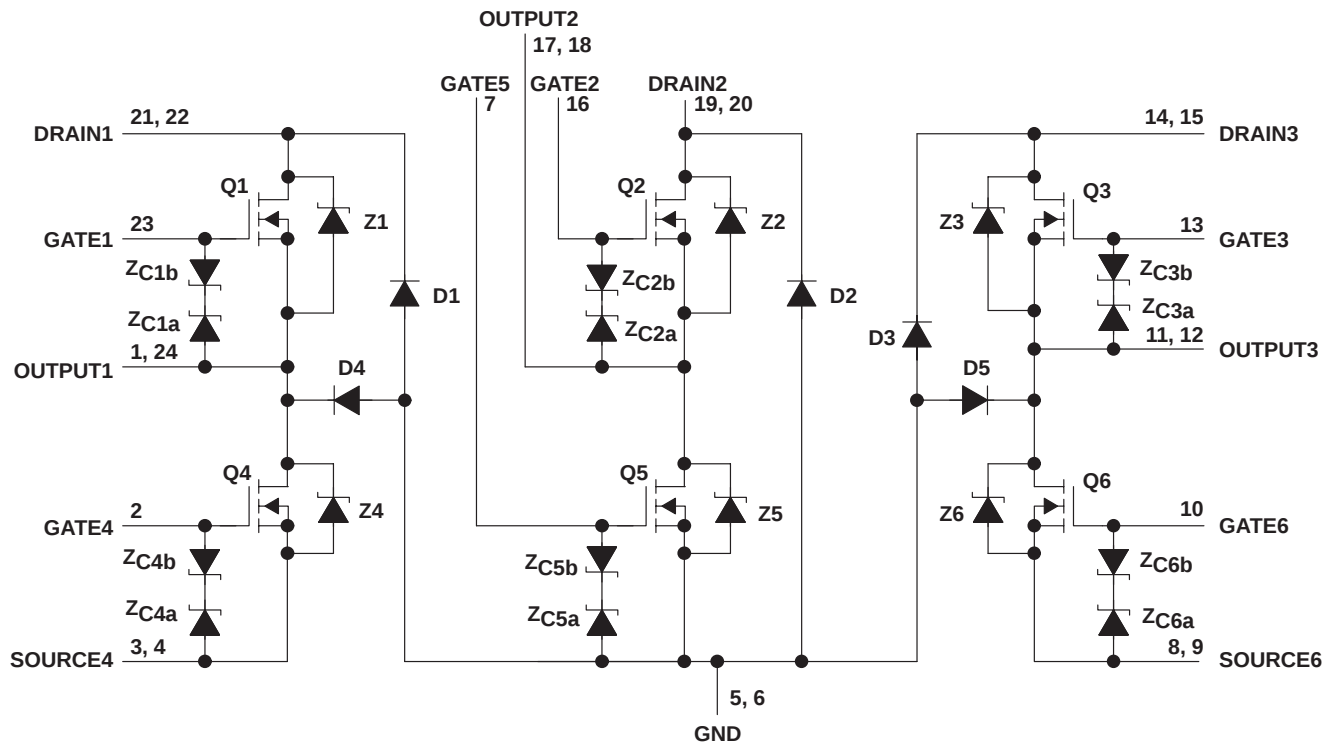
The TPIC1321L is a monolithic gate-protected logic-level power DMOS array that consists of six electrically isolated N-channel enhancement-mode DMOS transistors configured as 3-half H-bridges. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-k Ω resistor.

The TPIC1321L is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature of -40°C to 125°C .

DW PACKAGE
(TOP VIEW)

OUTPUT1	1	24	OUTPUT1
GATE4	2	23	GATE1
SOURCE4	3	22	DRAIN1
SOURCE4	4	21	DRAIN1
GND	5	20	DRAIN2
GND	6	19	DRAIN2
GATE5	7	18	OUTPUT2
SOURCE6	8	17	OUTPUT2
SOURCE6	9	16	GATE2
GATE6	10	15	DRAIN3
OUTPUT3	11	14	DRAIN3
OUTPUT3	12	13	GATE3

schematic



NOTE A: For correct operation, no terminal may be taken below GND.

TPIC1321L

3-HALF H-BRIDGE GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

SLIS042 – NOVEMBER 1994

absolute maximum ratings over operating case temperature range (unless otherwise noted)[†]

Drain-to-source voltage, V_{DS}	60 V
Output-to-GND voltage	60 V
Drain-to-GND voltage	100 V
SOURCE4, SOURCE6-to-GND voltage	60 V
Gate-to-source voltage range, V_{GS}	–9 V to 18 V
Continuous drain current, each output, $T_C = 25^\circ\text{C}$	1.25 A
Continuous source-to-drain diode current, $T_C = 25^\circ\text{C}$	1.25 A
Pulsed drain current, each output, I_{max} , $T_C = 25^\circ\text{C}$ (see Note 1 and Figure 15)	4 A
Continuous gate-to-source zener-diode current, $T_C = 25^\circ\text{C}$	± 50 mA
Pulsed gate-to-source zener-diode current, $T_C = 25^\circ\text{C}$	± 500 mA
Single-pulse avalanche energy, E_{AS} , $T_C = 25^\circ\text{C}$ (see Figures 4 and 16)	96 mJ
Continuous total dissipation, $T_C = 25^\circ\text{C}$ (see Figure 15)	1.39 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TPIC1321L
3-HALF H-BRIDGE GATE-PROTECTED LOGIC-LEVEL
POWER DMOS ARRAY
 SLIS042 – NOVEMBER 1994

electrical characteristics, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1\ \text{mA}$, See Figure 5	$V_{DS} = V_{GS}$,	1.5	1.75	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	$I_{GS} = 250\ \mu\text{A}$		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	$I_{SG} = 250\ \mu\text{A}$		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, D3, D4, D5)	Drain-to-GND current = $250\ \mu\text{A}$		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	$I_D = 1.25\ \text{A}$, See Notes 2 and 3	$V_{GS} = 5\ \text{V}$,		0.44	0.5	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	$I_S = 1.25\ \text{A}$, $V_{GS} = 0$ (Z1 – Z6), See Notes 2 and 3 and Figure 12			0.9	1.1	V
V_F	Forward on-state voltage, GND-to-drain	$I_D = 1.25\ \text{A}$ (D1 – D5) See Notes 2 and 3			4		V
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = 48\ \text{V}$, $V_{GS} = 0$	$T_C = 25^\circ\text{C}$		0.05	1	μA
			$T_C = 125^\circ\text{C}$		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	$V_{GS} = 15\ \text{V}$, $V_{DS} = 0$			20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	$V_{SG} = 5\ \text{V}$, $V_{DS} = 0$			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	$V_{DGND} = 48\ \text{V}$	$T_C = 25^\circ\text{C}$		0.05	1	μA
			$T_C = 125^\circ\text{C}$		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 5\ \text{V}$, $I_D = 1.25\ \text{A}$, See Notes 2 and 3 and Figures 6 and 7	$T_C = 25^\circ\text{C}$		0.35	0.4	Ω
			$T_C = 125^\circ\text{C}$		0.57	0.6	
g_{fs}	Forward transconductance	$V_{DS} = 15\ \text{V}$, See Notes 2 and 3 and Figure 9	$I_D = 625\ \text{mA}$,	1.6	1.74		S
C_{iss}	Short-circuit input capacitance, common source	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$,	$V_{GS} = 0$, See Figure 11		200	250	pF
C_{oss}	Short-circuit output capacitance, common source				175	220	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				40	75	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
 3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, $T_C = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	$I_S = 625\ \text{mA}$, $V_{GS} = 0$,	$V_{DS} = 48\ \text{V}$, $di/dt = 100\ \text{A}/\mu\text{s}$,		45		ns
Q_{RR}	Total diode charge	See Figures 1 and 14	Z1, Z2, and Z3		50		nC

TPIC1321L
3-HALF H-BRIDGE GATE-PROTECTED LOGIC-LEVEL
POWER DMOS ARRAY

SLIS042 – NOVEMBER 1994

resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$ Turn-on delay time	$V_{DD} = 25\text{ V}$, $R_L = 40\ \Omega$, $t_{en} = 10\text{ ns}$, $t_{dis} = 10\text{ ns}$, See Figure 2		34	70	ns
$t_{d(off)}$ Turn-off delay time			80	150	
t_r Rise time			28	55	
t_f Fall time			15	30	
Q_g Total gate charge	$V_{DS} = 48\text{ V}$, $I_D = 625\text{ mA}$, $V_{GS} = 5\text{ V}$, See Figure 3		4.6	5.8	nC
$Q_{gs(th)}$ Threshold gate-to-source charge			0.7	0.88	
Q_{gd} Gate-to-drain charge			2.5	3.13	
L_D Internal drain inductance			5		nH
L_S Internal source inductance			5		
R_g Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	See Notes 4 and 7		90		$^\circ\text{C/W}$
$R_{\theta JB}$ Junction-to-board thermal resistance	See Notes 5 and 7		44.5		
$R_{\theta JP}$ Junction-to-pin thermal resistance	See Notes 6 and 7		28		

NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.
5. Package mounted on a 24 in², 4-layer FR4 printed-circuit board.
6. Package mounted in intimate contact with infinite heatsink.
7. All outputs with equal power

PARAMETER MEASUREMENT INFORMATION

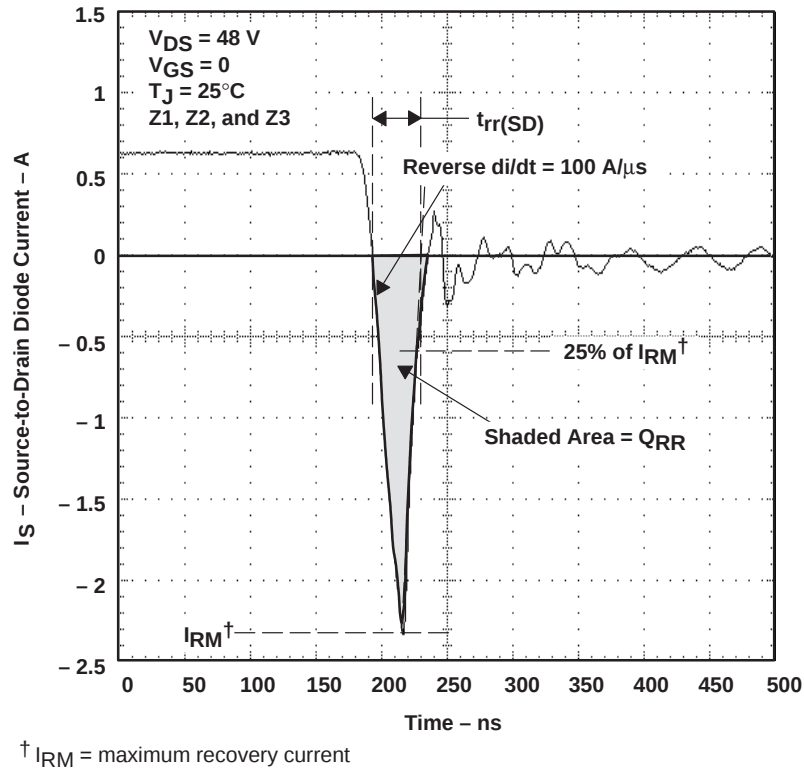
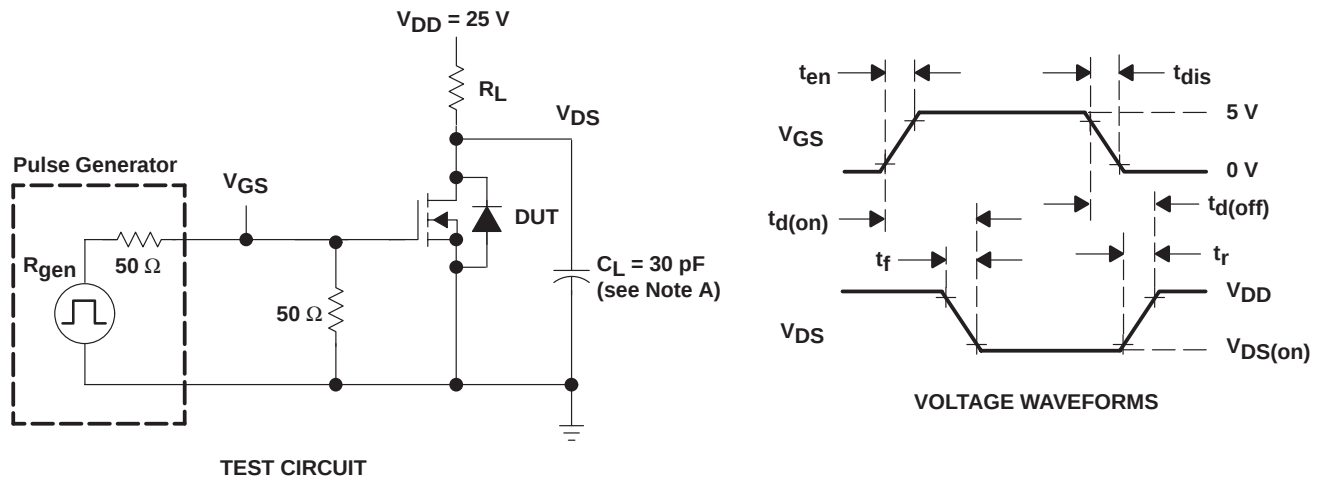


Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



NOTE A: C_L includes probe and jig capacitance.

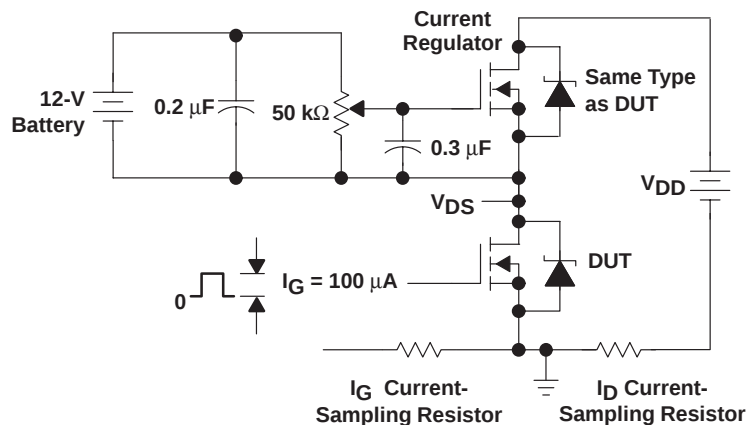
Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

TPIC1321L

3-HALF H-BRIDGE GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

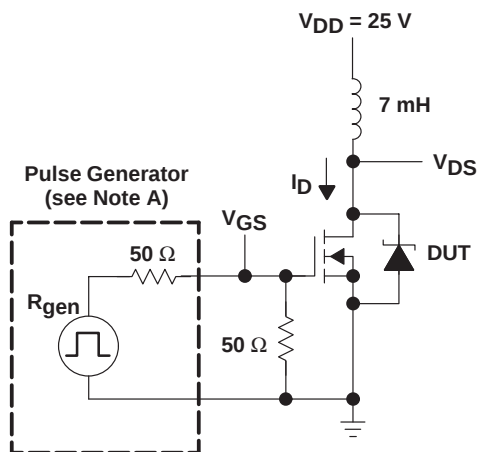
SLIS042 – NOVEMBER 1994

PARAMETER MEASUREMENT INFORMATION

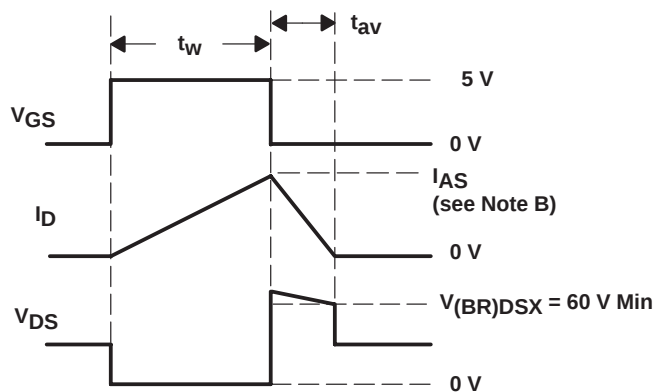


TEST CIRCUIT

Figure 3. Gate-Charge Test Circuit and Voltage Waveform



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 4$ A.

$$\text{Energy test level is defined as } E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 96 \text{ mJ.}$$

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

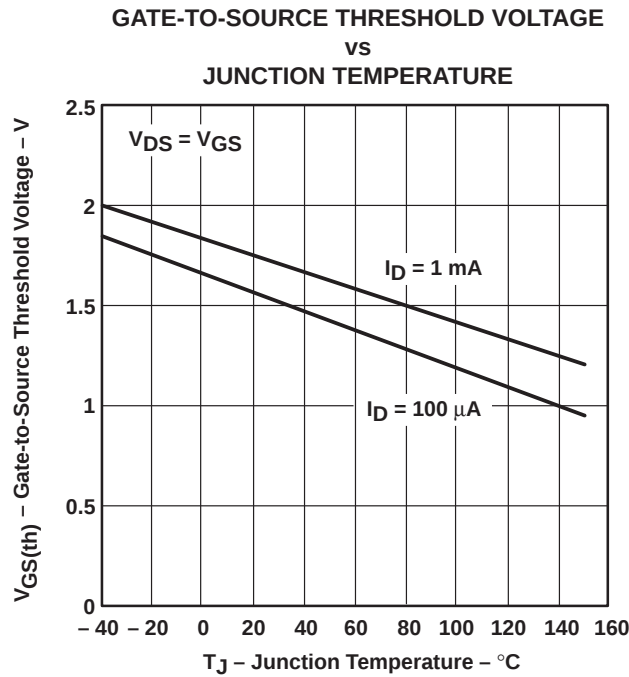


Figure 5

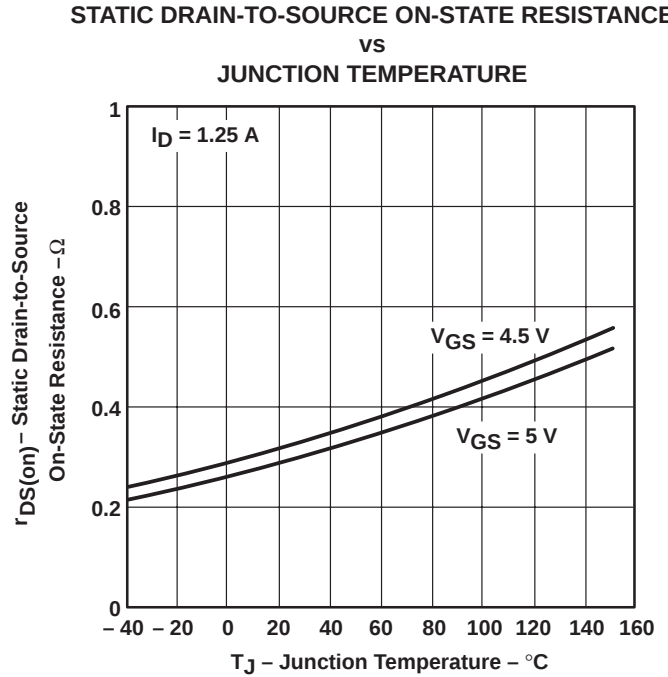


Figure 6

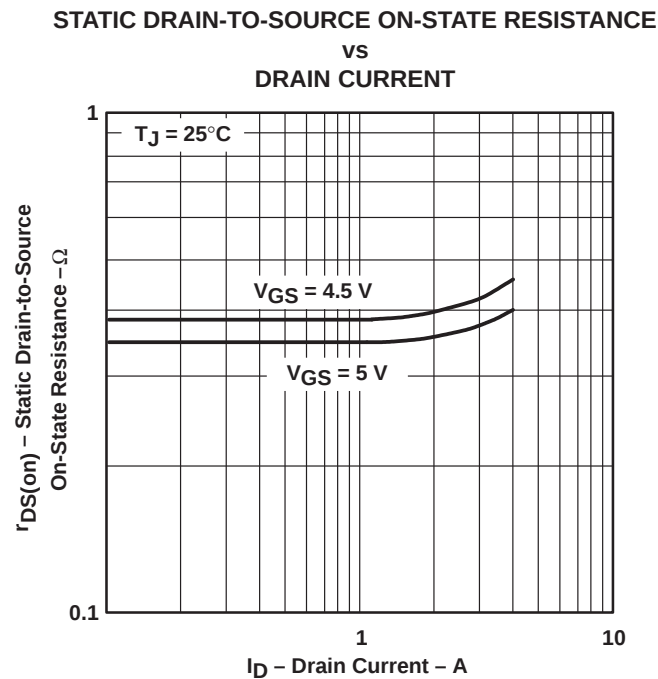


Figure 7

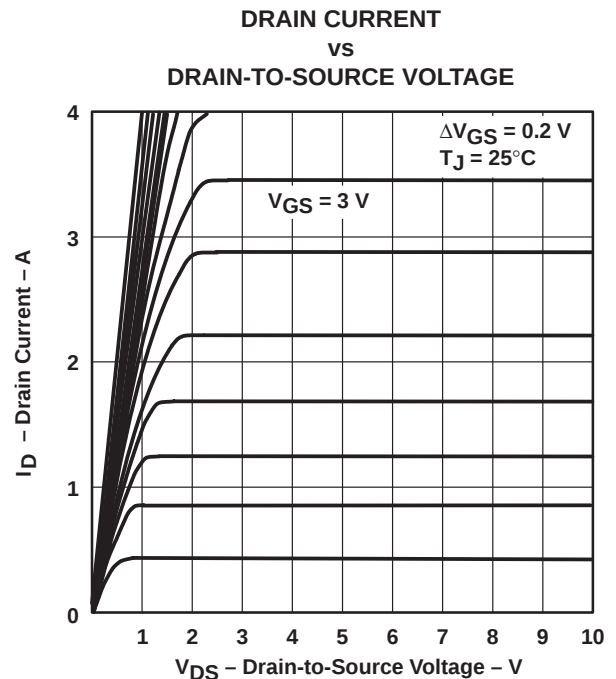


Figure 8

TPIC1321L

3-HALF H-BRIDGE GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

SLIS042 – NOVEMBER 1994

TYPICAL CHARACTERISTICS

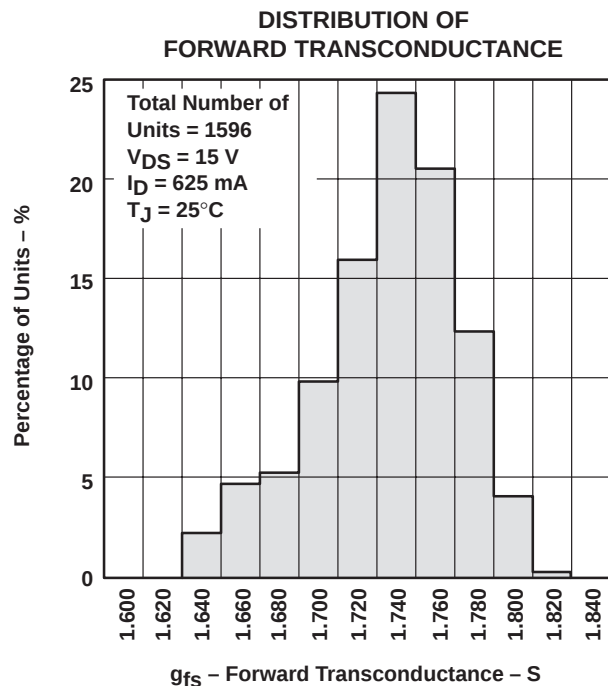


Figure 9

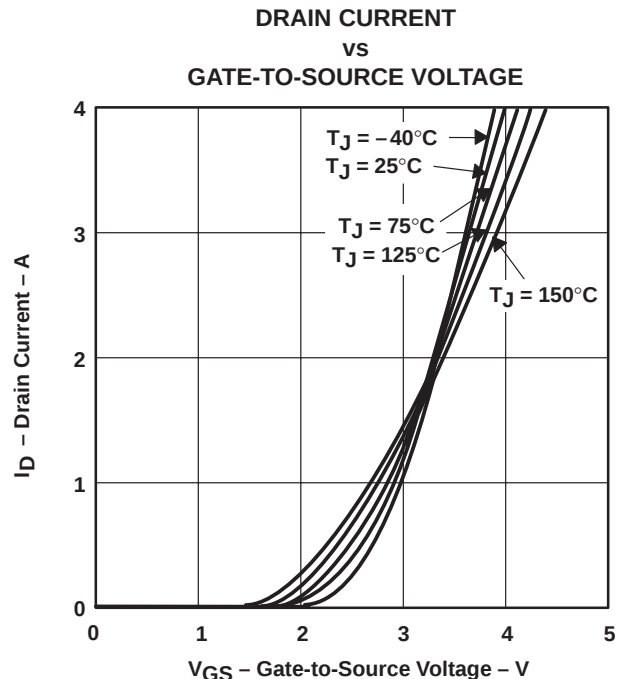


Figure 10

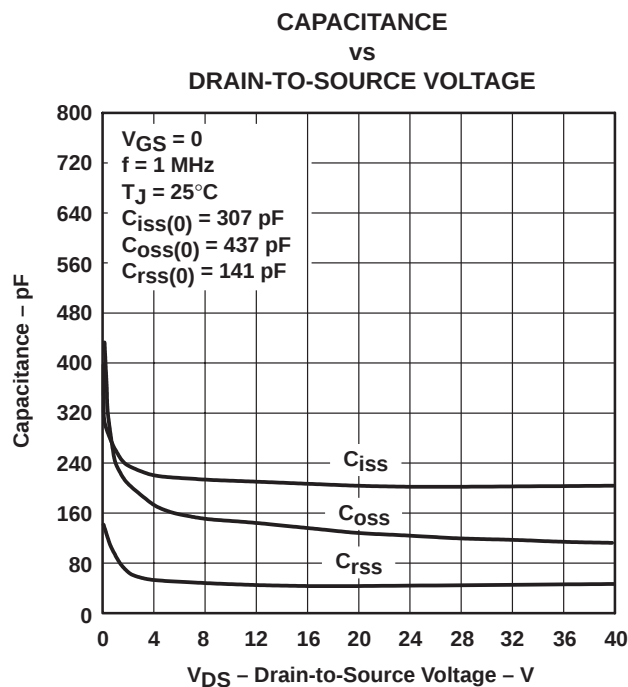


Figure 11

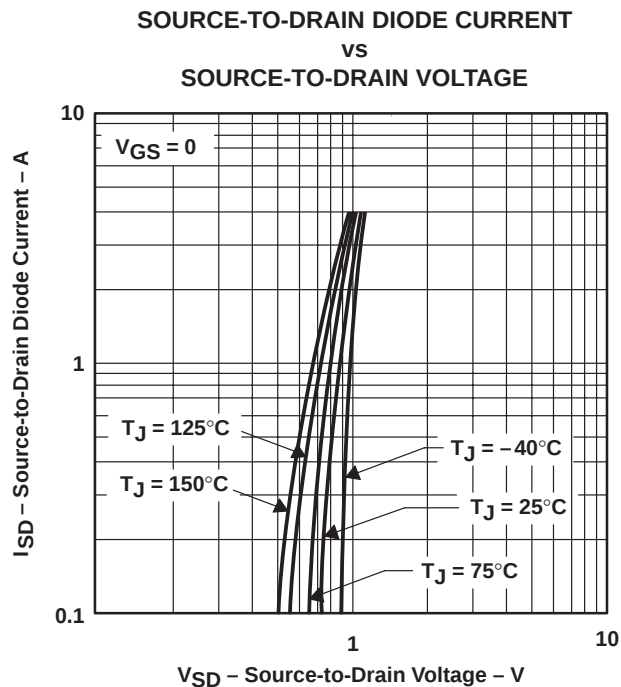


Figure 12

TYPICAL CHARACTERISTICS

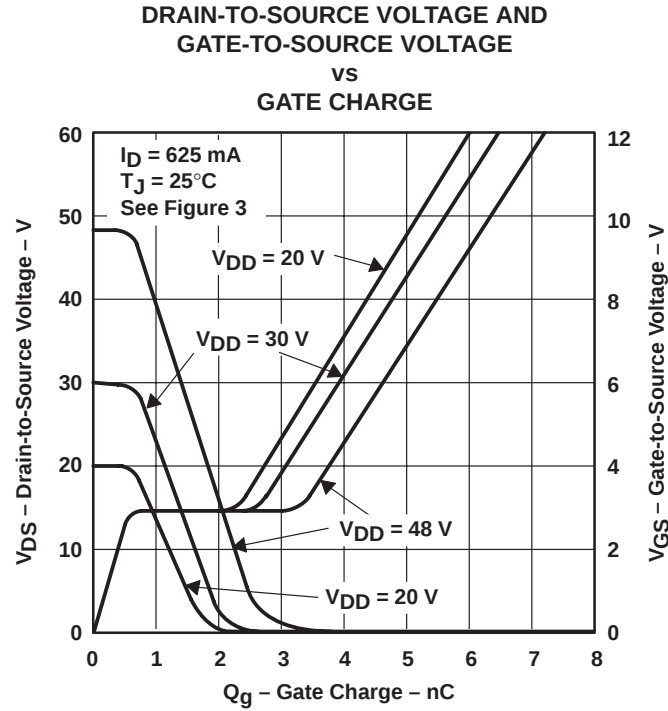


Figure 13

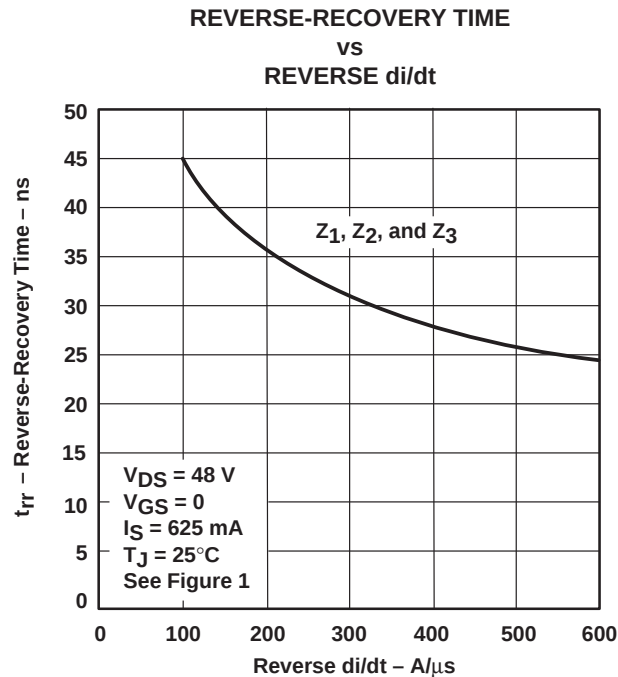
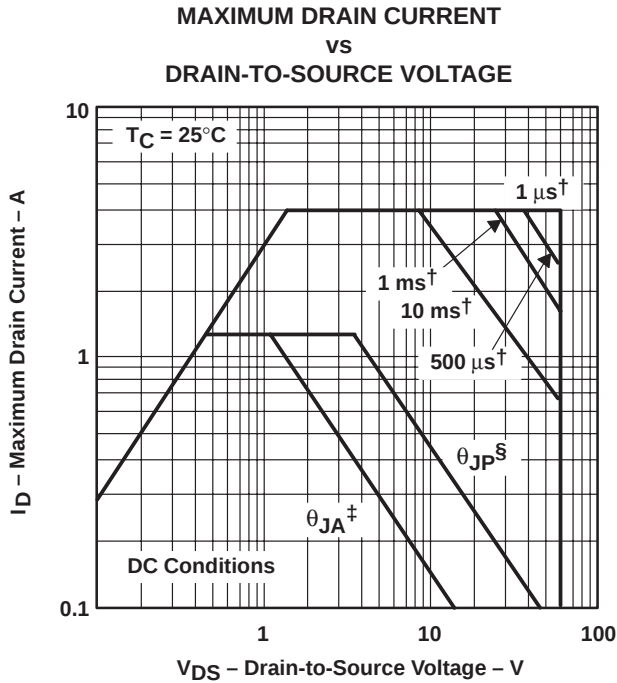


Figure 14

TPIC1321L
3-HALF H-BRIDGE GATE-PROTECTED LOGIC-LEVEL
POWER DMOS ARRAY

SLIS042 – NOVEMBER 1994

THERMAL INFORMATION



[†] Less than 2% duty cycle

[‡] Device mounted on FR4 printed-circuit board with no heatsink.

[§] Device mounted in intimate contact with infinite heatsink.

Figure 15

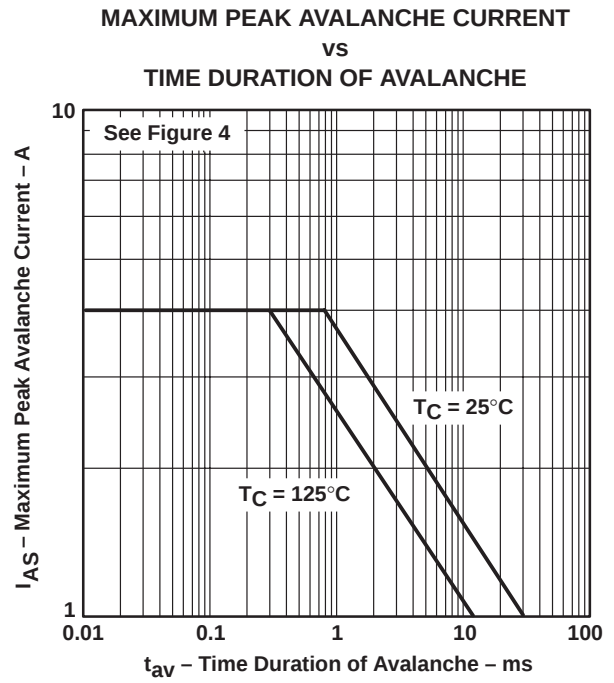
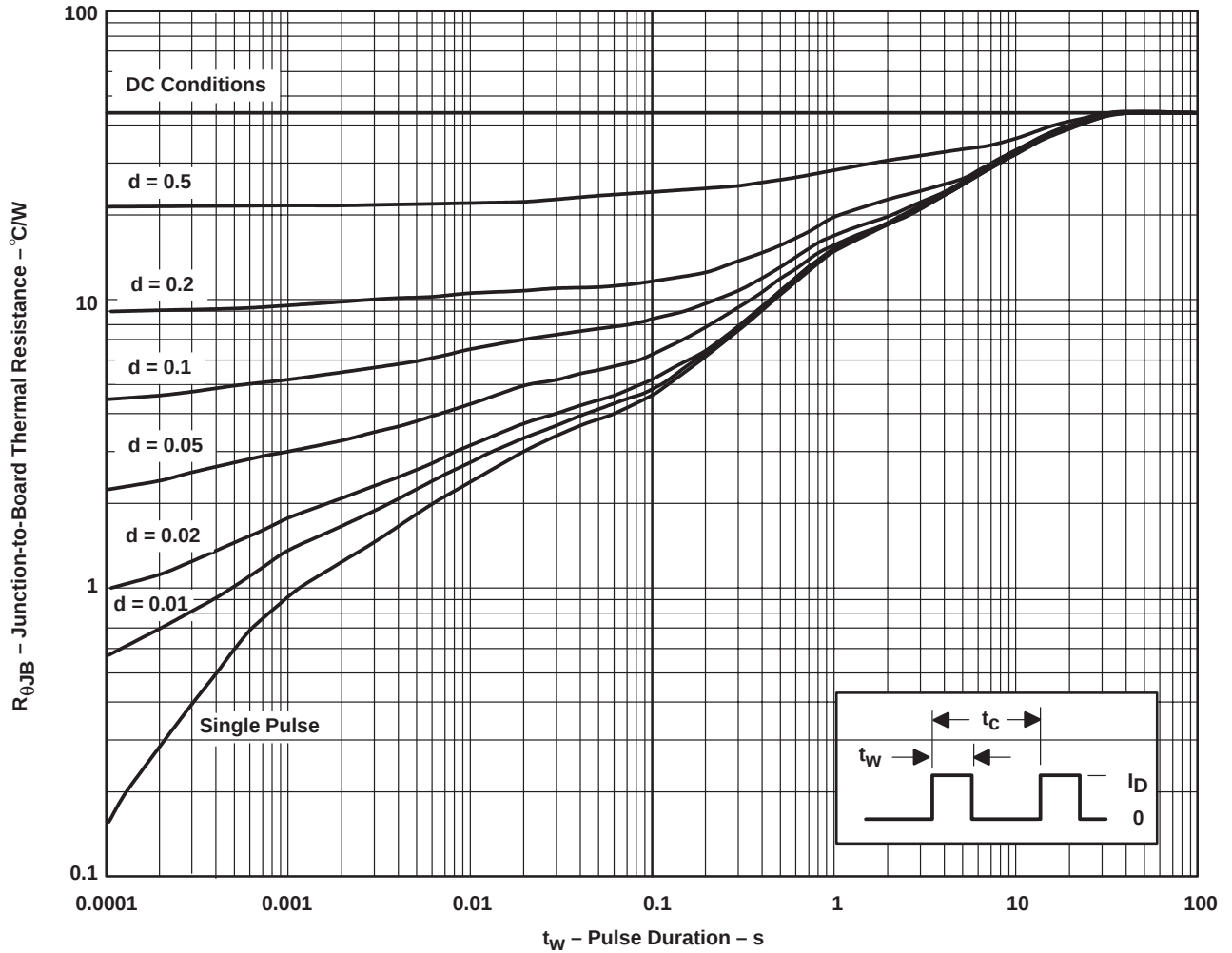


Figure 16

THERMAL INFORMATION

DW PACKAGE[†]
JUNCTION-TO-BOARD THERMAL RESISTANCE
VS
PULSE DURATION



[†] Device mounted on 24 in², 4-layer FR4 printed-circuit board with no heatsink.

NOTE A: $Z_{\theta B}(t) = r(t) R_{\theta JB}$
 t_W = pulse duration
 t_C = cycle time
 d = duty cycle = t_W/t_C

Figure 17

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.