

Preliminary W24256



32K × 8 CMOS STATIC RAM

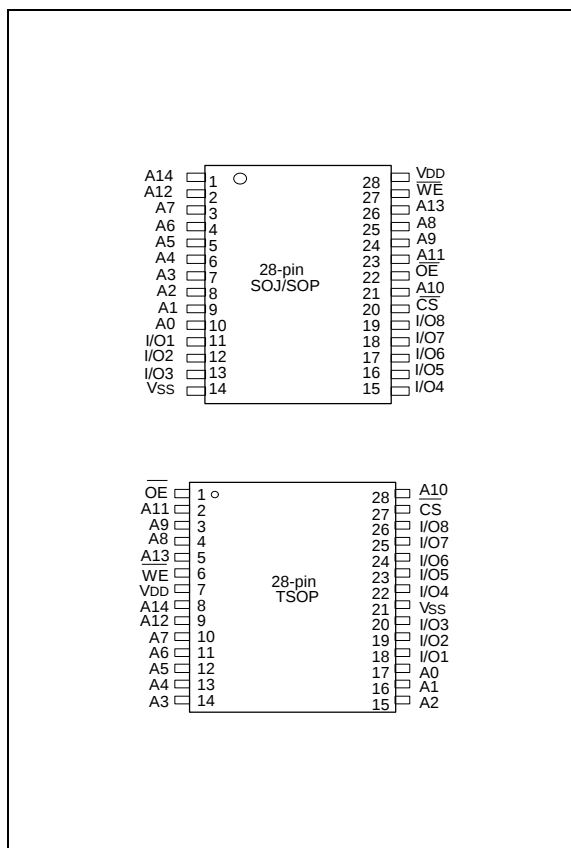
GENERAL DESCRIPTION

The W24256 is a normal speed, low power CMOS static RAM organized as 32768 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

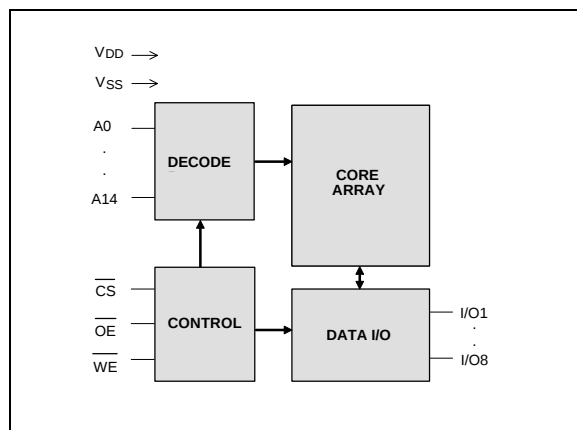
FEATURES

- High speed access time: 35 nS (max.)
- Low power consumption:
 - Active: 550 mW (max.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Available packages: 28-pin 300 mil SOJ, 330mil SOP, and standard type one TSOP (8 mm × 13.4 mm)

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A14	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
VSS	Ground

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DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to VSS Potential	-0.5 to +7.0	V
Input/Output to Vss Potential	-0.5 to VDD +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

TRUTH TABLE

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	MODE	I/O1- I/O8	VDD CURRENT
H	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	Output Disable	High Z	IDD
L	L	H	Read	Data Out	IDD
L	X	L	Write	Data In	IDD

OPERATING CHARACTERISTICS

(VDD = 5V $\pm$ 10%, VSS = 0V, TA = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Low Voltage	VIL	-	-0.5	-	+0.8	V
Input High Voltage	VIH	-	+2.2	-	VDD +0.5	V
Input Leakage Current	ILI	VIN = VSS to VDD	-5	-	+5	μ A
Output Leakage Current	ILO	V _{I/O} = VSS to VDD, $\overline{\text{CS}}$ = VIH or $\overline{\text{OE}}$ = VIH or $\overline{\text{WE}}$ = VIL	-5	-	+5	μ A
Output Low Voltage	VOL	IOL = +2.1 mA	-	-	0.4	V
Output High Voltage	VOH	IOH = -1 mA	2.4	-	-	V
Operating Power Supply Current	IDD	$\overline{\text{CS}}$ = VIL, I/O = 0 mA Cycle = min , Duty = 100%	-	-	110	mA
Standby Power Supply Current	ISB	$\overline{\text{CS}}$ = VIH Cycle = MIN., Duty = 100%	-	-	25	mA
	ISB1	$\overline{\text{CS}}$ $\geq$ VDD -0.2V	-	-	1	mA

Note: Typical characteristics are at VDD = 5V, TA = 25° C.

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CAPACITANCE

($V_{DD} = 5V$, $T_A = 25^\circ C$, $f = 1 MHz$)

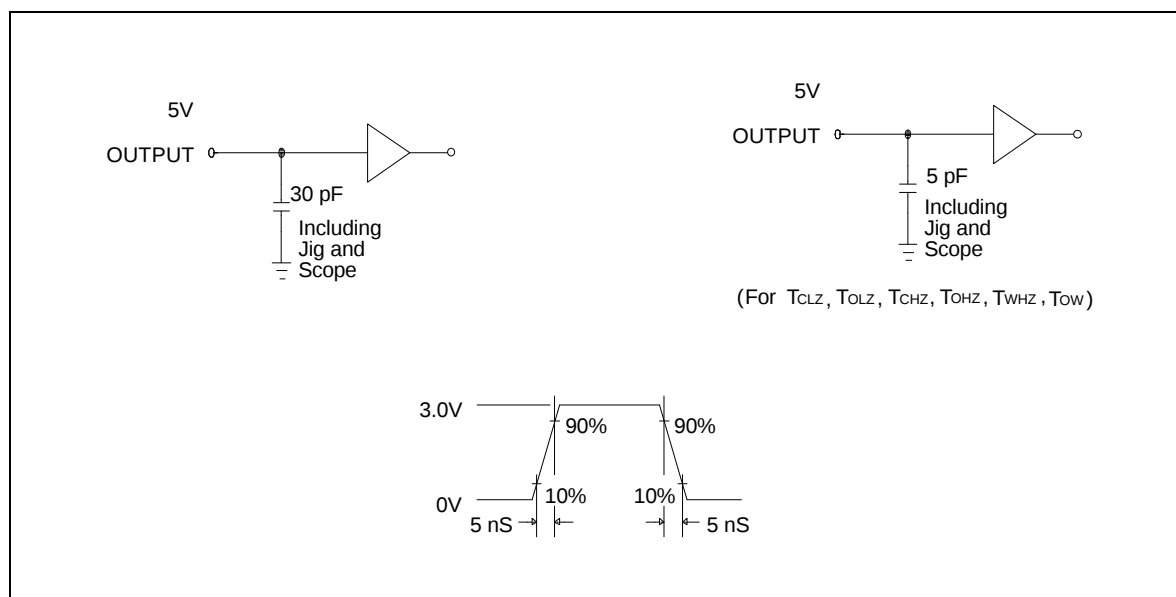
PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C _{IN}	V _{IN} = 0V	8	pF
Input/Output Capacitance	C _{I/O}	V _{OUT} = 0V	10	pF

Note: These parameters are sampled but not 100% tested.

AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	C _L = 30 pF + 1 TTL, I _{OH} /I _{OL} = -1 mA/2.1 mA

AC TEST LOADS AND WAVEFORM



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AC CHARACTERISTICS

(VDD = 5V $\pm$ 10%, VSS = 0V, TA = 0 to 70°C)

Read Cycle

PARAMETER	SYM.	W24256-35		UNIT
		MIN.	MAX.	
Read Cycle Time	TRC	35	-	nS
Address Access Time	TAA	-	35	nS
Chip Select Access Time	TACS	-	35	nS
Output Enable to Output Valid	TAOE	-	12	nS
Chip Selection to Output in Low Z	TCLZ*	3	-	nS
Output Enable to Output in Low Z	TOLZ*	0	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	7	nS
Output Disable to Output in High Z	TOHZ*	-	7	nS
Output Hold from Address Change	TOH	3	-	nS

* These parameters are sampled but not 100% tested.

Write Cycle

PARAMETER		SYM.	W24256-35		UNIT
			MIN.	MAX.	
Write Cycle Time		TWC	35	-	nS
Chip Selection to End of Write		TCW	20	-	nS
Address Valid to End of Write		TAW	20	-	nS
Address Setup Time		TAS	0	-	nS
Write Pulse Width		TWP	15	-	nS
Write Recovery Time	$\overline{CS}$, $\overline{WE}$	TWR	1.5	-	nS
Data Valid to End of Write		TDW	10	-	nS
Data Hold from End of Write		TDH	0	-	nS
Write to Output in High Z		TWHZ*	-	5	nS
Output Disable to Output in High Z		TOHZ*	-	5	nS
Output Active from End of Write		TOW	3	-	nS

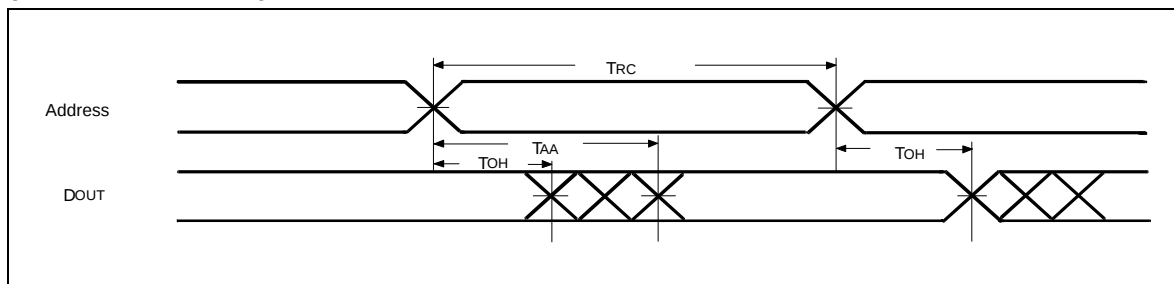
* These parameters are sampled but not 100% tested.



TIMING WAVEFORMS

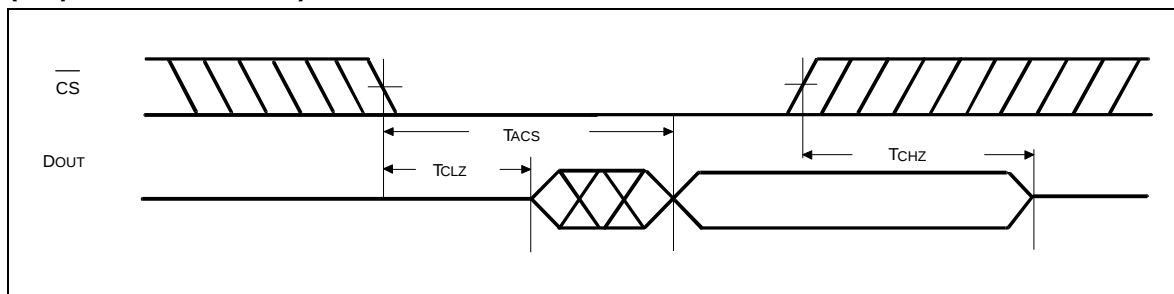
Read Cycle 1

(Address Controlled)



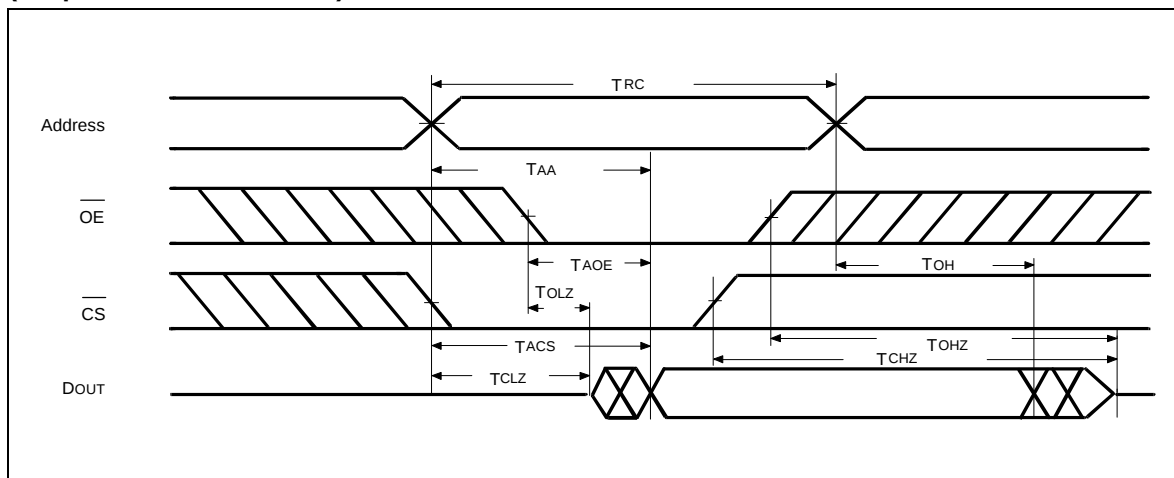
Read Cycle 2

(Chip Select Controlled)



Read Cycle 3

(Output Enable Controlled)

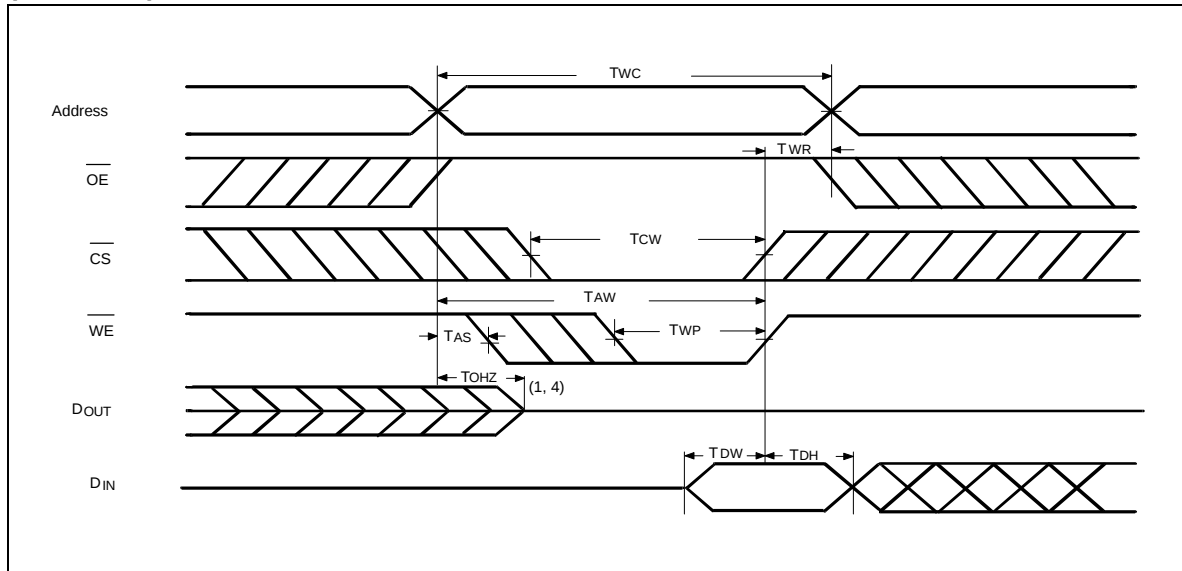




Timing Waveforms, continued

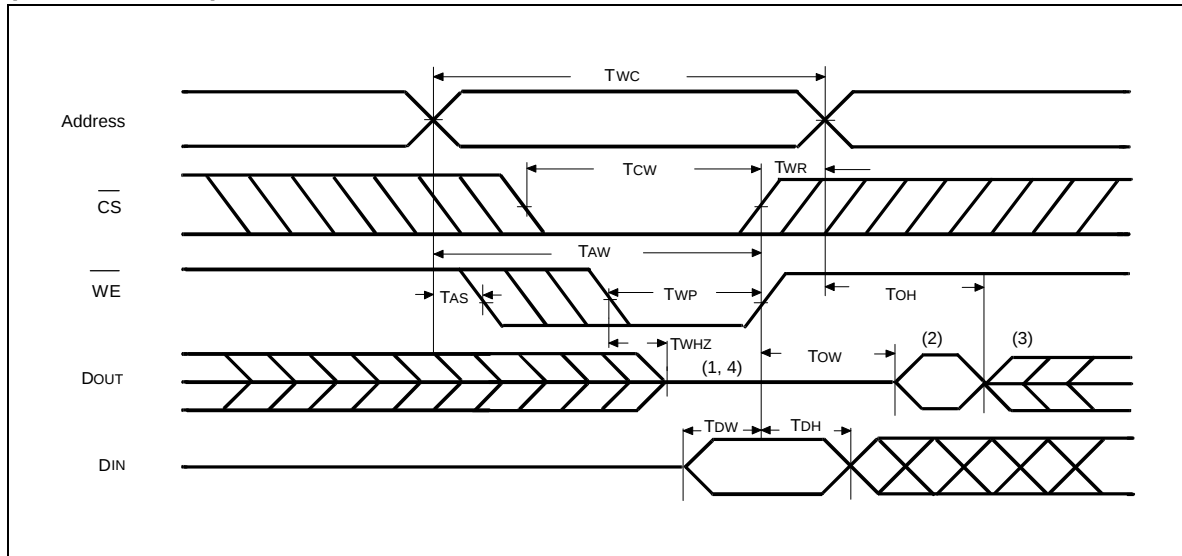
Write Cycle 1

($\overline{\text{OE}}$ Clock)



Write Cycle 2

($\overline{\text{OE}}$ = VIL Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.

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ORDERING INFORMATION

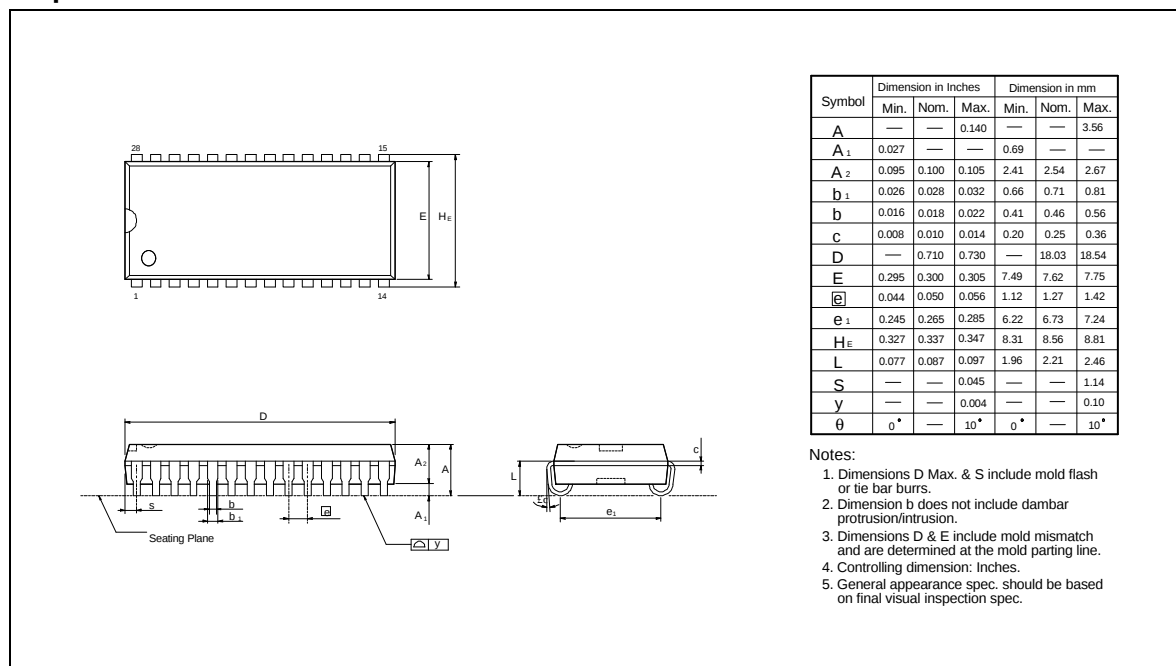
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24256J-35	35	110	1	300 mil SOJ
W24256S-35	35	110	1	330 mil SOP
W24256Q-35	35	110	1	Standard type one TSOP

Notes:

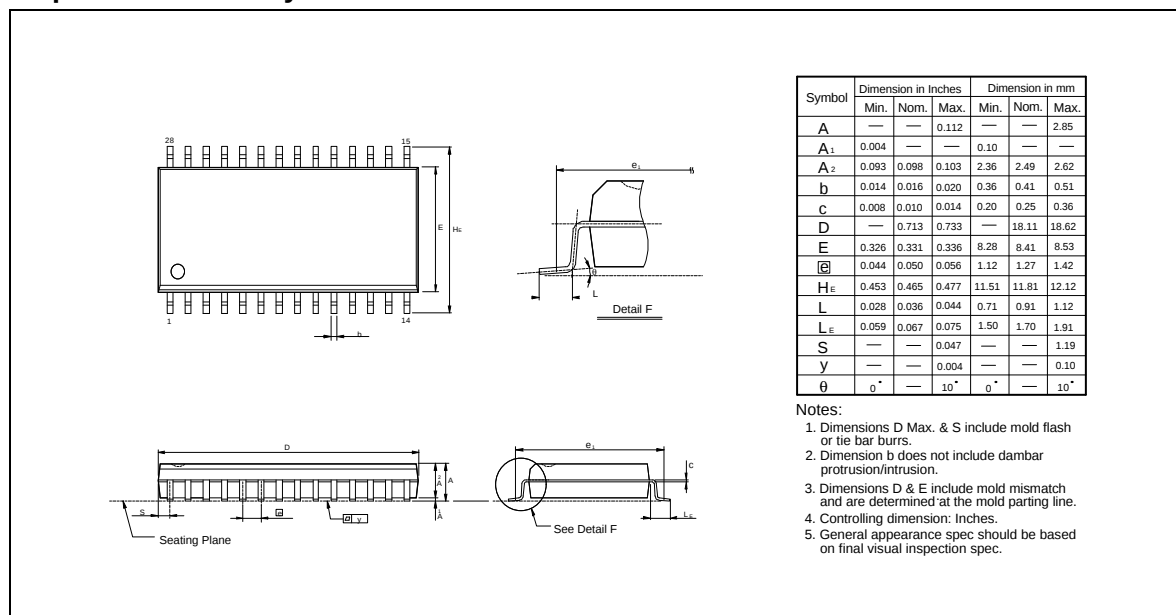
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

28-pin Small Outline J Band

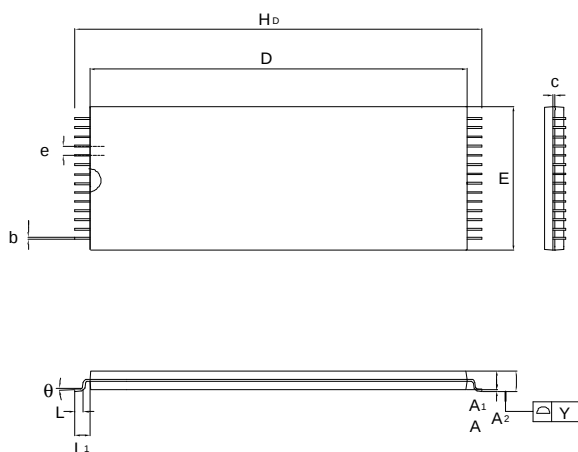


28-pin SO Wide Body



Package Dimensions, continued

28-pin Standard Type One TSOP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A ₁	0.002	—	0.006	0.05	—	0.15
A ₂	0.035	0.040	0.041	0.95	1.00	1.05
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	0.006	0.008	0.10	0.15	0.21
D	0.461	0.465	0.469	11.70	11.80	11.90
E	0.311	0.315	0.319	7.90	8.00	8.10
H ₀	0.520	0.528	0.536	13.20	13.40	13.60
e	—	0.022	—	—	0.55	—
L	0.020	0.024	0.028	0.50	0.60	0.70
L ₁	—	0.010	—	—	0.25	—
Y	0.000	—	0.004	0.00	—	0.10
θ	0	3	5	0	3	5

Note: Controlling dimension: Millimeters

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VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	May 2000	-	Initial Issued



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Note: All data and specifications are subject to change without notice.