ZARLINK SEMICONDUCTOR

ZL40122

High Speed, Current Feedback Quad Operational Amplifier

Data Sheet

April 2003

Features

- 450MHz small signal bandwidth
- 1500V/µs slew rate
- 5.2mA/channel static supply current
- 65mA output current
- 120MHz gain flatness to +/- 0.1dB
- 14 pin SOIC

Ordering Information

ZL40122/DCA (tubes) 14 lead SOIC
ZL40122/DCB (tape and reel) 14 lead SOIC
-40°C to +85°C

Applications

- Video switchers/routers
- Video line drivers
- Twisted pair driver/receiver
- Active filters

Description

The ZL40122 is a high speed, quad, current feedback operational amplifier offering high performance at a low cost. The device has a very high output current drive capability of 65mA while requiring only 5.2mA of static supply current. This feature makes the ZL40122 the ideal choice where a high density of high speed devices is required.

The flat gain response to 120MHz, 450MHz small signal bandwidth and 1500V/µs slew rate make the device an excellent solution for video applications such as driving video signals down significant cable lengths.

Other applications which may take advantage of the ZL40122 superior dynamic performance features include low cost high order active filters and twisted pair driver/receivers.

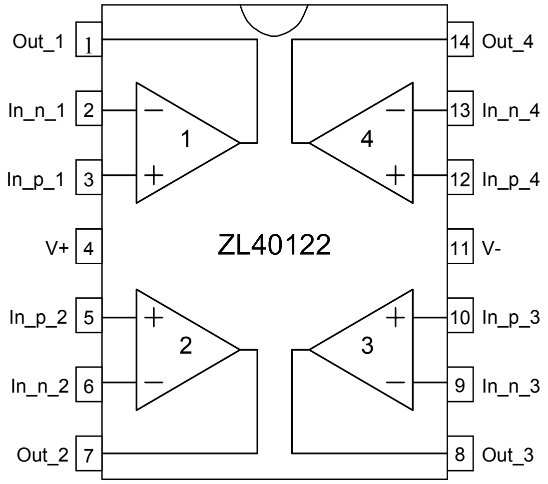


Figure 1 - Functional Block Diagram and Pin Connection

Application Notes

Current Feedback Op Amps

Current feedback op amps offer several advantages over voltage feedback amplifiers:

- AC bandwidth not dependent on closed loop gain
- High Slew Rate
- Fast settling time

The architecture of the current feedback opamp consists of a high impedance non-inverting input and a low impedance inverting input which is always feedback connected. The error current is amplified by a transimpedance amplifier which can be considered to have gain

$$Z(f) = \frac{Z_o}{1 + j\left(\frac{f}{f_o}\right)}$$

where Z_o is the DC gain.

It can be shown that the closed loop non-inverting gain is given by

$$\frac{Vout}{Vin} = \frac{Av}{1 + j\left(\frac{fR_f}{f_o Z_o}\right)}$$

where Av is the DC closed loop gain, R_f is the feedback resistor. The closed loop bandwidth is therefore given by

$$BW_{CL} = \frac{f_o Z_o}{R_f} = \frac{GB_{OL}}{R_f}$$

and for low values of closed loop gain Av depends only on the feedback resistor R_f and not the closed loop gain.

Increasing the value of R_f

- Increases closed loop stability
- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Reduces overshoot

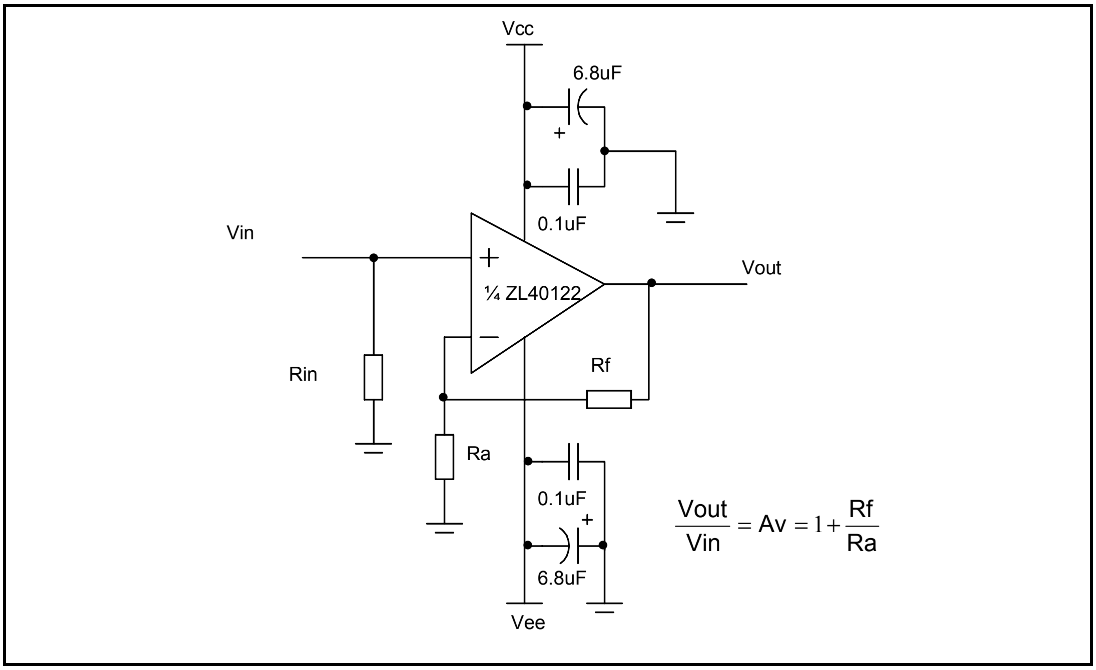
Using a resistor value of R_f=510Ω for Av=+2 V/V gives good stability and bandwidth. However since requirements for stability and bandwidth vary it may be worth experimentation to find the optimal R_f for a given application.

Layout Considerations

Correct high frequency operation requires a considered PCB layout as stray capacitances have a strong influence over high frequency operation for this device. The Zarlink evaluation board serves as a good example layout that should be copied. The following guidelines should be followed:

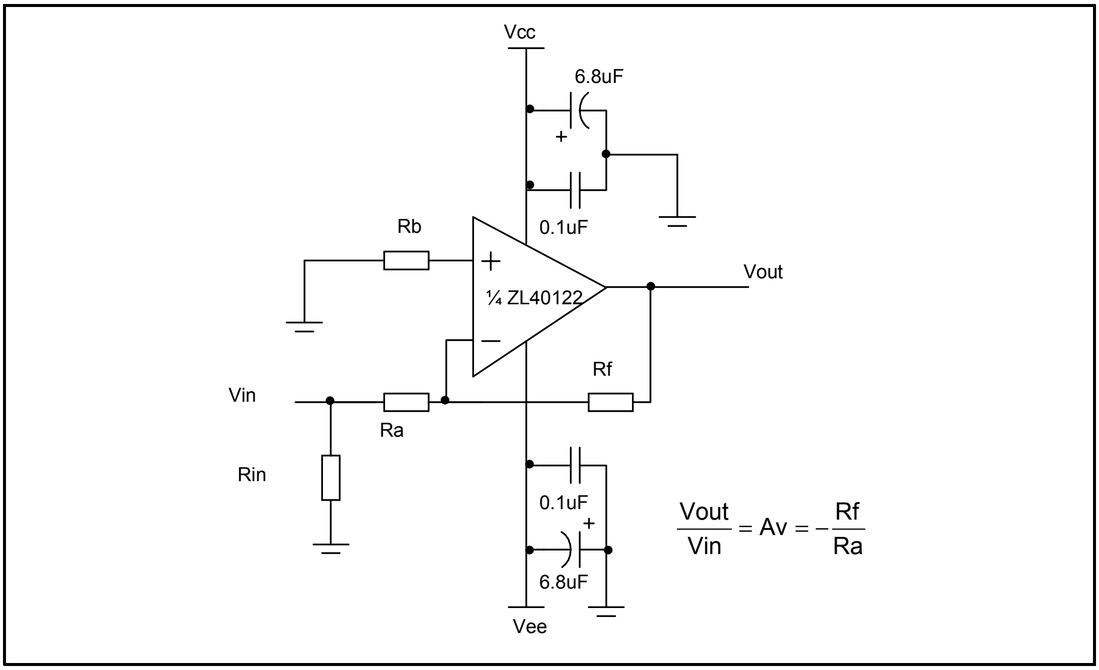
- Include 6.8uF tantalum and 0.1uF ceramic capacitors on both positive and negative supplies
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitances
- Minimize all trace lengths to reduce series inductance

Application Diagrams



$$\frac{Vout}{Vin} = Av = 1 + \frac{Rf}{Ra}$$

Figure 2 - Non-inverting Gain



$$\frac{Vout}{Vin} = Av = -\frac{Rf}{Ra}$$

Figure 3 - Inverting Gain

Absolute Maximum Ratings

	Parameter	Symbol	Min	Max	Units
1	Vin Differential	V_{IN}		±1.2	V
2	Output Short Circuit Protection	$V_{OS/C}$		See Apps Note in this data sheet	
3	Supply voltage	V+, V-		±6.5	V
4	Voltage at Input Pins	$V_{(+IN)}$, $V_{(-IN)}$	V-	V+	V
5	Voltage at Output Pins	V_O	V-	V+	V
6	EDS Protection (HBM Human Body Model) (see Note 2)		2	(see Note 3)	kV
7	Storage Temperature		-55	+150	°C
8	Latch-up test		±100mA for 100ms	(see Note 4)	
9	Supply transient test		20% pulse for 100ms	(see Note 5)	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF. Machine model, 20Ωin series with 100pF.

Note 3: 0.8kV between the pairs of +INA, -INA and +INB pins only. 2kV between supply pins, OUTA or OUTB pins and any input pin.

Note 4: ±100mA applied to input and output pins to force the device to go into "latch-up". The device passes this test to JEDEC spec 17.

Note 5: Positive and Negative supply transient testing increases the supplies by 20% for 100ms.

Operating Range

Characteristic	Min	Typ	Max	Units	Comments
Supply Voltage (Vcc)	±4.0		±6.0	V	
Operating Temperature (Ambient)	-40		+85	°C	
Junction to Ambient resistance	Rth(j-a)	150		°C 4 layer FR4 board	
Junction to Case resistance	Rth(j-c)	60		°C 4 layer FR4 board	

Electrical Characteristics - Vcc=±5V, T_{amb}=25C(typ.),T_{amb}=-40C to +85C(min-max), Av=+2V/V, Rf=510Ω, Rload=100Ω unless specified.

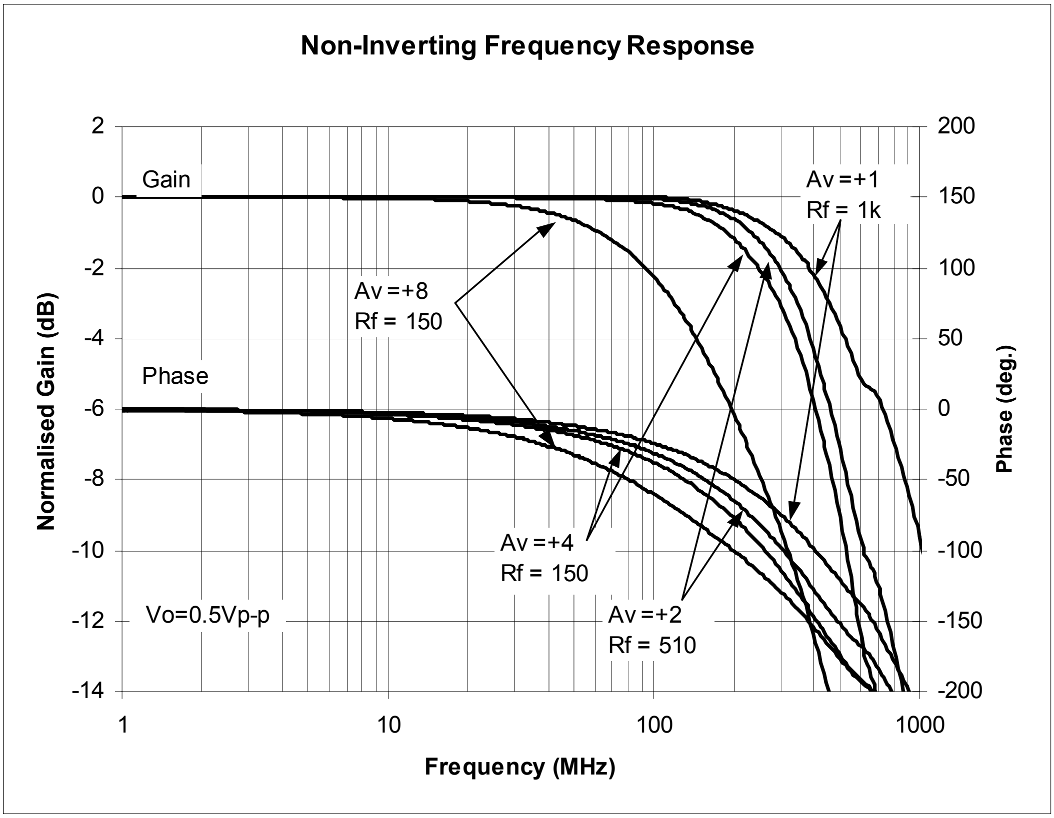
Characteristic	Conditions	Typ 25C	Min/ Max 25C	Min/ Max –40 to +85C	Units	Test Type[1]
Frequency Domain Response						
-3dB Bandwidth	Av=+1; Vo < 0.5Vp-p; Rf=1.5kΩ	450	-	-	MHz	C
	Av=+2; Vo < 0.5Vp-p; Rf=510Ω	380	-	-	MHz	C
	Av=+2; Vo < 5V p-p; Rf=510Ω	170	-	-	MHz	C
+/- 0.1dB Flatness	Av=+2; Vo < 0.5Vp-p; Rf=510Ω	120	-	-	MHz	C
Differential Gain (NTSC)	Rload=150Ω	0.01	-	-	%	C
Differential Phase (NTSC)	Rload=150Ω	0.015	-	-	deg.	C
Time Domain Response						
Rise and Fall Time	Vout=0.5V Step	1	-	-	ns	C
	Vout=5V Step	2.8	-	-	ns	C
Settling Time to 0.1%	Vout=2V Step	6	-	-	ns	C
Overshoot	Vout=0.5V Step	4	-	-	%	C
Slew Rate	Vout=5V Step	1500	-	-	V/µs	C
Noise and Distortion						
2nd Harmonic Distortion	Vout=2Vp-p, 1MHz	-84	-	-	dBc	C
3nd Harmonic Distortion	Vout=2Vp-p, 1MHz	-85	-	-	dBc	C
Equivalent Input Noise						
Voltage	>1MHz	5.5	-	-	nV $\sqrt{Hz}$	C
Non-Inverting Current	>1MHz	1.3	-	-	pV $\sqrt{Hz}$	C
Inverting Current	>1MHz	11	-	-	pA $\sqrt{Hz}$	C
Static, DC Performance						
Input Offset Voltage		2.7	±6.3	±7.7	mV	A
Average Drift		-	-	15	µV/deg. C	C
Input Bias Current – Non-inverting		2.6	±5.6	±6	uA	A
Average Drift		-	-	6	nA/deg. C	C

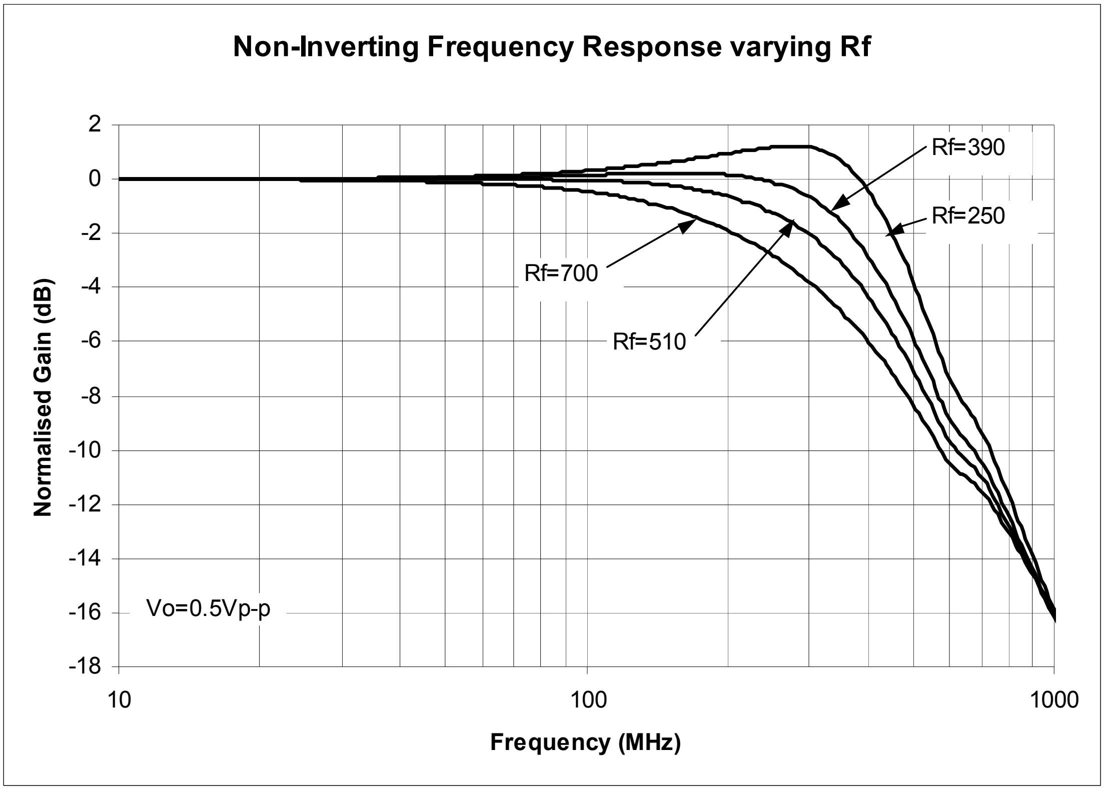
Characteristic	Conditions	Typ 25C	Min/ Max 25C	Min/ Max –40 to +85C	Units	Test Type[1]
Input Bias Current – Inverting		7.4	±25	±28	µA	A
Average Drift		-	-	15	nA/deg. C	C
Power Supply Rejection Ratio (+ve)	DC	61	58	57	dB	A
Power Supply Rejection Ratio (-ve)	DC	58	56	55	dB	A
Common Mode Rejection Ratio	DC	54	50	49	dB	A
Supply Current (per Channel)	Quiescent	5.2	6.5	6.7	mA	A
Miscellaneous Performance						
Input Resistance (Non-inverting)		8	-	-	MΩ	C
Input Capacitance (Non-inverting)		1	-	-	pF	C
Common Mode Input Range		±2.4	±2.2	±2.0	V	A
Output Voltage Range	Rload=100Ω	±2.8	±2.7	±2.6	V	A
Output Current (max)		65	-	-	mA	C
Output Resistance, Closed Loop	DC	90	-	-	mΩ	C

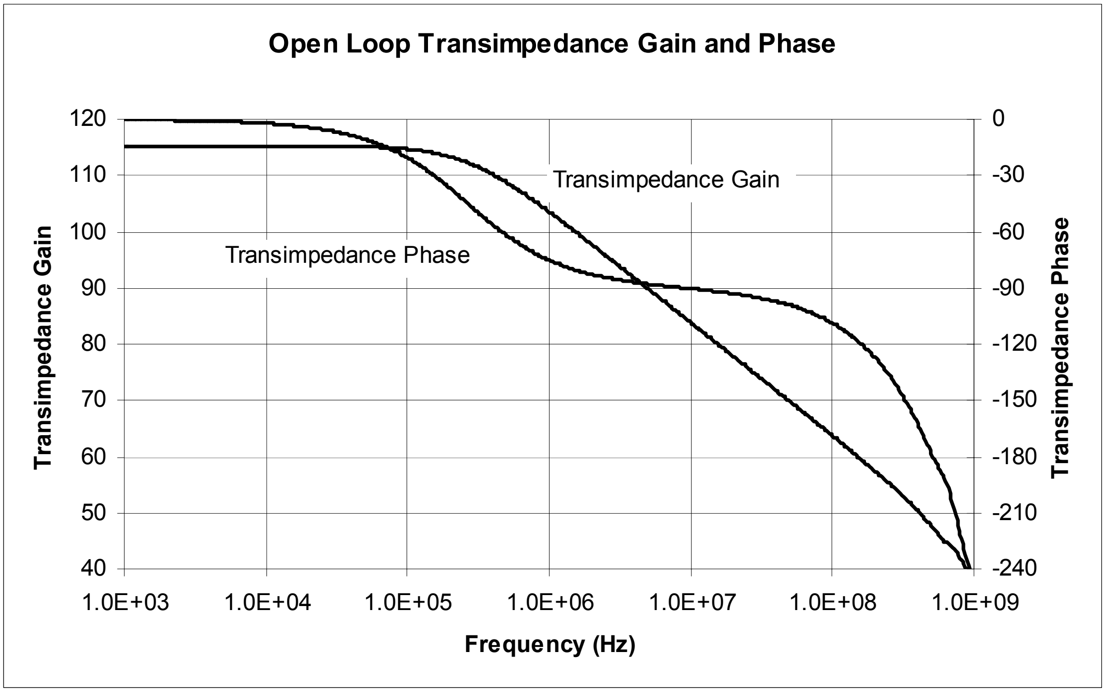
Note: Test Types:

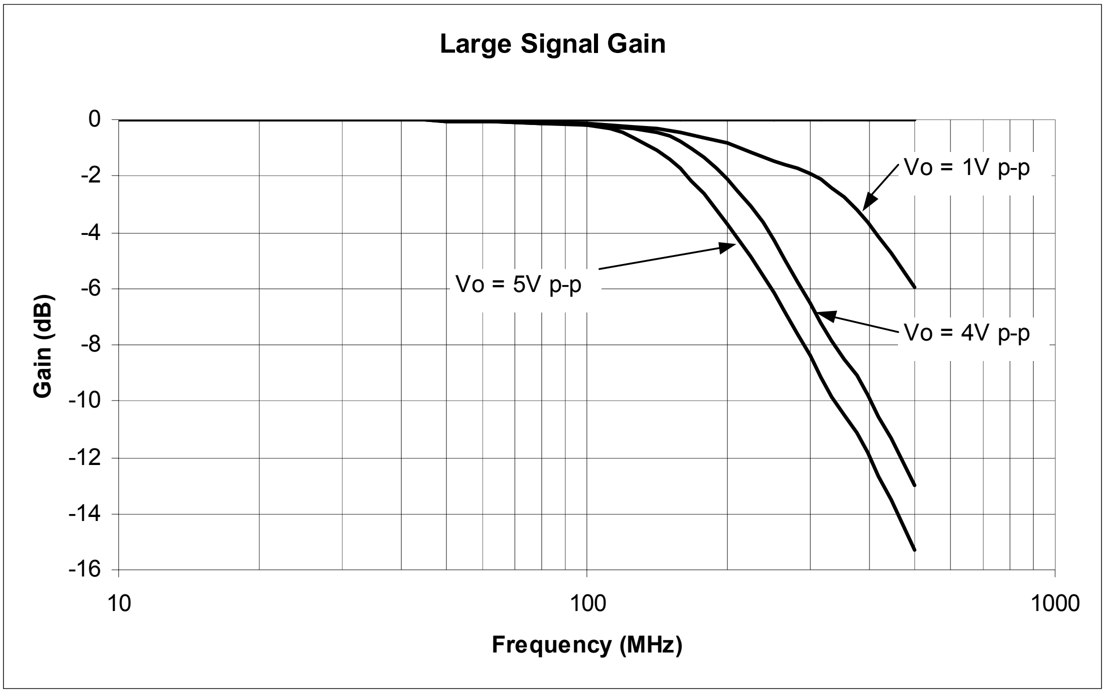
(A) 100% tested at 25°C. Over temperature limits are set by characterization and simulation.
(B) Limits set by characterization or simulation.
(C) Typical value only for information.

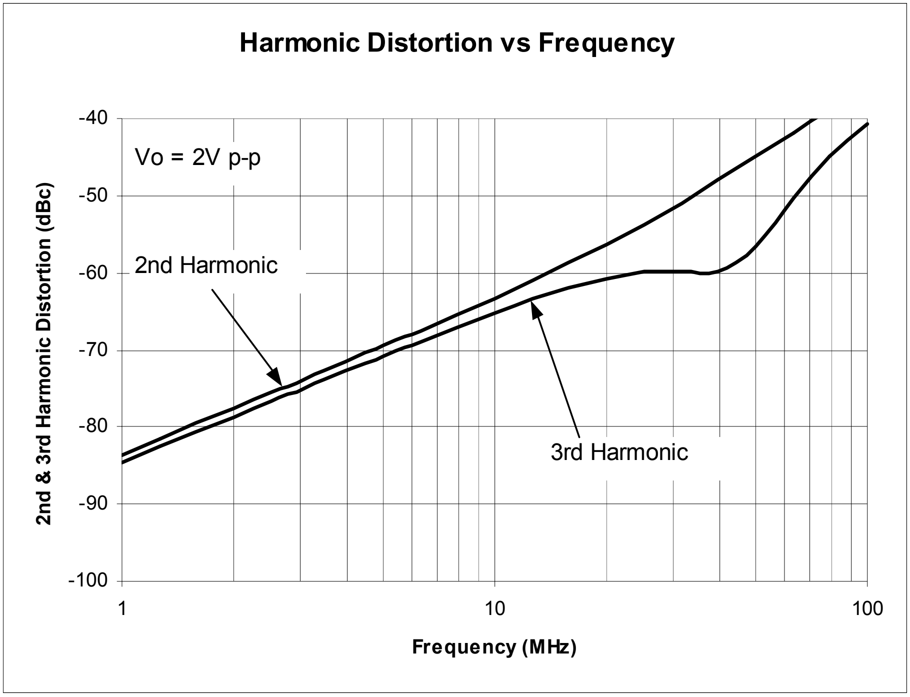
Typical Performance Characteristics - T_{amb}=25degC, V_{supply}=± 5V, Rload=100Ω, Av=+2V/V, Rf=510Ω, unless otherwise specified.

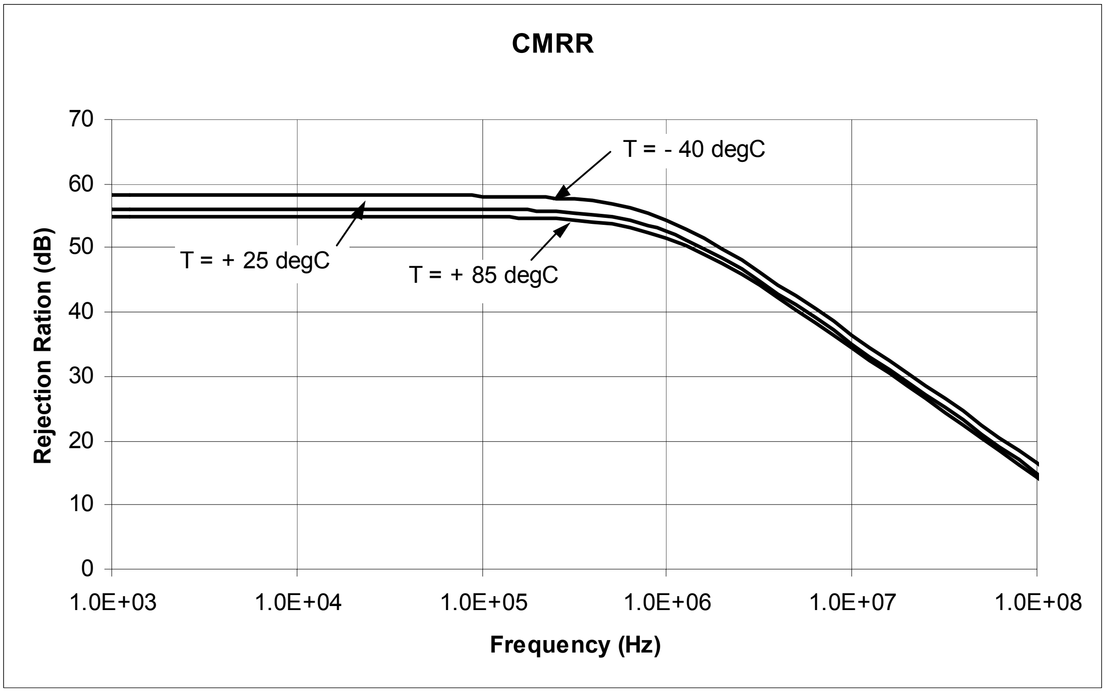


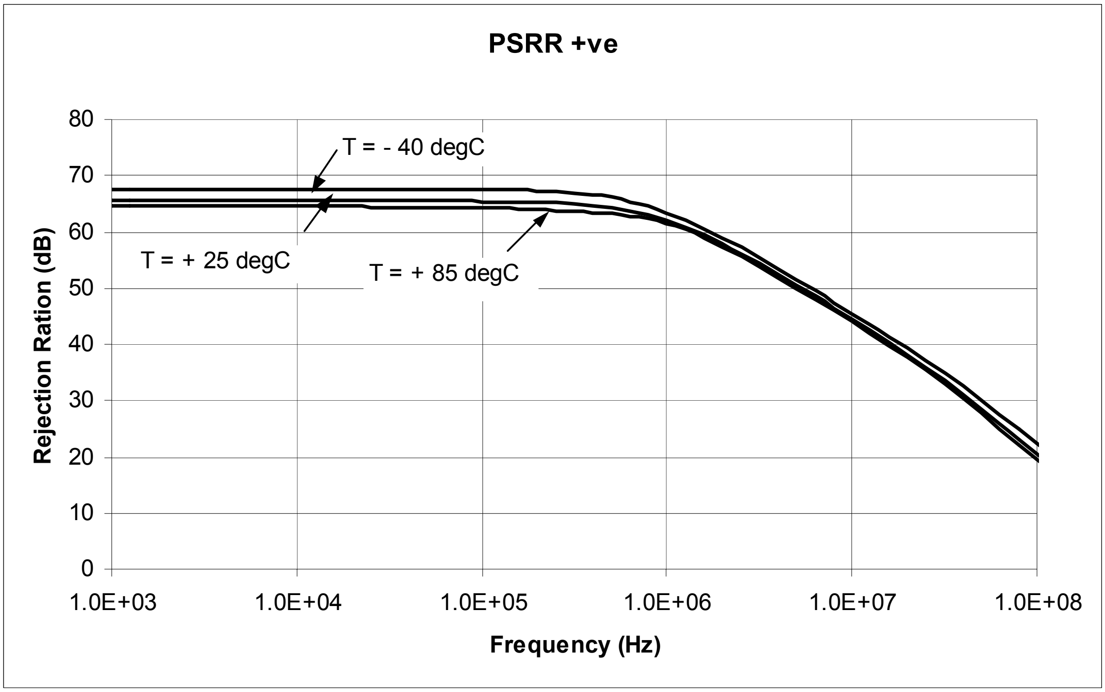

Non-Inverting Frequency Response varying Rf
Normalised Gain (dB)
2
0
-2
-4
-6
-8
-10
-12
-14
-16
-18
10
100
1000
Frequency (MHz)
Rf=390
Rf=250
Rf=700
Rf=510
Vo=0.5Vp-p

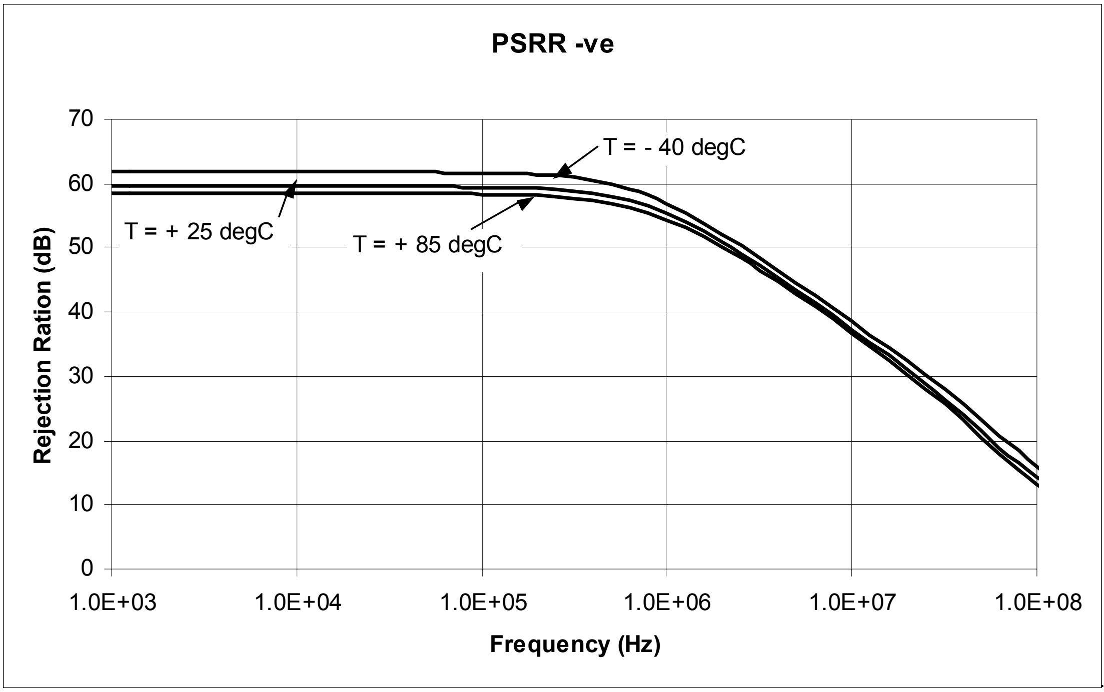

Open Loop Transimpedance Gain and Phase
Transimpedance Gain
120
110
100
90
80
70
60
50
40
Transimpedance Phase
0
-30
-60
-90
-120
-150
-180
-210
-240
1.0E+03
1.0E+04
1.0E+05
1.0E+06
1.0E+07
1.0E+08
1.0E+09
Frequency (Hz)
Transimpedance Gain
Transimpedance Phase

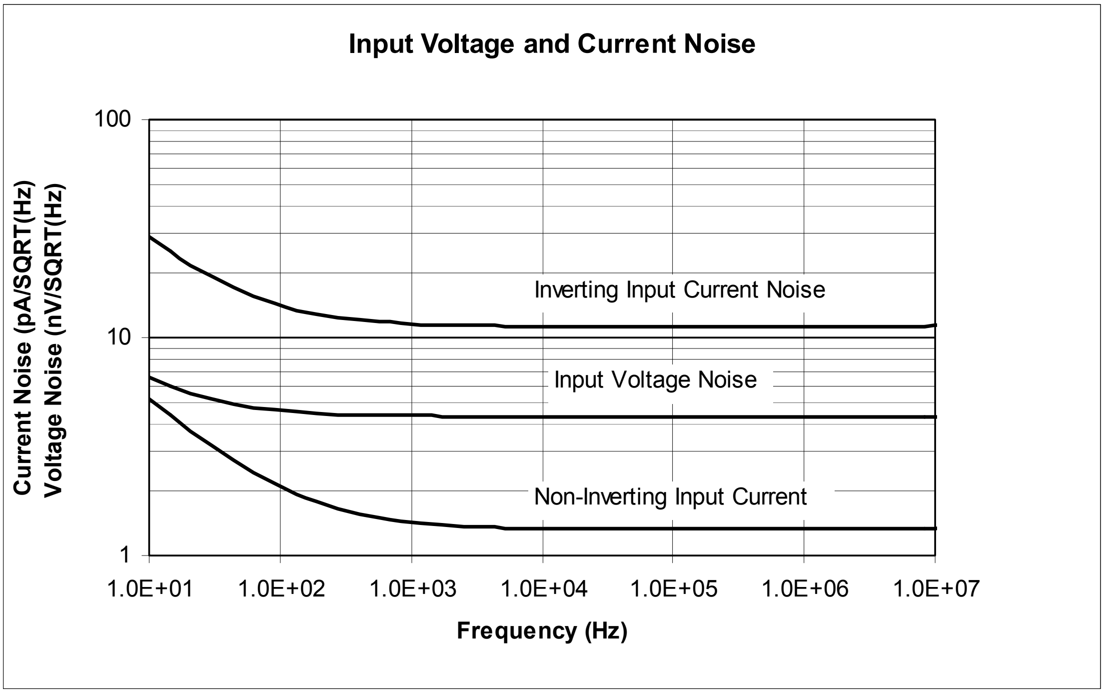

Large Signal Gain
0
-2
-4
-6
-8
-10
-12
-14
-16
Gain (dB)
10
100
1000
Frequency (MHz)
Vo = 1V p-p
Vo = 5V p-p
Vo = 4V p-p

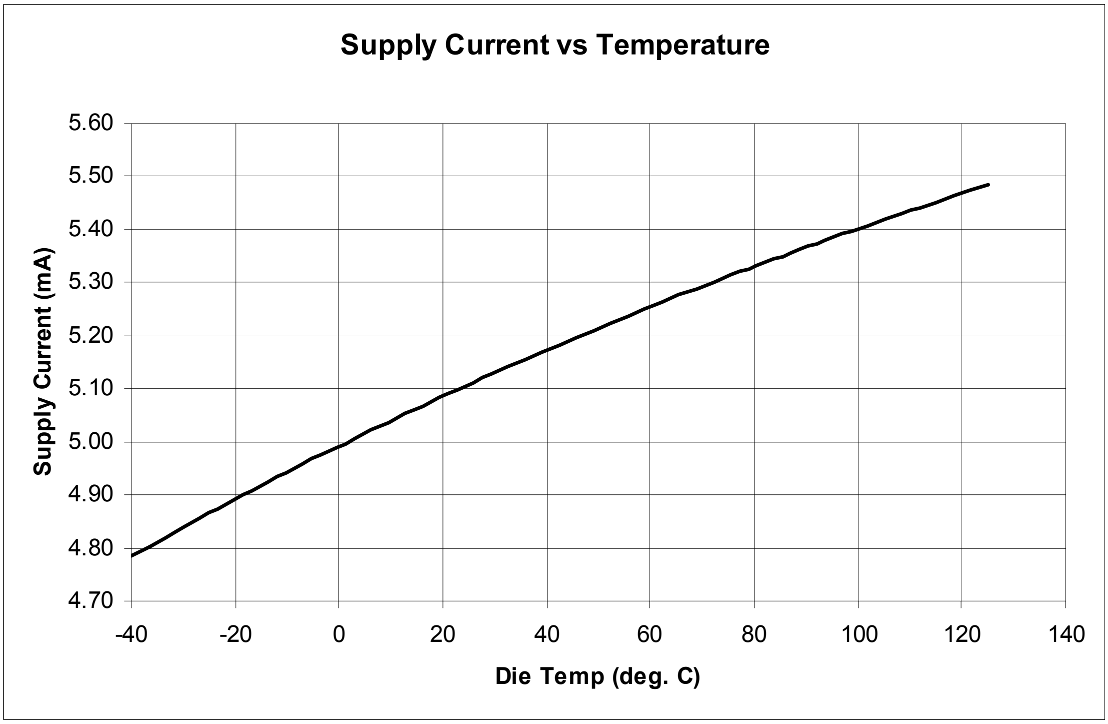

Harmonic Distortion vs Frequency
-40
-50
-60
-70
-80
-90
-100
2nd & 3rd Harmonic Distortion (dBc)
1
10
100
Frequency (MHz)
Vo = 2V p-p
2nd Harmonic
3rd Harmonic

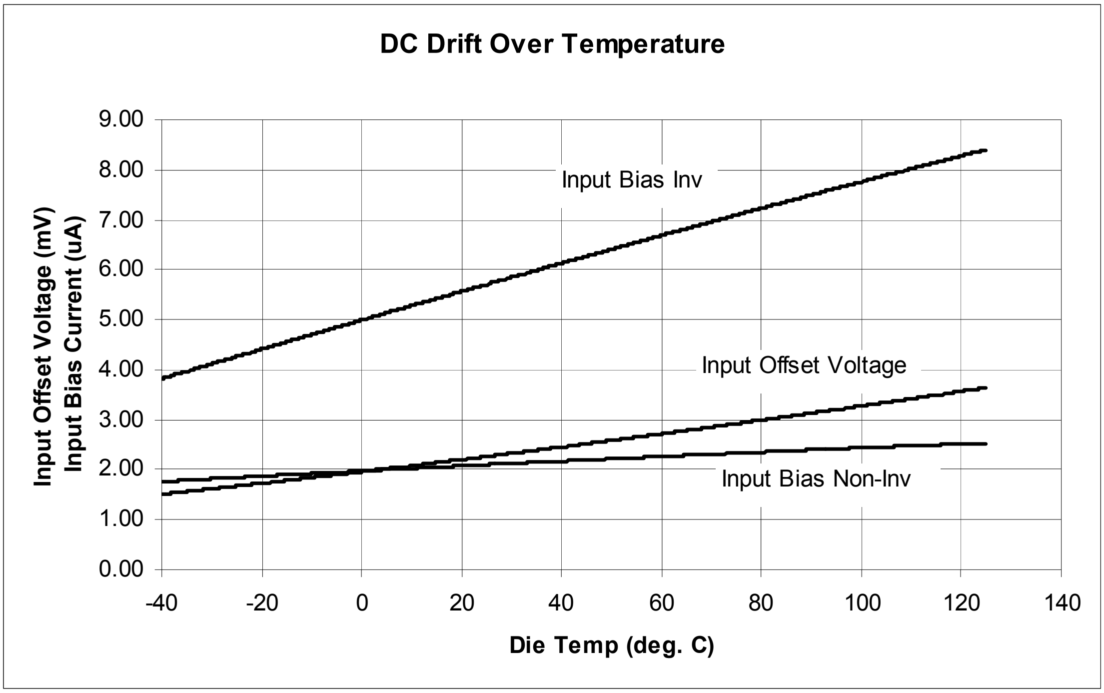

CMRR
Rejection Ration (dB)
0
10
20
30
40
50
60
70
1.0E+03
1.0E+04
1.0E+05
1.0E+06
1.0E+07
1.0E+08
Frequency (Hz)
T = - 40 degC
T = + 25 degC
T = + 85 degC

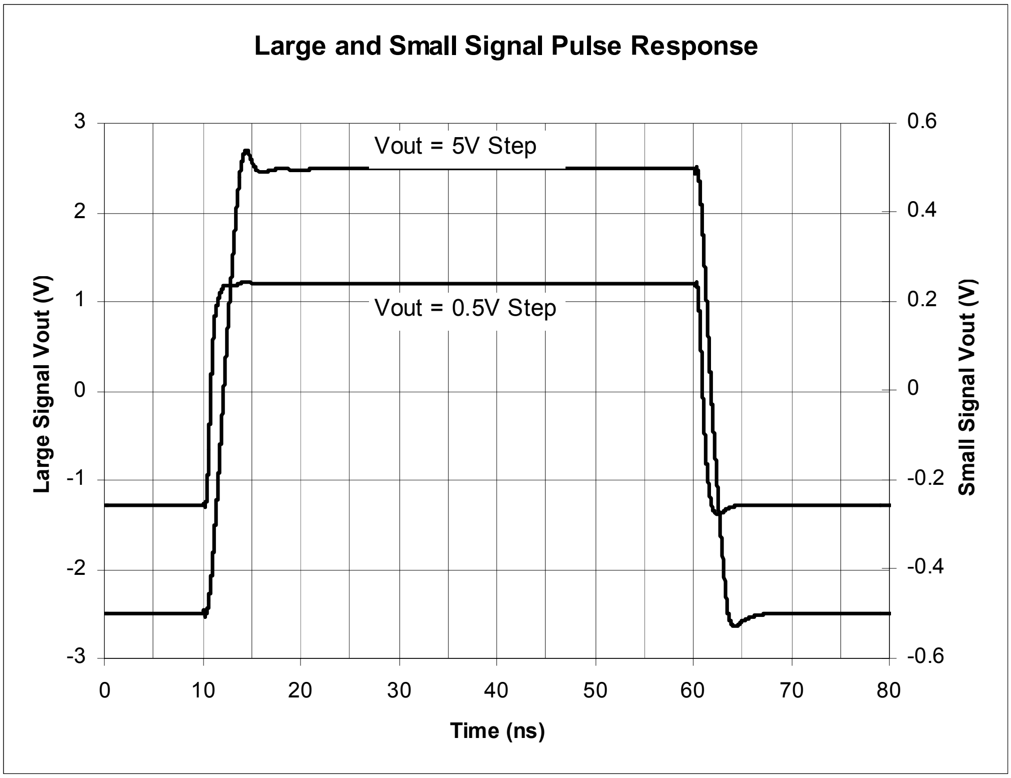

PSRR +ve
Rejection Ration (dB)
0
10
20
30
40
50
60
70
80
1.0E+03
1.0E+04
1.0E+05
1.0E+06
1.0E+07
1.0E+08
Frequency (Hz)
T = - 40 degC
T = + 25 degC
T = + 85 degC

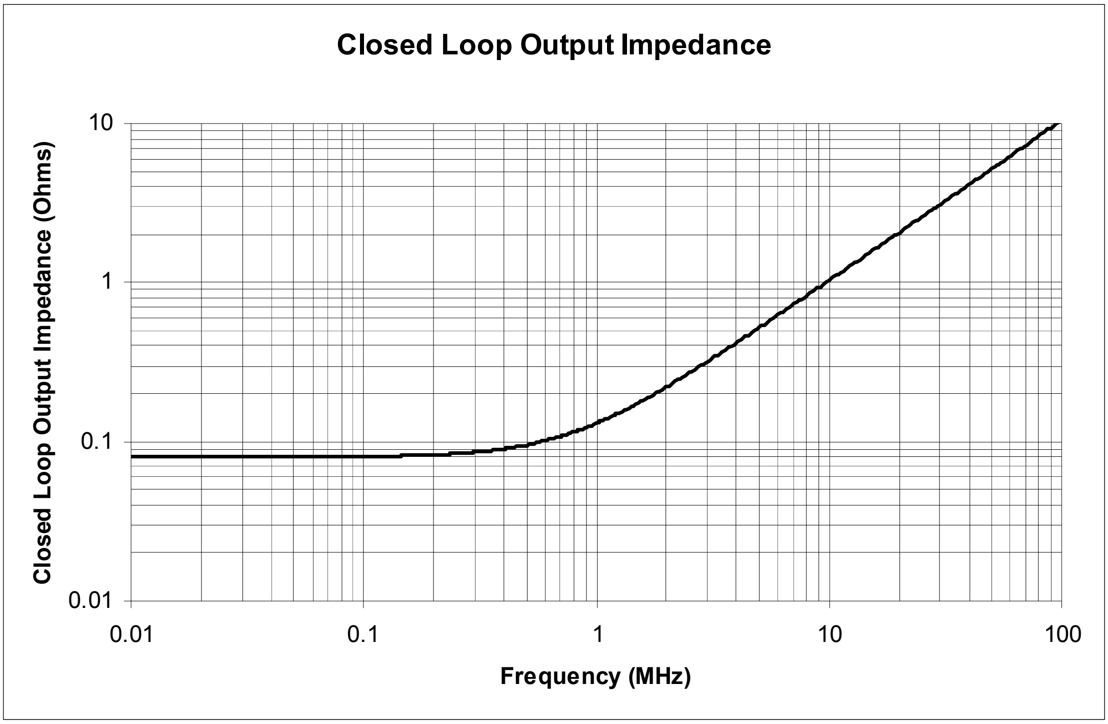

PSRR -ve
Rejection Ration (dB)
70
60
50
40
30
20
10
0
T = - 40 degC
T = + 25 degC
T = + 85 degC
1.0E+03
1.0E+04
1.0E+05
1.0E+06
1.0E+07
1.0E+08
Frequency (Hz)

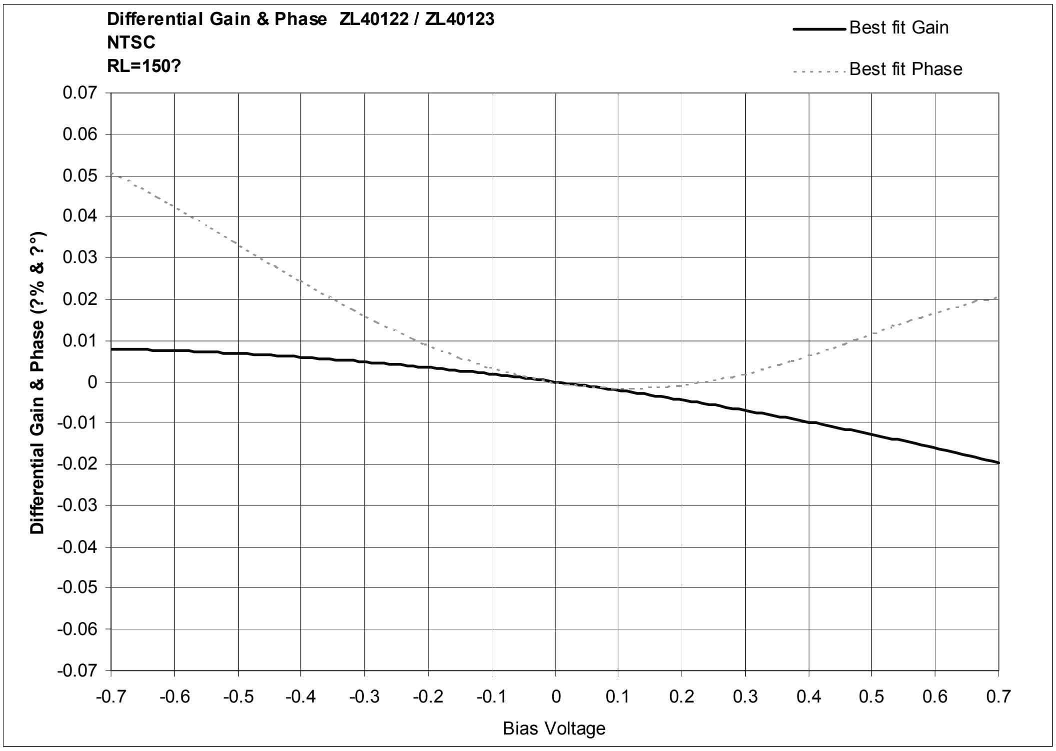

Input Voltage and Current Noise
Current Noise (pA/SQRT(Hz)
Voltage Noise (nV/SQRT(Hz)
100
10
1
Inverting Input Current Noise
Input Voltage Noise
Non-Inverting Input Current
1.0E+01
1.0E+02
1.0E+03
1.0E+04
1.0E+05
1.0E+06
1.0E+07
Frequency (Hz)

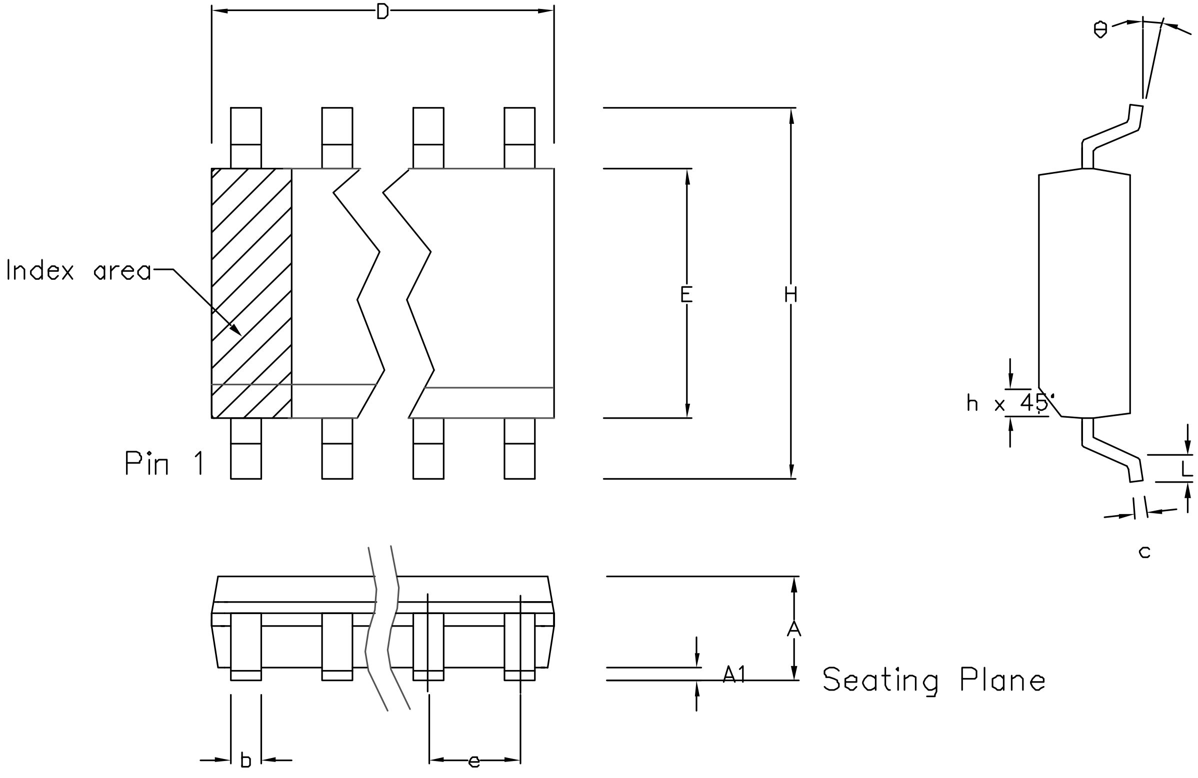

Supply Current vs Temperature
5.60
5.50
5.40
5.30
5.20
5.10
5.00
4.90
4.80
4.70
Supply Current (mA)
-40
-20
0
20
40
60
80
100
120
140
Die Temp (deg. C)


DC Drift Over Temperature
9.00
8.00
7.00
6.00
5.00
4.00
3.00
2.00
1.00
0.00
Input Offset Voltage (mV)
Input Bias Current (uA)
Input Bias Inv
Input Offset Voltage
Input Bias Non-Inv
-40
-20
0
20
40
60
80
100
120
140
Die Temp (deg. C)


Large and Small Signal Pulse Response
Vout = 5V Step
Vout = 0.5V Step
Large Signal Vout (V)
3
2
1
0
-1
-2
-3
Small Signal Vout (V)
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
0
10
20
30
40
50
60
70
80
Time (ns)


Closed Loop Output Impedance
Closed Loop Output Impedance (Ohms)
10
1
0.1
0.01
0.01
0.1
1
10
100
Frequency (MHz)


Differential Gain & Phase ZL40122 / ZL40123
NTSC
RL=150?
Best fit Gain
Best fit Phase
Differential Gain & Phase (?% & ?°)
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0
-0.01
-0.02
-0.03
-0.04
-0.05
-0.06
-0.07
-0.7
-0.6
-0.5
-0.4
-0.3
-0.2
-0.1
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
Bias Voltage



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	8.55	8.75	0.337	0.344
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
O	0º	8º	0º	8º
h	0.25	0.50	0.010	0.020
	Pin Features			
N	14		14	
Conforms to JEDEC MS-012AB Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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APPRD.					

ZARLINK
SEMICONDUCTOR

Previous package codes
MP / S

Package Code DC

Package Outline for
14 lead SOIC
(0.150" Body Width)

GPD00011

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