1.0 Key Features

LIN-Bus Transceiver
- LIN compliant to specification rev. 1.3 and rev. 2.0
- I^2T high voltage technology
- Bus voltage ± 40V
- Transmission rate up to 20 kBaud
- SOIC-150-8 Package

Protection
- Thermal shutdown
- Indefinite short circuit protection to supply and ground
- Load dump protection (45V)

Power Saving
- Operating voltage = 4.75 to 5.25V
- Power down supply current < 50µA

EMS Compatibility
- Integrated filter and hysteresis for receiver

EMI Compatibility
- Integrated slope control for transmitter
- Slope control dependant from Vbat to enable maximum capacitive-load

2.0 General Description

The single-wire transceiver AMIS-30600 is a monolithic integrated circuit in a SOIC-8 package. It works as an interface between the protocol controller and the physical bus.

The AMIS-30600 is especially suitable to drive the bus line in LIN systems in automotive and industrial applications. Further it can be used in standard ISO9141 systems.

In order to reduce the current consumption the AMIS-30600 offers a stand-by mode. A wake-up caused by a message on the bus pulls the INH-output high until the device is switched to normal operation mode.

The transceiver is implemented in I^2T100 technology enabling both high-voltage analog circuitry and digital functionality to co-exist on the same chip.

The AMIS-30600 provides an ultra-safe solution to today's automotive in-vehicle networking (IVN) requirements by providing unlimited short circuit protection in the event of a fault condition.

3.0 Ordering Information

Table 1: Ordering Code

Marketing Name	Package	Temp. Range
AMIS30600AGA	SOIC 150 8 150 4	-40°C…125°C

4.0 Block Diagram

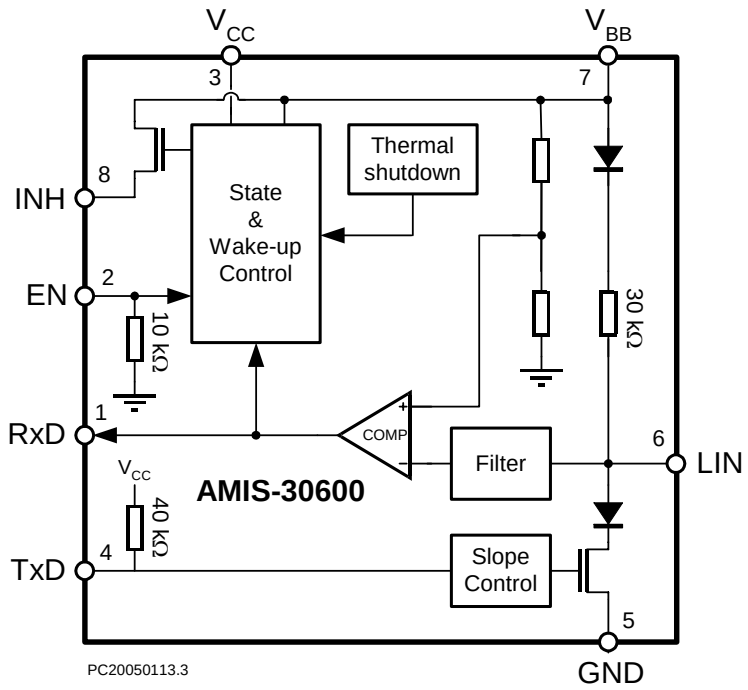


Figure 1: Block Diagram

5.0 Typical Application

5.1 Application Schematic

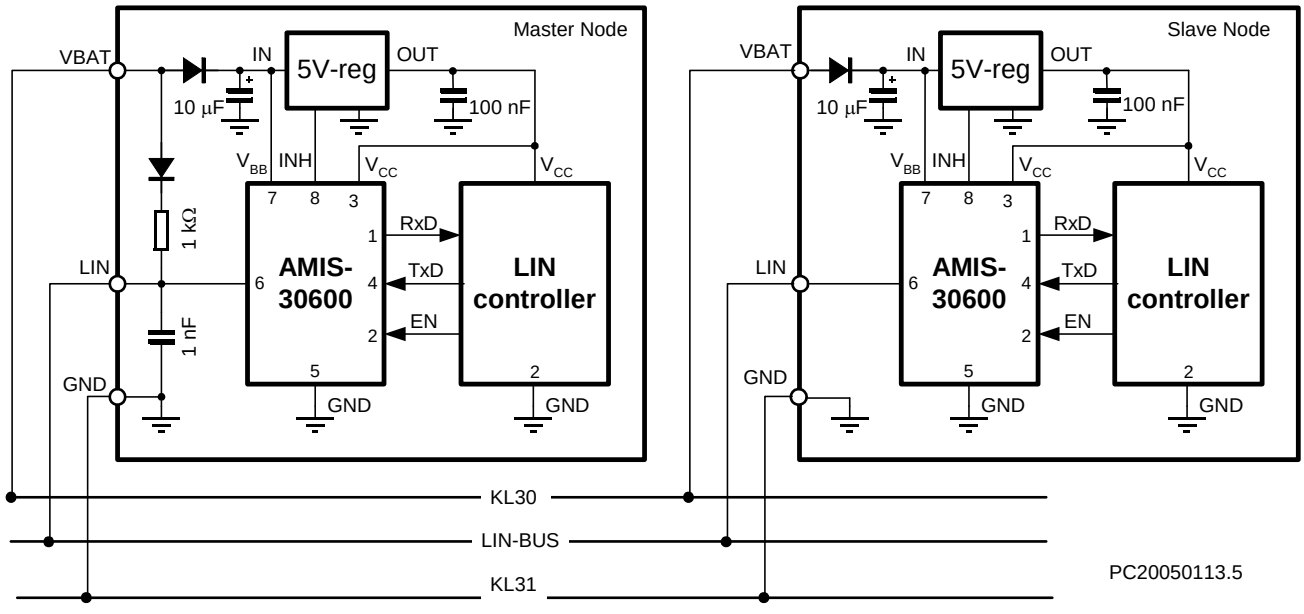


Figure 2: Application Diagram

5.2 Pin Description

5.2.1 Pin Out (top view)

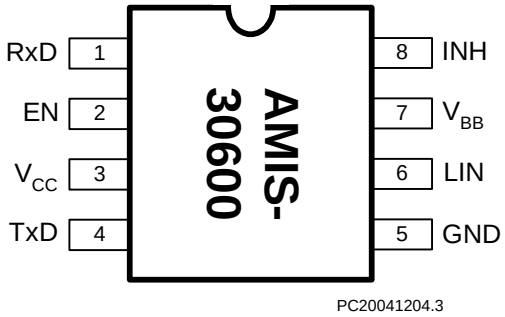


Figure 3: Pin Configuration

5.2.2 Pin Description

Table 2: Pinout

Pin	Name	Description
1	RxD	Receive data output; low in dominant state
2	EN	Enable input; transceiver in normal operation mode when high
3	VCC	5V supply input
4	TxD	Transmit data input; low in dominant state; internal 40 KΩ pull-up
5	GND	Ground
6	LIN	LIN bus output/input; low in dominant state; internal 30 KΩ pull-up
7	VBB	Battery supply input
8	INH	Inhibit output; to control a voltage regulator; becomes high when wake-up via LIN bus occurs

5.3 Application Information

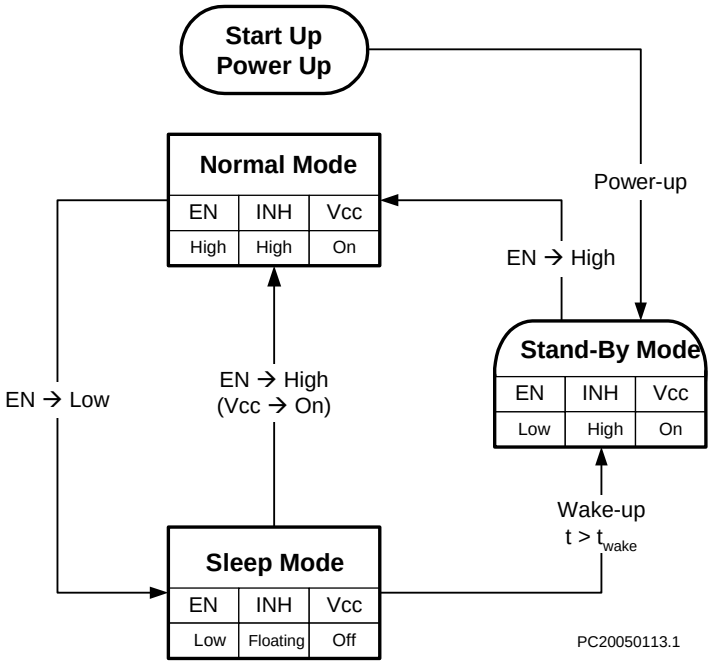


Figure 4: State Diagram

For fail safe reasons the AMIS-30600 already has an internal pull up resistor of 30kΩ implemented. To achieve the required timings for the dominant to recessive transition of the bus signal an additional external termination resistor of 1kΩ is required. It is recommended to place this resistor in the master node. To avoid reverse currents from the bus line into the battery supply line in case of an unpowered node, it is recommended to place a diode in series to the external pull up. For small systems (low bus capacitance) the EMC performance of the system is supported by an additional capacitor of at least 1nF in the master node (see Figure 2, Typical Application Diagram).

The AMIS-30600 has a slope which depends of the supply Vbat. This implementation guarantees biggest slope-time under all load conditions. The rising slope has to be slower then the external RC-time-constant, otherwise the slope will be terminated by the RC-time-constant and no longer by the internal slope-control. This would effect the symmetry of the bus-signal and would limit the maximum allowed bus-speed.

A capacitor of 10µF at the supply voltage input VB buffers the input voltage. In combination with the required reverse polarity diode this prevents the device from detecting power down conditions in case of negative transients on the supply line.

In order to reduce the current consumption, the AMIS-30600 offers a sleep operation mode. This mode is selected by switching the enable input EN low (see Figure 4, State Diagram).

In the sleep mode a voltage regulator can be controlled via the INH output in order to minimize the current consumption of the whole application. A wake-up caused by a message on the communication bus automatically enables the voltage regulator by switching the INH output high. In case the voltage regulator control input is not connected to INH output or the micro-controller is active respectively, the AMIS-30600 can be set in normal operation mode without a wake-up via the communication bus.

6.0 Electrical Characteristics

6.1 Absolute Maximum Ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage		-0.3	+7	V
V_{BB}	Battery supply voltage		-0.3	+40	V
V_{LIN}	DC voltage at pin LIN	$0 < V_{CC} < 5.50V$; note 1	-40	+40	V
V_{INH}	DC voltage at pin INH	$0 < V_{CC} < 5.50V$	-0.3	V_{BB} + 0.3	V
V_{TxD}	DC voltage at pin TxD	$0 < V_{CC} < 5.50V$	-0.3	V_{CC} + 0.3	V
V_{RxD}	DC voltage at pin RxD	$0 < V_{CC} < 5.50V$	-0.3	V_{CC} + 0.3	V
V_{EN}	DC voltage at pin EN	$0 < V_{CC} < 5.50V$	-0.3	V_{CC} + 0.3	V
$V_{esd(LIN)}$	Electrostatic discharge voltage at LIN pin	Note 2	-4	+4	kV
V_{esd}	Electrostatic discharge voltage at all other pins	Note 2	-4	+4	kV
$V_{tran(LIN)}$	Transient voltage at pin LIN	Note 3	-150	+150	V
$V_{tran(VBB)}$	Transient voltage at pin VBB	Note 4	-150	+150	V
T_{amb}	Ambient temperature		-40	+150	°C

Notes:
1. 80V version available, contact sales for details.
2. Standardized human body model system ESD pulses in accordance to IEC 1000.4.2.
3. Applied transient waveforms in accordance with “ISO 7637 parts 1 & 3” capacitive coupled test pulses 1 (-100V), 2 (+100V), 3a (-150V), and 3b (+150V). See Figure 8.
4. Applied transient waveforms in accordance with “ISO 7637 parts 1 & 3” direct coupled test pulses 1 (-100V), 2 (+75V), 3a (-150V), 3b (+150V), and 5 (+80V). See Figure 8.

6.2 Operating Range

Table 5: Operating Range

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	4.75		+5.25	V
V_{BB}	Battery supply voltage	7.3		+18	V
T_{junc}	Maximum junction temperature	-40		+150	°C
T_{jsd}	Thermal shutdown temperature	+150	+170	+190	°C
R_{thj-a}	Thermal resistance junction to ambient		185		°C/W

6.3 DC Electrical Characteristics

V_{CC} = 4.75 to 5.25V; V_{BB} = 7.3 to 18V; $V_{EN} > V_{EN,on}$; T_{amb} = -40 to +125°C; R_L = 500Ω unless specified otherwise. All voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Table 6: DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply (pin VCC and pin VBB)						
I_{CC}	5V supply current	Dominant; V_{TxD} =0V Recessive; V_{TxD} =V_{CC}		400 250	700 500	µA µA
I_{BB}	Battery supply current	Dominant; V_{TxD} =0V Recessive; V_{TxD} =V_{CC}		1 100	1.5 200	mA µA
I_{BB}	Battery supply current	Sleep mode; V_{INH} = 0V		35	55	µA
I_{CC}	5V supply current	Sleep mode; V_{INH} = 0V		0.25	1	µA
Transmitter Data Input (pin TxD)						
V_{IH}	High-level input voltage	Output recessive	0.7 x V_{CC}	-	V_{CC}	V
V_{IL}	Low-level input voltage	Output dominant	0	-	0.3 x V_{CC}	V
$R_{TxD,pu}$	Pull-up resistor to Vcc		24		60	kΩ
Receiver Data Output (pin RxD)						
V_{OH}	High-level output voltage	I_{RXD} = -10mA	0.8 x V_{CC}		V_{CC}	V
V_{OL}	Low-level output voltage	I_{RXD} = 5mA	0		0.2 x V_{CC}	V
Enable Input (pin EN)						
$V_{EN,on}$	High-level input voltage	Normal mode	0.7 x V_{CC}	-	V_{CC}	V
$V_{EN,off}$	Low-level input voltage	Low power mode	0	-	0.3 x V_{CC}	V
$R_{EN,pd}$	Pull-down resistor to GND		6	10	15	kΩ
Inhibit Output (pin INH)						
$V_{INH,d}$	High-level voltage drop: $V_{INH,d}$ = V_{BB} - V_{INH}	I_{INH} = - 0.15mA		0.5	1.0	V
$I_{INH,lk}$	Leakage current	Sleep mode; V_{INH} = 0V	-5.0	-	5.0	µA
Bus Line (pin LIN)						
$V_{bus,rec}$	Recessive bus voltage at pin LIN	V_{TxD} =V_{CC}	0.9 x V_{BB}	-	V_{BB}	V
$V_{bus,dom}$	Dominant output voltage at pin LIN	V_{TxD} = 0V V_{TxD} = 0V; I_{bus} = 40mA	0	-	0.15 x V_{BB} 1.4	V V
$I_{bus,sc}$	Bus short circuit current	$V_{bus,short}$ = 18V	40	85	130	mA
$I_{bus,lk}$	Bus leakage current	V_{CC}=V_{BB}=0V; V_{bus}=8V V_{CC}=V_{BB}=0V; V_{bus}=20V	-400	-200 5	 20	µA
R_{bus}	Bus pull-up resistance	V_{TxD} = 0V	20	30	47	kΩ
$V_{bus,rd}$	Receiver threshold: recessive to dominant		0.4 x V_{BB}	0.48 x V_{BB}	0.6 x V_{BB}	V
$V_{bus,dr}$	Receiver threshold: dominant to recessive		0.4 x V_{BB}	0.52 x V_{BB}	0.6 x V_{BB}	V
Vq	Receiver hysteresis	$V_{bus,hys}$=$V_{bus,rec}$-$V_{bus,dom}$	0.05 x V_{BB}	0.04 x V_{BB}	0.175 x V_{BB}	V
V_{WAKE}	Wake-up threshold voltage		0.4 x V_{BB}		0.6 x V_{BB}	V

6.4 AC Electrical Characteristics

V_{CC} = 4.75 to 5.25V; V_{BB} = 7.3 to 18V; V_{EN} > $V_{EN,on}$; T_{amb} = -40 to +125°C; R_L = 500Ω unless specified otherwise.
Load for slope definitions (typical loads) = [L1] 1nF 1kΩ / [L2] 6.8nF 600Ω / [L3] 10nF 500Ω.

Table 7: AC Characteristics According to LIN V1.3

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dynamic Transceiver Characteristics According to LIN v1.3						
t _slope_F	Slope time falling edge	See Figure 6	4	-	24	µs
t _slope_R	Slope time rising edge	See Figure 6	4	-	24	µs
t _slope _Sym	Slope time symmetry	t _slope_F - t _slope_R	-8	-	+8	µs
T_rec_F	Propagation delay Bus dominant to RxD = low; note 1	See Figure 5, 6		2	6	µs
T_rec_R	Propagation delay Bus recessive to RxD = high; note 1	See Figure 5, 6		2	6	µs
tWAKE	Wake-up delay time		30	100	200	µs

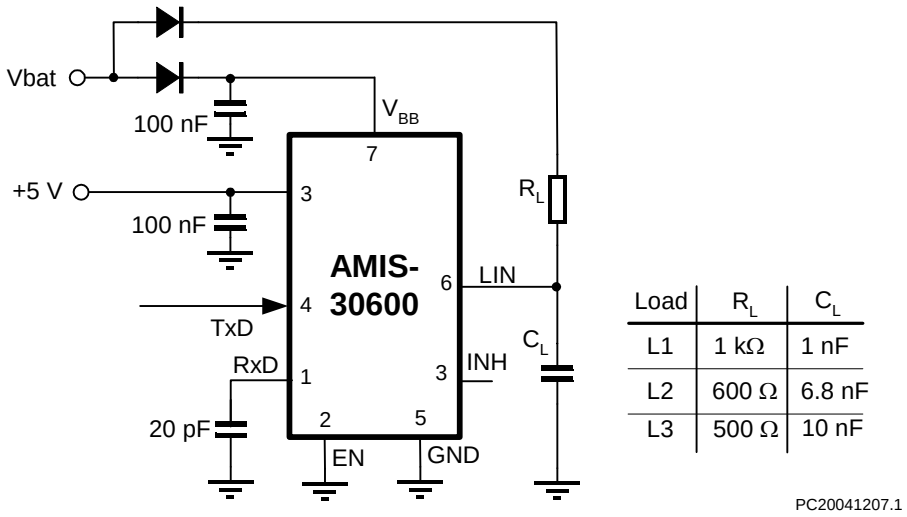
Notes:
1. Not measured on ATE.

V_{CC} = 4.75 to 5.25V; V_{BB} = 7.3 to 18V; V_{EN} > $V_{EN,on}$; T_{amb} = -40 to +125°C; R_L = 500Ω unless specified otherwise.
Load for slope definitions (typical loads) = [L1] 1nF 1kΩ / [L2] 6.8nF 600Ω / [L3] 10nF 500Ω.

Table 8: AC Characteristics According to LIN V2.0

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dynamic Receiver Characteristics according to LIN v2.0						
trx_pdr	Propagation delay bus dominant to RxD = low; note 1	See Figure 7			6	µs
trx_pdf	Propagation delay Bus recessive to RxD = high; note 1	See Figure 7			6	µs
trx_sym	Symmetry of receiver propagation delay	trx_pdr - trx_pdf	-2	-	+2	µs
Dynamic Transmitter Characteristics according to LIN v2.0						
D1	Duty cycle 1 = $t_{Bus\_rec(min)}/(2 \times t_{Bit})$; See Figure 7	THRec(max)= 0.744 x V_{bat}; THDom(max)= 0.581 x V_{bat}; V_{bat} = 7.0V ... 18V; t_{Bit}= 50µs	0.396		0.5	
D1	Duty cycle 1 = $t_{Bus\_rec(min)}/(2 \times t_{Bit})$; See Figure 7	THRec(max)= 0.744 x V_{bat}; THDom(max)= 0.581 x V_{bat}; V_{bat} = 7.0V; t_{Bit}= 50µs; t_{amb} = -40°C	0.366		0.5	
D2	Duty cycle 2 = $t_{Bus\_rec(max)}/(2 \times t_{Bit})$; See Figure 7	THRec(min)= 0.284 x V_{bat}; THDom(min)= 0.422 x V_{bat}; V_{bat} = 7.6V ... 18V; t_{Bit}= 50µs;	0.5		0.581	

Notes:
1. Not measured on ATE.



Load	R_L	C_L
L1	1 kΩ	1 nF
L2	600 Ω	6.8 nF
L3	500 Ω	10 nF

Figure 5: Test Circuit for Timing Characteristics

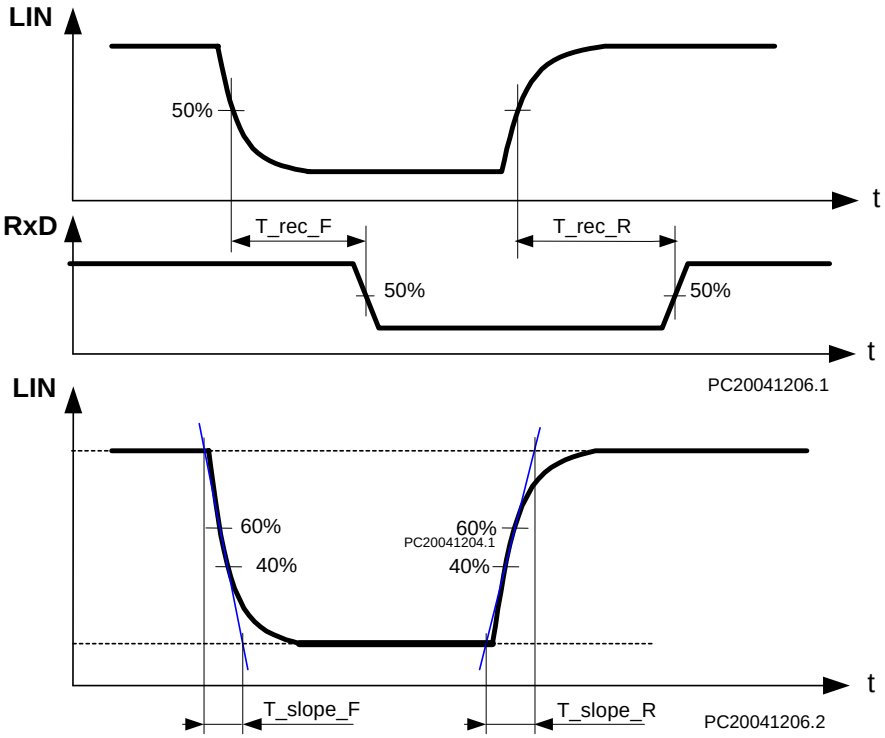


Figure 6: Timing Diagram for AC Characteristics According to LIN 1.3

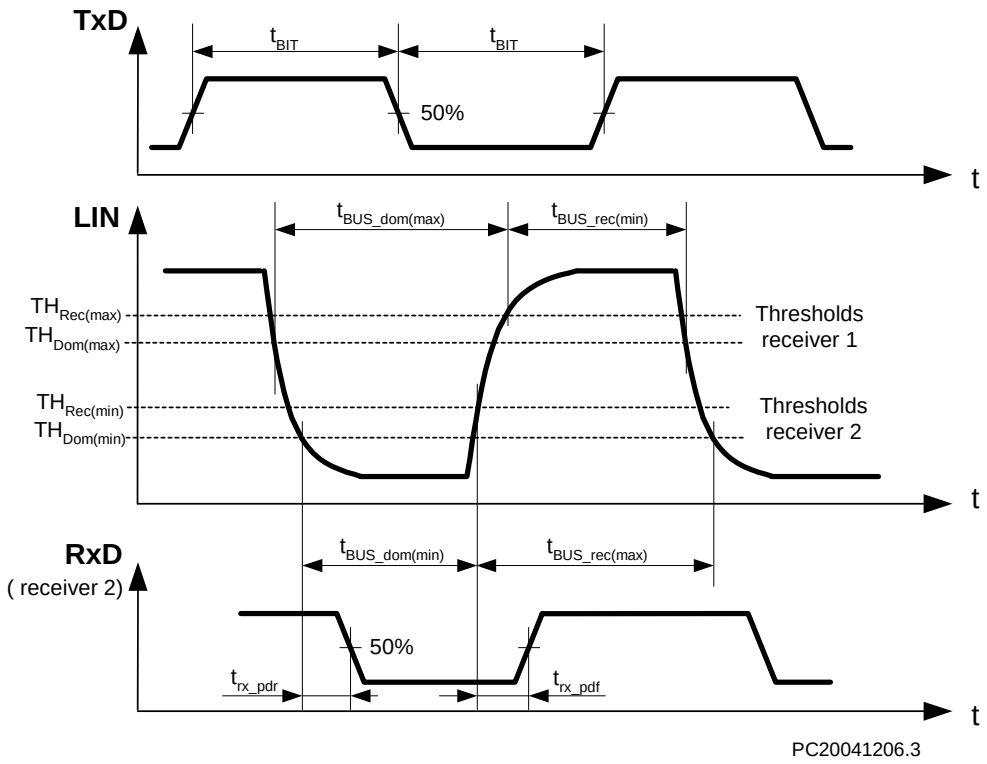


Figure 7: Timing Diagram for AC Characteristics According to LIN 2.0

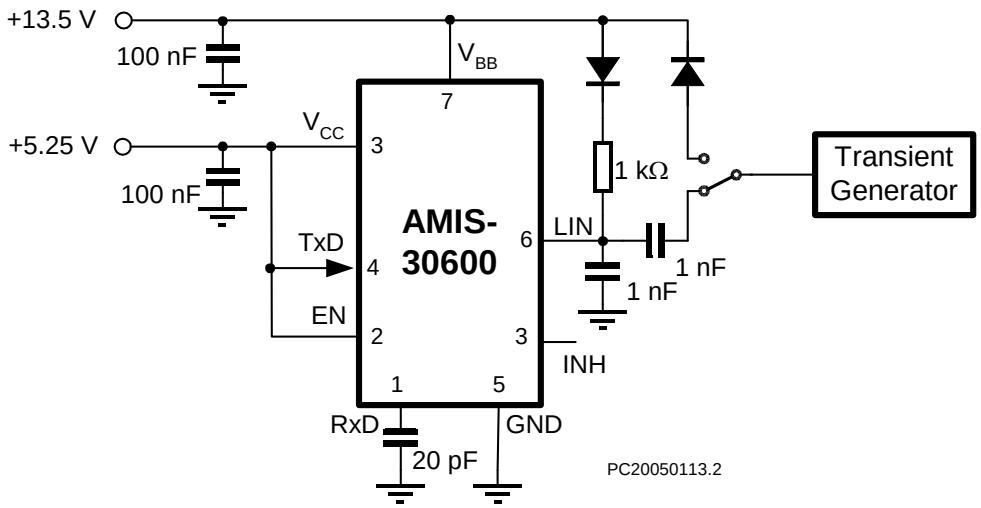
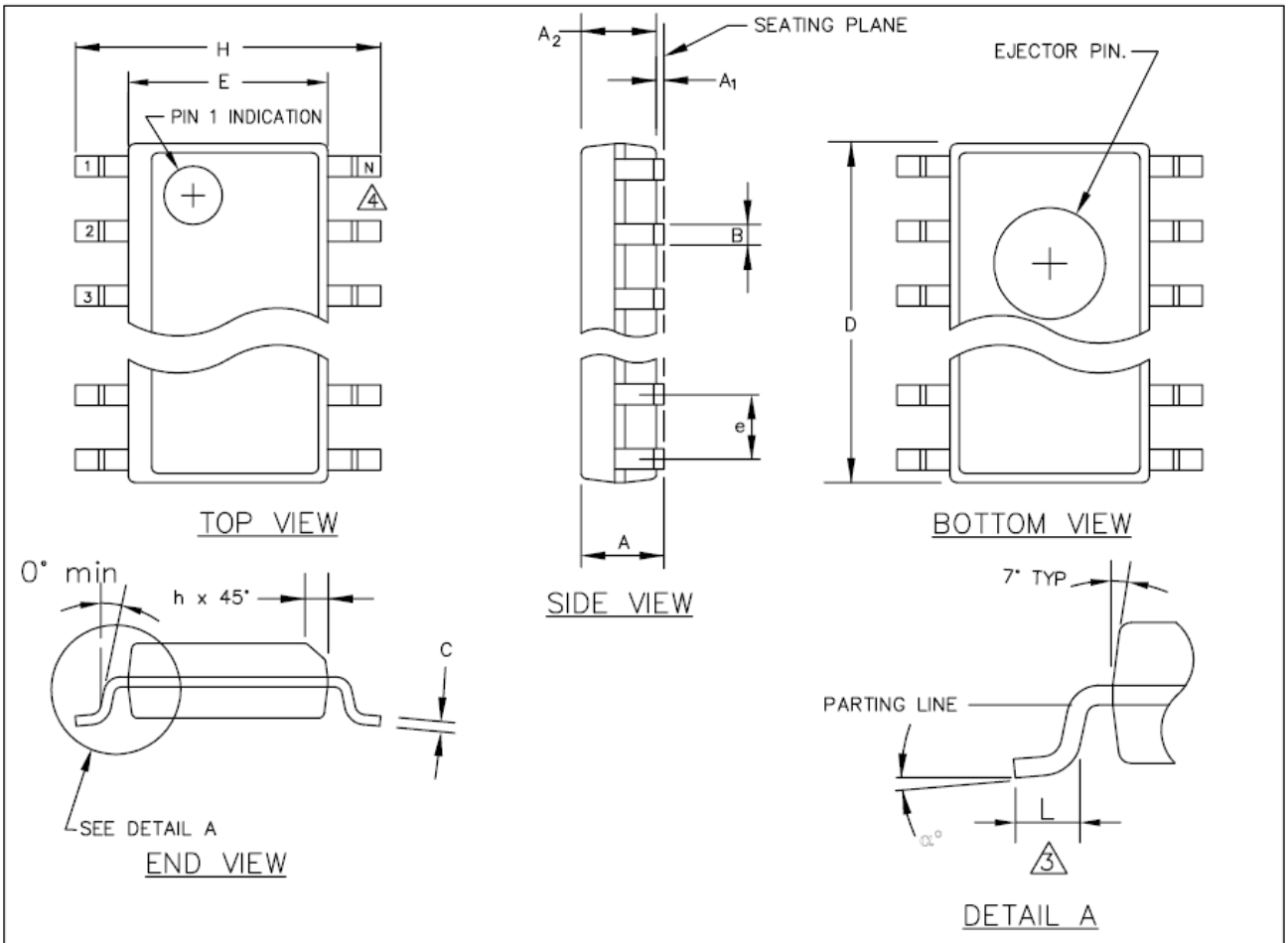


Figure 8: Test Circuit for Transient Measurements

7.0 Package Outline

SOIC-8: Plastic small outline; 8 leads; body width 150 mil; JEDEC: MS-012. AMIS reference: SOIC150 8 150 G



SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	.061	.064	.068	
A_1	.004	.006	0.010	
A_2	.055	.058	.061	
B	.0138	.016	.020	
C	.0075	.008	.0098	
D	SEE VARIATIONS			1
E	.150	.155	.157	
e	.050 BSC			
H	.230	.236	.244	
h	.010	.013	.016	
L	.016	.025	.035	
N	SEE VARIATIONS			2
α°	0°	5°	8°	

VARIATIONS	1 D			2 N
NOTE	MIN.	NOM.	MAX.	
AA	.189	.194	.196	8
AB	.337	.342	.344	14
AC	.386	.391	.393	16

NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M – 1982.
3. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
4. "N" IS THE NUMBER OF TERMINAL POSITIONS.
5. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
6. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
7. CONTROLLING DIMENSION: INCHES.

Drawn:	PJ 10/28/03
CAD Dwg. No.	6000209.DWG
Ref Dwg. No.	
Drawing Number\CAD File	6000209
Rev.	D
Scale:	
Sheet	

SOIC150
8, 14, 16 LEAD

AMI SEMICONDUCTOR, Inc.
2300 Buckskin Rd., Pocatello, Idaho 83201

8.0 Soldering

8.1 Introduction to Soldering Surface Mount Packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in the AMIS "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).
There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

8.2 Re-flow Soldering

Re-flow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven.
Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.
Typical re-flow peak temperatures range from 215 to 250°C. The top-surface temperature of the packages should preferably be kept below 230°C.

8.3 Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems. To overcome these problems the double-wave soldering method was specifically developed.
If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - Larger than or equal to 1.27mm, the footprint longitudinal axis is preferred to be parallel to the transport direction of the printed-circuit board;
  - Smaller than 1.27mm, the footprint longitudinal axis must be parallel to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45º angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.
Typical dwell time is four seconds at 250°C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

8.4 Manual Soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C.
When using a dedicated tool, all other leads can be soldered in one operation within two to five seconds between 270 and 320°C.

Table 9: Soldering Process

Package	Soldering Method	
	Wave	Reflow(1)
BGA, SQFP	Not suitable	Suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	Not suitable (2)	Suitable
PLCC (3) , SO, SOJ	Suitable	Suitable
LQFP, QFP, TQFP	Not recommended (3)(4)	Suitable
SSOP, TSSOP, VSO	Not recommended (5)	Suitable

Notes:
1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods."
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5mm.

9.0 Company or Product Inquiries

For more information about AMI Semiconductor, our technology and our product, visit our website at: http://www.amis.com

North America
Tel: +1.208.233.4690
Fax: +1.208.234.6795

Europe
Tel: +32 (0) 55.33.22.11
Fax: +32 (0) 55.31.81.12