

Power Amplifier Module for JCDMA

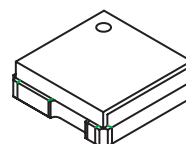
Description

The CXG1178K is the power amplifier module which operates at a single power supply. This IC is designed using the Sony's original p-Gate HFET process.

Features

- Single power supply operation:
 $V_{DD1} = V_{DD2} = 3.5V$ (High mode),
 $1.5V$ (Mid mode),
 $1.0V$ (Low mode),
 $V_{GG} = 2.8V$
- Ultrasmall package: $0.027cc$ ($4.5mm \times 4.5mm \times 1.35mm$)
- High efficiency: $\eta_{add} = 40.5\%$ @ $P_{OUT} = 27.5dBm$ (High mode),
 $\eta_{add} = 17.6\%$ @ $P_{OUT} = 14dBm$ (Mid mode)
- Output power (High/Mid/Low mode switching supported):
 $P_{OUT} = 18$ to $27.5dBm$: High mode,
 $P_{OUT} = 14$ to $18dBm$: Mid mode,
 $P_{OUT} \leq 14dBm$: Low mode
- Gain (High mode): $G_p = 28.5dB$ (@ $900MHz$)

8 pin LCC (Ceramic)



Applications

Power amplifier for JCDMA system cellular phones

Structure

p-Gate HFET module

Absolute Maximum Ratings ($T_a = 25^\circ C$)

• Operating case temperature	T_{case}	-30 to $+110$	$^\circ C$
• Storage temperature	T_{stg}	-30 to $+125$	$^\circ C$
• Bias voltage	V_{DD1}, V_{DD2}	6	V
• Bias voltage	V_{GG}	3.3	V
(@ $V_{DD1} = V_{DD2} \leq 3.5V$)			
• Input power	P_{IN}	8	dBm

Recommended Bias Voltage Conditions

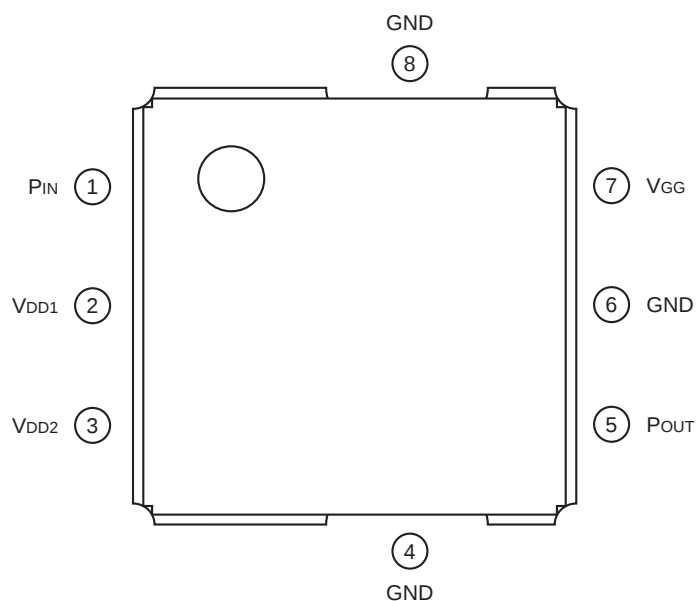
- $V_{DD1} = V_{DD2} = 1.0$ to $4.2V$
- $V_{GG} = 2.8V \pm 1\%$

Descriptions in this specification are specified for the Sony's recommended evaluation board .
GaAs module is ESD sensitive devices. Special handling precautions are required.

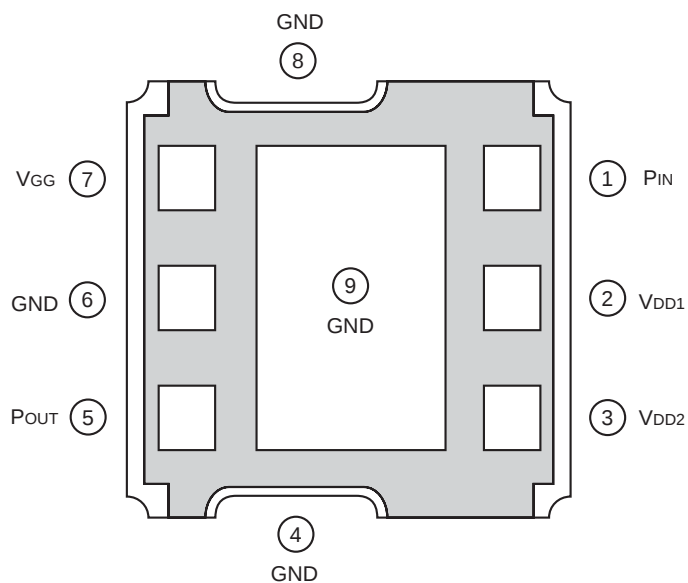
Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Package Outline/Pin Configuration

Front



Back



Note) Pin 4, 8 and 9 should be soldered on the land of the board.

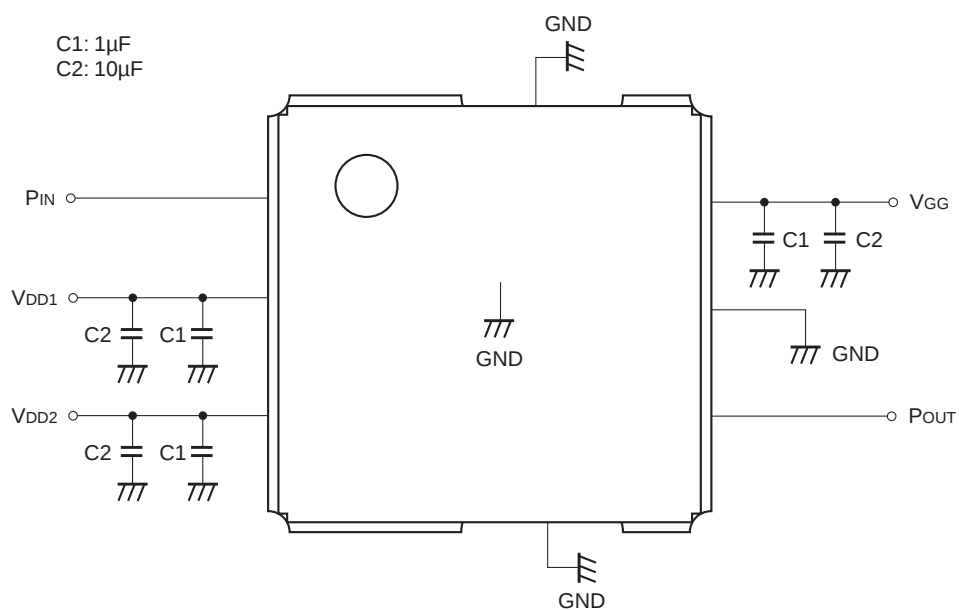
For the land to which Pin 9 is connected, make the through holes in the land and form the GND pattern.

Electrical Characteristics

(ZS = ZL = 50Ω, IS-95 Modulation, Ta = 25°C)

Item	Conditions	Min.	Typ.	Max.	Unit
Frequency		887		925	MHz
Current consumption 1	P _{OUT} = 27.5dBm, V _{DD1} = V _{DD2} = 3.5V, V _{GG} = 2.8V		397	412	mA
Current consumption 2	P _{OUT} = 14dBm, V _{DD1} = V _{DD2} = 1.5V, V _{GG} = 2.8V		95	102	mA
Current consumption 3	P _{OUT} = 9dBm, V _{DD1} = V _{DD2} = 1.0V, V _{GG} = 2.8V		59	66	mA
Gain 1	P _{OUT} = 27.5dBm, V _{DD1} = V _{DD2} = 3.5V, V _{GG} = 2.8V	26.5	28.5		dB
Gain 2	P _{OUT} = 18dBm, V _{DD1} = V _{DD2} = 1.5V, V _{GG} = 2.8V	20.5	22.5		dB
Gain 3	P _{OUT} = 14dBm, V _{DD1} = V _{DD2} = 1.0V, V _{GG} = 2.8V	17.5	19.5		dB
ACPR1 (High mode)	P _{OUT} = 27.5dBm, V _{DD1} = V _{DD2} = 3.5V, V _{GG} = 2.8V, ±900kHz offset, 30kHz band width		−52	−47	dBc
ACPR2 (High mode)	P _{OUT} = 27.5dBm, V _{DD1} = V _{DD2} = 3.5V, V _{GG} = 2.8V, ±1.98MHz offset, 30kHz band width		−62	−57	dBc
ACPR1 (Mid mode)	P _{OUT} = 18dBm, V _{DD1} = V _{DD2} = 1.5V, V _{GG} = 2.8V, ±900kHz offset, 30kHz band width		−55	−47	dBc
ACPR2 (Mid mode)	P _{OUT} = 18dBm, V _{DD1} = V _{DD2} = 1.5V, V _{GG} = 2.8V, ±1.98MHz offset, 30kHz band width		−62	−57	dBc
ACPR1 (Low mode)	P _{OUT} = 14dBm, V _{DD1} = V _{DD2} = 1.0V, V _{GG} = 2.8V, ±900kHz offset, 30kHz band width		−54	−47	dBc
ACPR2 (Low mode)	P _{OUT} = 14dBm, V _{DD1} = V _{DD2} = 1.0V, V _{GG} = 2.8V, ±1.98MHz offset, 30kHz band width		−63	−57	dBc
2nd harmonics	P _{OUT} = 27.5dBm, V _{DD1} = V _{DD2} = 3.5V, V _{GG} = 2.8V		−41	−30	dBc
3rd harmonics	P _{OUT} = 27.5dBm, V _{DD1} = V _{DD2} = 3.5V, V _{GG} = 2.8V		−57	−30	dBc
Gate current	P _{OUT} ≤ 27.5dBm, V _{GG} = 2.8V		1.8	2.5	mA
Idle current 1	P _{IN} , P _{OUT} = None, V _{DD1} = V _{DD2} = 3.5V, V _{GG} = 2.8V		85	110	mA
Idle current 2	P _{IN} , P _{OUT} = None, V _{DD1} = V _{DD2} = 1.5V, V _{GG} = 2.8V		51	66	mA
Idle current 3	P _{IN} , P _{OUT} = None, V _{DD1} = V _{DD2} = 1.0V, V _{GG} = 2.8V		40	52	mA

Recommended External Circuit

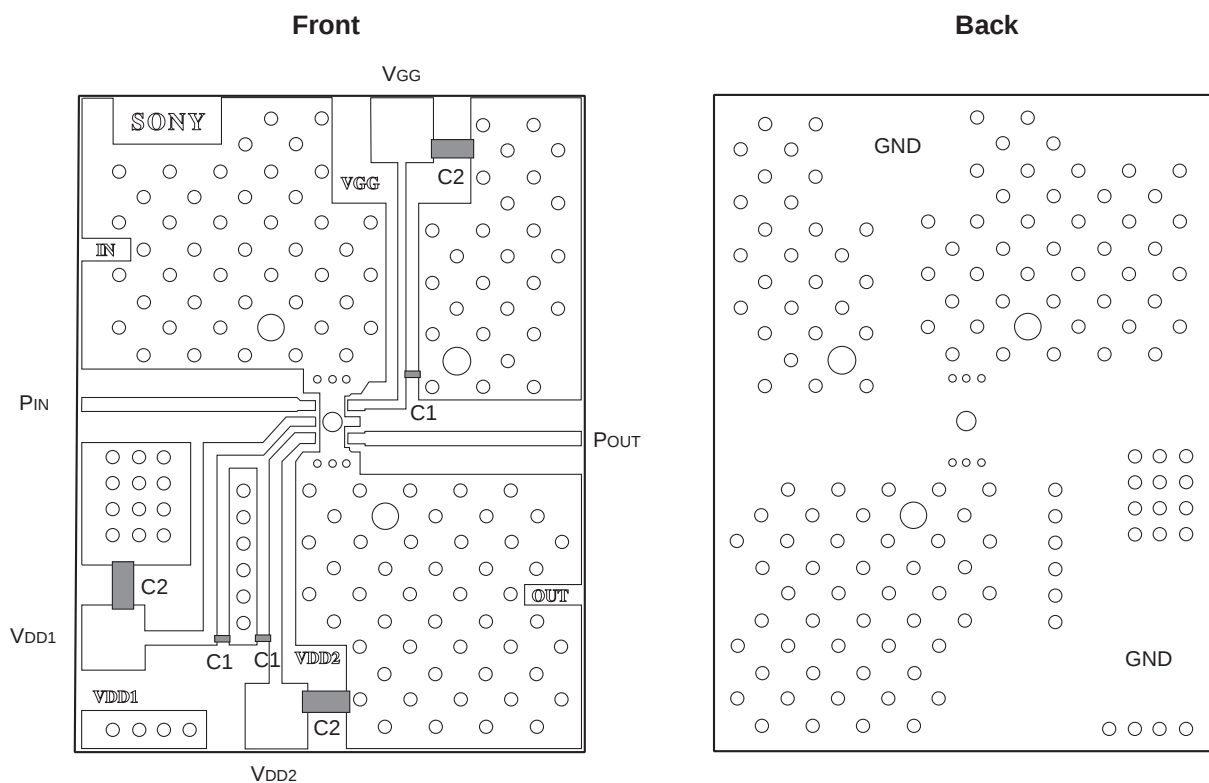


Recommended Evaluation Board

Board material: Glass fabric-base epoxy

Size: 40mm $\times$ 50mm $\times$ 0.6mm

Relative dielectric constant: 4.6



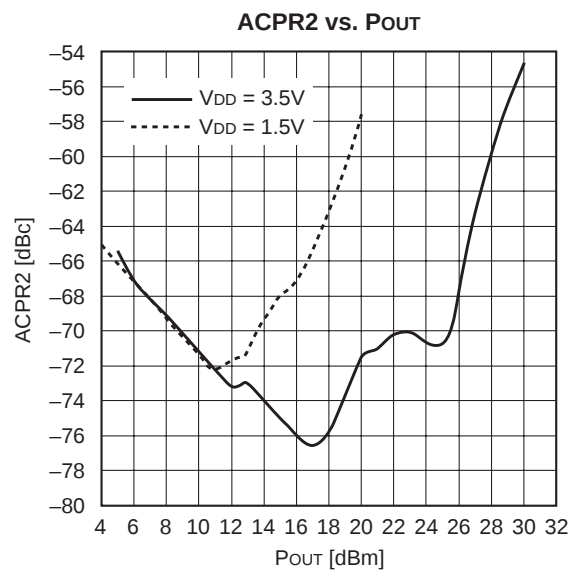
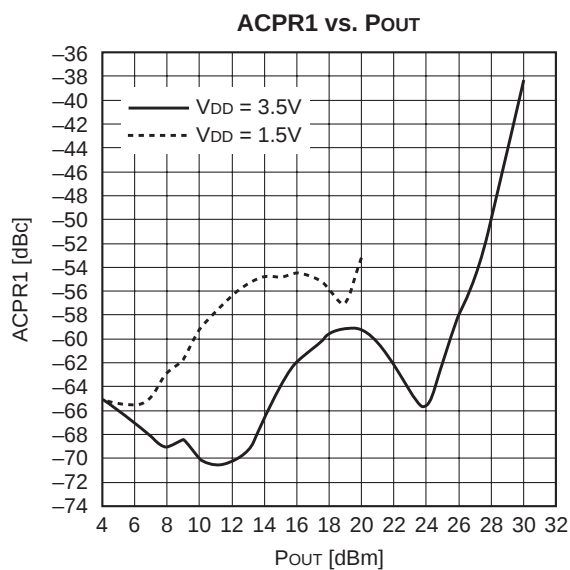
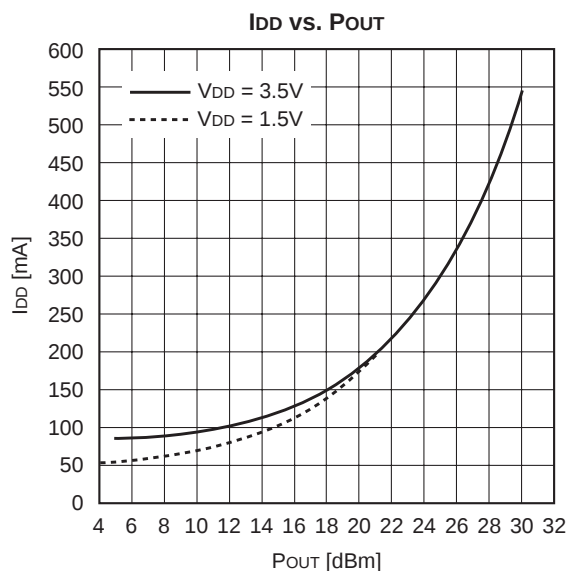
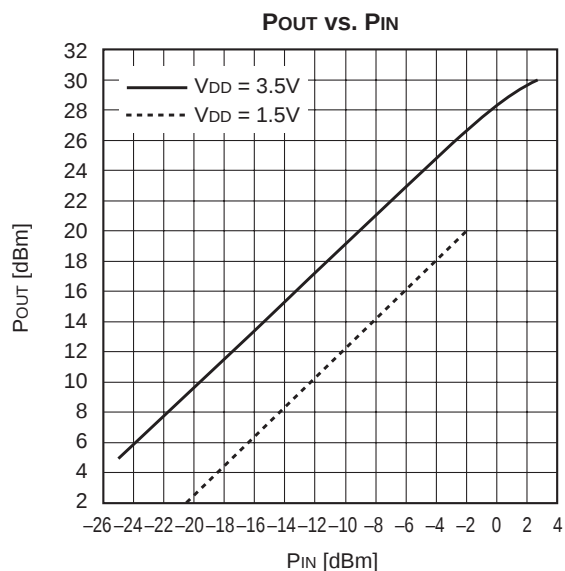
Example of Representative Characteristics

Conditions: $f = 900\text{MHz}$

$V_{DD1} = V_{DD2} = 3.5\text{V}$, $V_{GG} = 2.8\text{V}$ (High mode)

$V_{DD1} = V_{DD2} = 1.5\text{V}$, $V_{GG} = 2.8\text{V}$ (Mid mode)

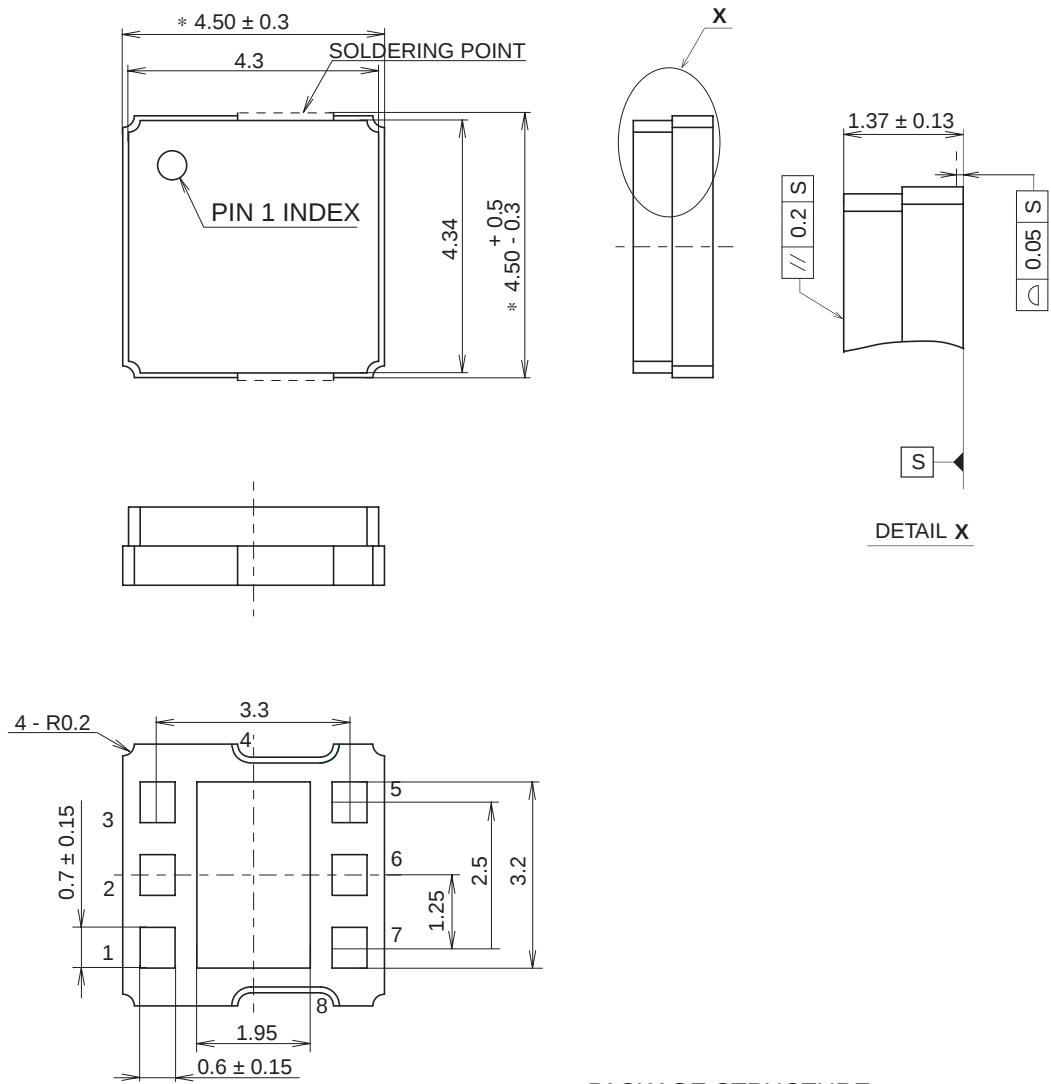
$T_a = 25^\circ\text{C}$



Package Outline

Unit: mm

8PIN LCC



NOTE: Dimension "*" does not include cutting burr.

SONY CODE	LCC-8C-371
EIAJ CODE	_____
JEDEC CODE	_____

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC SUBSTRATE
TERMINAL TREATMENT	GOLD PLATING
TERMINAL MATERIAL	NICKEL PLATING
PACKAGE MASS	0.08g