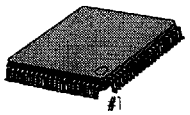
KS7213 CCD TIMING GENERATOR

GENERAL DESCRIPTION

The KS7213 is a timing generator IC which generates the timing pulses necessary for color CCD image sensors.

80-QFP-1212



ORERING INFORMATION

Device	Package	Operating Temperature
KS7213	80-QFP-1212	0 ~ 70°C

FEATURES

(1) SYNC signals and timing pulse generation.
- CCD, CDS, ADC clock system.
- PCLK (DCP2 Pipeline clock) system.
- Fsc. (sub-carrier frequency) clock system.

(2) External Sync mode available with External Line Reset or External VD/HD signals.

(3) Digital Image Stabilizing system(DIS) supported.
- Vertical stabilizing (Horizontal stabilizing --> FCM)
- Supported CCD type : 270K, 320K, 440K, 470K, 570K, 630K, pixels CCD

(4) Variable programmable High/low speed shutter.
- 1/2sec. to 1/100,000sec.
- Non flicker operation available. (by line lock)

(5) Digital Zoom supported.
- Vertical zooming ; x1 to x4, 192 step.
  (Horizontal zooming and Pixel interpolation --> DZ-IC)

(6) High speed pulse timings adjustable.
- H1/H2 : 0 ~ 30ns, 2ns step, from PCLK.
- RG : -8 ~ 7ns, 1ns step, from H1/H2.
- SHP : -8 ~ 7ns, 1ns step, from H1/H2.
- SHD : -8 ~ 7ns, 1ns step, from H1/H2
- SP0 : -8 ~ 14ns, 2ns step, pos/neg, from H1/H2
- FWCK : -8 ~ 14ns, 2ns step, pos/neg, from H1/H2

(7) Video signal system ; NTSC / PAL

(8) Camera system ; NORMAL / Hi-BAND / DIS / WIDE (NTSC / PAL), Hi-DIS / Hi-WIDE (NTSC only)

(9) Oscillation source ; Single crystal
- NTSC : 28.6363MHz
- PAL : 28.3750MHz

(10) 2-port of serial I/O interface for system MICOM and DIS MICOM.

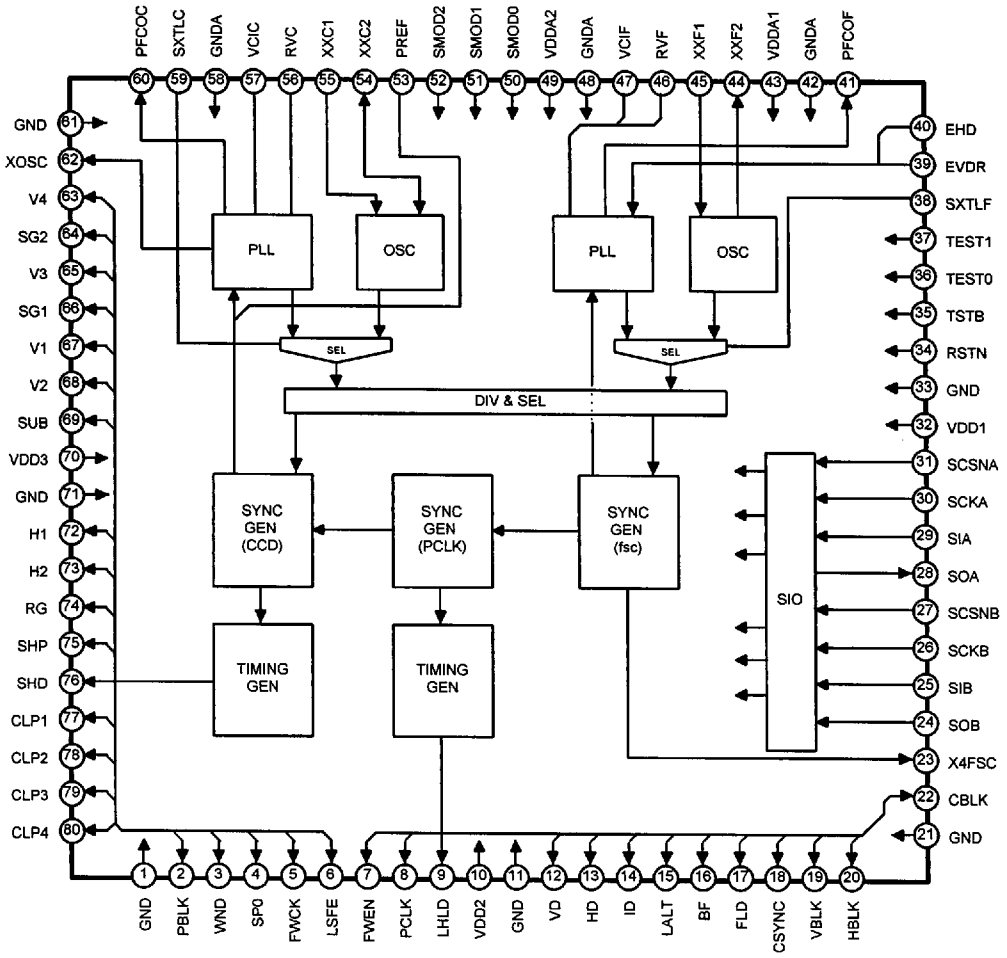
(11) Power save mode ; most of output signals be disabled (Low level fixed), except `CSYNC`

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	- 0.3 ~ + 7.0	V
Input Voltage	V_I	- 0.3 ~ V_{DD} + 0.3	V
Output Voltage	V_O	-0.3 ~ V_{DD} + 0.3	V
Latch-up Current	L_{LU}	±100	mA
Storage Temperature	T_{STG}	- 40 ~ + 125	°C
Operating Temperature	T_{OPR}	0 ~ + 70	°C

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No	Symbol	I/O	From/To	Description	ACT Level	PWR Save	Note
1	GND	-	-	Digital ground	-		
2	PBLK	O	CDS	Pre-blanking pulse	"L"	"L"	
3	WND	O	CDS	Windows pulse	"H"	"L"	
4	SP0	O	ADC	Sampling pulse	↑	"L"	
5	FWCK	O	FCM	FCM write clock	↑	"L"	
6	LSFE	O	(field mem)	Low Speed Shutter Field enable	"H"	"L"	
7	FWEN	O	FCM	FCM write enable	"L"	"L"	
8	PCLK	O	DCP	Pipeline Clock for DCP	↑	"L"	
9	LHLD	O	DCP	Line Hold	"H"	"L"	
10	VDD2	-	-	Power Supply for PCLK logic	-		
11	GND	-	-	Digital ground	-		
12	VD	O	DCP, FCM	V driving pulse	↓	"L"	
13	HD	O	DCP, FCM	H driving pulse	↓	"L"	
14	ID	O	DCP	Line identifier	"H/L"	"L"	
15	LALT	O	DCP	Line alternation	"H/L"	"L"	
16	BF	O	DCP	Burst flag	"L"	"L"	
17	FLD	O	DCP	Field index	"H/L"	"L"	
18	CSYNC	O	DCP	Composite Sync	↓	act.	
19	VBLK	O	DCP	Vertical blanking	"L"	"L"	
20	HBLK	O	DCP	Horizontal blanking	"L"	"L"	
21	GND	-	-	Digital ground	-		
22	CBLK	O	DCP	Composite blanking	"L"	"L"	
23	X4FSC	O	DCP	Sub-carrier X4 (4fsc)	↑	act.	
24	SOB	O	MICOM	Serial I/O port-B data output	-		
25	SIB	I	MICOM	Serial I/O port-B data input	-		normal "L"
26	SCKB	I	MICOM	Serial I/O port-B clock	-		
27	SCSNB	I	MICOM	Serial I/O port-B chip select	-		
28	SOA	O	MICOM	Serial I/O port-A data output	-		
29	SLA	I	MICOM	Serial I/O port-A data input	-		
30	SCKA	I	MICOM	Serial I/O port-A clock	-		
31	SCSNA	I	MICOM	Serial I/O port-A chip select	-		
32	VDD1	-	-	Power Supply for Fsc logic	-		
33	GND	-	-	Digital ground	-		
34	RSTN	-	System	Initial reset (Active Low)	-		
35	TSTB	I	System	Test strobe pulse input	-		
36	TEST0	I	System	"LL": Normal mode, "LH": Test mode 1	-		normal "L"
37	TEST1	I	System				
38	SXTL	I	-	X'tal / VCO select for F-clock	"H/L"	-	normal "L"
39	EVDR	I	Ext. Sync	Ext. Line Reset / Ext. VD	"L"	-	
40	EHD	I	Ext. Sync	Ext. HD	"L"	-	
41	PFCOF	O	Loop Filter	PFC charge pump output (fsc)	"L"		
42	GNDA	-	-	Analog Ground	-		

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{DD} = 5.0V, Ta = 0 to 70°C)

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}		4.75	5.0	5.25	V	
	I_{DD}		-	40	-	mA	
Input Voltage	V_{IH}		$0.7V_{DD}$	-	-	V	
	V_{IL}		-		$0.3V_{DD}$	V	
Input Current	I_{IH}	$V_{IH} = V_{DD}$	-10		10	μA	
	I_{IL}	$V_{IL} = V_{SS}$	-10		10	μA	
Output Voltage	V_{OH0}	I_{OH} = -1μA	V_{DD} - 0.05		-	V	
	V_{OH1}	I_{OH} = -1mA	2.4	-	-	V	(*1)
	V_{OH2}	I_{OH} = -2mA	2.4	-	-	V	(*2)
	V_{OH3}	I_{OH} = -4mA	2.4	-	-	V	(*3)
	V_{OH4}	I_{OH} = -8mA	2.4	-	-	V	(*4)
	V_{OH5}	I_{OH} = -12mA	2.4	-	-	V	(*5)
	V_{OL0}	I_{OL} = 1μA	-	-	0.05	V	
	V_{OL1}	I_{OL} = 1mA	-	-	0.4	V	(*1)
	V_{OL2}	I_{OL} = 2mA	-	-	0.4	V	(*2)
	V_{OL3}	I_{OL} = 4mA	-	-	0.4	V	(*3)
	V_{OL4}	I_{OL} = 8mA	-	-	0.4	V	(*4)
	V_{OL5}	I_{OL} = 12mA	-	-	0.4	V	(*5)
Leakage	I_{OZ}	$V_O = V_{DD}$ or V_{SS}	-10	-	10	μA	(*6)

(*1) Most of output pins except (*2), (*3), (*4), (*5), (*6).
(*2) Pin no. 2, 3, 8, 23, 28, 77, 78, 79, 80.
(*3) Pin no. 75, 76.
(*4) Pin no. 74.
(*5) Pin no. 72, 73.
(*6) Pin no. 24, 28 (3 state output)

(Continued)

Pin No	Symbol	I/O	From/To	Description	ACT Level	PWR Save	Note
43	VDDA1	-	-	Power Supply for Fsc analog	-		
44	XXF2	O	X'tal	Ext.Crystal for int. sync mode	-		
45	XXF1	I	X'tal	(4fsc)	-		
46	RVF	O	Ext.resistor	Ext. Resistor for VCO (fsc)	-		
47	VCIF	I	Loop Filter	VCO control voltage input (fsc)	-		
48	GNDA	-	-	Analog Ground	-		
49	VDDA2	-	-	Power Supply for PCLK & CCD analog	-		
50	SMOD0	I	System	Operation mode select input.	-		
51	SMOD1	I	System	SMOD2: NTSC/PAL			
52	SMOD2	I	System	SMOD1,0: "00" = Normal "01" = Hiband "10" = DIS/Wide "11" = HiDIS/HiWide			
53	PREF	O	-	PFC Reference output for CCD clock	-		for test
54	XXC2	O	X'tal	Ext. Crystal for test	-		
55	XXC1	I	X'tal	(2CCD clock)	-		
56	RVC	O	Ext.resistor	Ext. Resistor for VCO (fsc)	-		
57	VCIC	I	Loop Filter	VCO control voltage input (CCD)	-		normal "L"
58	GNDA	-	-	Analog Ground	-		
59	SXTLC	I	-	X'tal/VCO select for CCD clock	"L"		normal "H"
60	PFCOC	O	Loop Filter	PFC charge pump output (fsc)	"L"		
61	GND	-	-	Digital ground	-		
62	XOSC	-	-	CCD clock X2	↑	"L"	
63	V4	O	VD	V scanning pulse 4	"H/L"	"L"	
64	SG2	O	VD	Sensor Gate pulse 2	"L"	"L"	
65	V3	O	VD	V scanning pulse 3	"H/L"	"L"	
66	SG1	O	VD	Sensor Gate pulse 1	"L"	"L"	
67	V1	O	CCD(VD)	V scanning pulse 1	"H/L"	"L"	
68	V2	O	CCD(VD)	V scanning pulse 2	"H/L"	"L"	
69	SUB	O	CCD(VD)	Substrate clock pulse	"L"	"L"	
70	VDD3	-	-	Power Supply for CCD logic	-	-	
71	GND	-	-	Digital ground	-	-	
72	H1	O	CCD	H scanning pulse 1	"H/L"	"L"	
73	H2	O	CCD	H scanning pulse 2	"H/L"	"L"	
74	RG	O	CCD	Reset Gate pulse	"H"	"L"	
75	SHP	O	CDS	Pre-charge S/H pulse	"L"	"L"	
76	SHD	O	CDS	Data S/H pulse	"L"	"L"	
77	CLP1	O	CDS	OPB clamping pulse 1	"H"	"L"	
78	CLP2	O	CDS	OPB clamping pulse 2	"H"	"L"	
79	CLP3	O	CDS	OPB clamping pulse 3	"H"	"L"	
80	CLP4	O	CDS	OPB clamping pulse 4	"H"	"L"	

AC CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
Ringing Time 1	t_{R1}	C_L = 10pF		3		nSec	
Falling Time 1	t_{F1}	C_L = 10pF		3		nSec	
Ringing Time 2	t_{R2}	C_L = 20pF		3		nSec	(*1)
Falling Time 2	t_{F2}	C_L = 20pF		3		nSec	(*1)
Ringing Time 3	t_{R3}	C_L = 50pF		10		nSec	(*2)
Falling Time 3	t_{F3}	C_L = 50pF		10		nSec	(*2)

(*1) Pin no. 74 (RG : Reset Gate)
(*2) Pin no. 72, 73 (H1, H2 : Horizontal driving clock)

CONTROL REGISTERS

PORT-A module 0 (for SYSTEM MICOM)

COMMAND

`0`	`0`	`0`	`0`	RE	WE	`0`	`0`

WE : Write Enable / $\overline{\text{Disable}}$

RE : Read Enable / $\overline{\text{Disable}}$

ADRS

<WRITE>

	MSB							LSB
0	SG2 = SG1	PWR SAV	FCM OFF	SYNC Ext/$\overline{\text{Int}}$	$\overline{\text{DIS}}$/ ENB	CINE ENB	EHD OFF	FV2 ON
1	ZMIV							
	-1	-2	-3	-4	-5	-6	-7	-8
2	ZSTI							
	7	6	5	4	3	2	1	0
3	ZSTS							
	-1	-2	-3	-4	-5	-6	-7	-8
4	SHTR MD		LSSC				HSSC	
	1	0	3	2	1	0	9	8
5	HSSC							
	7	6	5	4	3	2	1	0
6	SDCX				SDRG			
	3	2	1	0	3	2	1	0
7	SDHD				SDHP			
	3	2	1	0	3	2	1	0
8	SDSP				SDFW			
	3	2	1	0	3	2	1	0
9	SDRA							
	3	2	1	0	0	0	0	0

<READ>

	MSB							LSB
0	SG2 = SG1	PWR SAV	FCM OFF	SYNC Ext/$\overline{\text{Int}}$	$\overline{\text{DIS}}$/ ENB	CINE ENB	EHD OFF	FV2 ON
1	ZLAPHA							
	-1	-2	-3	-4	-5	-6	-7	-8
2	NSL							
	7	6	5	4	3	2	1	0
3	ZINIT							
	-1	-2	-3	-4	-5	-6	-7	-8
4	SHTR MD		LSSCO				HSSCO	
	1	0	3	2	1	0	9	8
5	HSSCO							
	7	6	5	4	3	2	1	0
6	SDCX				SDRG			
	3	2	1	0	3	2	1	0
7	SDHD				SDHP			
	3	2	1	0	3	2	1	0
8	SDSP				SDFW			
	3	2	1	0	3	2	1	0
9	SDRA							
	3	2	1	0	3	2	1	0

STOP BYTE	`1`	`1`	`1`	`0`	`0`	`1`	`0`	P

(1) FV2 ON ; `0` : 2fv OFF / 2fv ON
(2) EHD OFF ; `0` : EXT.HD ON / `1` : EXT.HD OFF.
(3) CINEMA mode; `0` : Normal Mode / `1` : CINEMA Mode.
(4) DIS Enable ; `0` : Not DIS Mode / `1` : DIS Mode.
(5) SYNC Ext / Int ; `0` : Internal Sync. / `1` : External Sync.
(6) FCM OFF ; `0` : With FCM. / `1` : Without FCM.
(7) PWRSAV ; `0` : Normal operation mode.
`1` : Power - save mode (only `CSYNC` active)
(8) SG2 = SG1; `0` : Normal operation mode.
`1` : `SG2` will be same timing as `SG1` (for exam.).
(9) ZMIV : Inverse number of vertical zoom magnifying ratio. (8 bit)
`(0.) 11111111` ~ `(0.) 01000000` (192 step), ALL`0` means 1X.
(10) ZSTI, ZSTS : CCD vertical start point by zoom. (16 bit)
ZSTI, : Integer lines, ZSTS : Sub-pixel, ZSTI.ZSTS > 0.
(11) SHTR MD : Shutter mode select (2bit)
`0 0` : No shutter mode
`0 1` : Low speed shutter mode (1/2 - 1/60 sec.)
`1 0` : High speed shutter mode (1/60 - 1/100,000 sec.)
`1 1` : (Reserved)
(12) LSSC : Low Shutter Speed Control (4bit) --> see Time Chart 3-1, 3-2
(13) HSSC : High Shutter Speed Control (10bit) --> see Time Chart 3-3, 3-4
(14) SDCX : "PCLK" to "H1", "H2" delay adjust control code. (4bit)
(15) SDRG : "H1" to "G" delay adjust control code. (4bit)
(16) SDHP : "H1" to "SHP" delay adjust control code. (4bit)
(17) SDHD : "H1" to "SHD" delay adjust control code. (4bit)
(18) SDSP : "H1" to "SP0" delay adjust and polarity control code. (4bit)
(19) SDFW : "H1" to "FWCK" delay adjust and polarity control code. (4bit)
(20) SDRA : RG,SHP Pulse width Adjust. (4bit)
* (14) to (20) ; see Table1
(21) P : Even Parity for write access.
(22) ZALPHA : Vertical zoom interpolating coefficient. (8bit) --> see Fig. 1
ZALPHA = decimal (ZINIT + N X ZMIV)
(23) NSL : A number of vertical skip line. (8bit) --> see Fig. 1
ZINIT = integer (ZSTI.ZSTS + DOFI.DOFS)
(24) ZINIT : Initial value of ZALPHA. (8bit)
ZINIT = decimal (ZSTI.ZSTS + DOFI.DOFS) --> see Fig. 1
(25) LSSCO : Low speed shutter control counter value. (4bit)
(26) HSSCO : High speed shutter control counter value. (10bit)

DELAY ADJUST CONTROL CODE

Table 1.

(1) H1/H2 CTL

SDCX	DELAY
0000	0
0001	2ns
0010	4ns
0011	6ns
0100	8ns
0101	10ns
0110	12ns
0111	14ns
1000	16ns
1001	18ns
1010	20ns
1011	22ns
1100	24ns
1101	26ns
1110	28ns
1111	30ns

(2) RG CTL

SDRG	DELAY
1000	-8ns
1001	-7ns
1010	-6ns
1011	-5ns
1100	-4ns
1101	-3ns
1110	-2ns
1111	-1ns
0000	0
0001	1ns
0010	2ns
0011	3ns
0100	4ns
0101	5ns
0110	6ns
0111	7ns

(3) SHD CTL

SDHD	DELAY
1000	-8ns
1001	-7ns
1010	-6ns
1011	-5ns
1100	-4ns
1101	-3ns
1110	-2ns
1111	-1ns
0000	0
0001	1ns
0010	2ns
0011	3ns
0100	4ns
0101	5ns
0110	6ns
0111	7ns

(4) SHP CTL

SDHP	DELAY
1000	-8ns
1001	-7ns
1010	-6ns
1011	-5ns
1100	-4ns
1101	-3ns
1110	-2ns
1111	-1ns
0000	0
0001	1ns
0010	2ns
0011	3ns
0100	4ns
0101	5ns
0110	6ns
0111	7ns

(5) SPO CTL

SDSP	EDGE	DELAY
0000	↑	0
0001		2ns
0010		4ns
0011		6ns
0100		8ns
0101		10ns
0110		12ns
0111		14ns
1000	↓	0
1001		2ns
1010		4ns
1011		6ns
1100		8ns
1101		10ns
1110		12ns
1111		14ns

(6) FWCK CTL

SDFW	EDGE	DELAY
0000	↑	0
0001		2ns
0010		4ns
0011		6ns
0100		8ns
0101		10ns
0110		12ns
0111		14ns
1000	↓	0
1001		2ns
1010		4ns
1011		6ns
1100		8ns
1101		10ns
1110		12ns
1111		14ns

(7) HI D/W CTL

SDRA	DELAY
1000	8ns
1001	9ns
1010	10ns
1011	11ns
1100	12ns
1101	13ns
1110	14ns
1111	15ns
0000	0
0001	1ns
0010	2ns
0011	3ns
0100	4ns
0101	5ns
0110	6ns
0111	7ns

POAT-A module 7 (for SYSTEM MICOM)

`0`	`1`	`1`	`1`	RE	WE	0	0

WE : Write Enable / $\overline{\text{Disable}}$

RE : Read Enable / $\overline{\text{Disable}}$

ADRS	<WRITE> MSB							LSB	<READ> MSB							LSB
0	Y VP/HP	F VP/HP	TFCV 9	8	7	6	5	4	Y VP/HP	F VP/HP	TFCV 9	8	7	6	5	4
1	TFCV 3	2	1	0	-	TFCH 10	9	8	TFCV 3	2	1	0	-	TFCH 10	9	8
2	TFCH 7	6	5	4	3	2	1	0	TFCH 7	6	5	4	3	2	1	0
3	TYCF-	TYCV 0	9	8	7	6	5	4	TYCF-	TYCV 0	9	8	7	6	5	4
4	TYCV 3	2	1	0	-	TYCH 10	9	8	TYCV 3	2	1	0	-	TYCH 10	9	8
5	TYCH 7	6	5	4	3	2	1	0	TYCH 7	6	5	4	3	2	1	0
6	EXP CAS/PAR	H SYNC	TYCH 13	12	11	10	9	8	EXP CAS/PAR	H SYNC	TYCH 13	12	11	10	9	8
7	TCCD 7	6	5	4	3	2	1	0	TCCD 7	6	5	4	3	2	1	0
STOP BYTE	`1`	`1`	`1`	`0`	`0`	`1`	`0`	`P`								

(1) TFCV : FSC clock counter test data.

(a) TFCV : H counter (11bit)

(b) TFCH : H counter (10bit)

(2) YCLK counter test data.

(a) TYCF : F counter (1bit)

(b) TYCV : V counter (11bit)

(c) TYCH : H counter (11bit)

* (1) to (2) ; Write : counter load data. Read : counter output data.

(3) Y VP/HP ; YPLL(PCLK) Mode `0` : HPLL/ `1` : VPLL.

(4) F VP/HP ; FPLL(4FSC) Mode `0` : HPLL/ `1` : VPLL.

(5) EPLL mode ; External Sync PAL mode select (Option) `0` cascode/ `1` : parallel

(6) Hsync ; `0` None of Exeternal EHD `1` Exeternal EHD

Notes ; Line lock(EVD, PLL) can be programmed by using this bit.

(7) P ; Even parity for write access.

PORT-A module F (for SYSTEM MICOM)

COMMAND

`1`	`1`	`1`	`1`	RE	WE	0	0

WE : Write Enable / $\overline{\text{Disable}}$

RE : Read Enable / $\overline{\text{Disable}}$

ADRS <WRITE>

	MSB							LSB
0				-				

<READ>

PE	WF	`0`	`0`	`0`	`0`	`0`	`0`

(1) PE : Register write parity error

`1` : ERROR

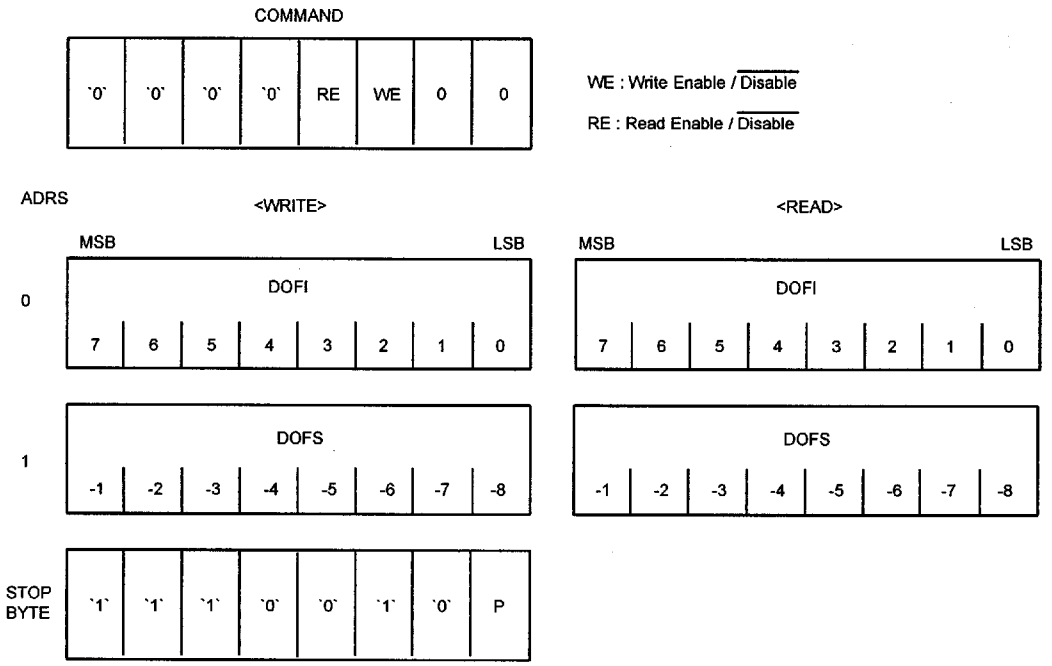
`0` : Not ERROR

(2) WF : Register write status flag

`1` : Waiting for write data be accepted

`0` : Accepted

PORT-B module 0 (for DIS MICOM)



(1) DOFI, DOFS : Vertical offset from CCD start point by DIS vertical motion vector. (16bit)
DOFI : Integer lines, DOFS : Sub-pixel,
when DOFI.DOFS < 0, written by 16 bit 2`s comp.

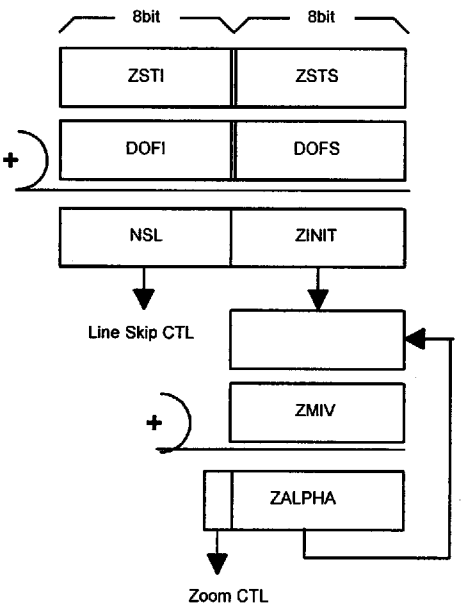


Fig. 1 Relation of Zoom Reg. & DIS Reg.

PORT-B module F (for DIS MICOM)

COMMAND

`1`	`1`	`1`	`1`	RE	WE	`0`	`0`

WE : Write Enable / $\overline{\text{Disable}}$

RE : Read Enable / $\overline{\text{Disable}}$

ADRS <WRITE>

	MSB							LSB
0	—							

<READ>

MSB							LSB
PE	WF	`0`	`0`	`0`	`0`	`0`	`0`

(1) PE : Register write parity error

`1` : ERROR

`0` : Not ERROR

(2) WF : Register write status flag

`1` : Waiting for write data be accepted

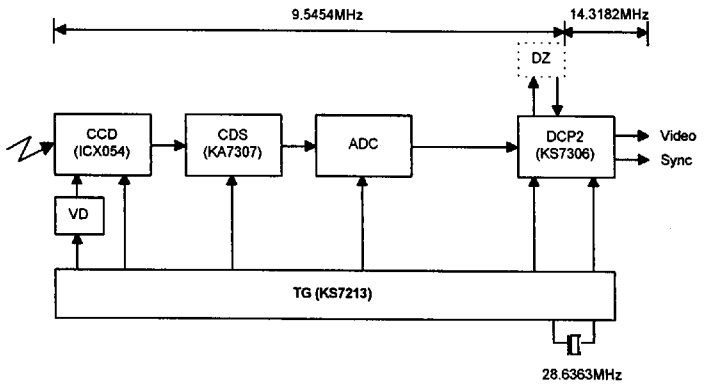
`0` : Accepted

DCP2 SYSTEM CLOCK and SYNC

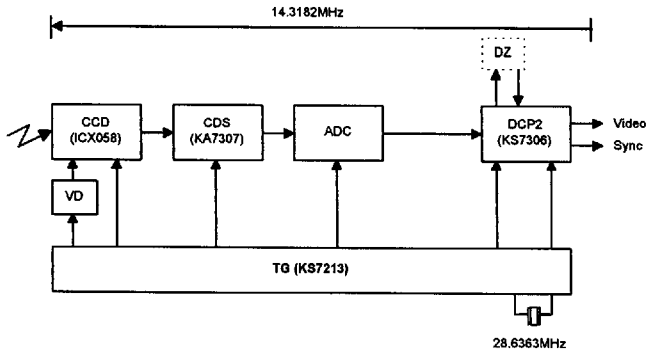
TV System	CCD Scale	Camera System		Sampling Frequency [MHz]	Scan Period		Picture Size		Stabiliz. Margin	CCD Type	Note
					H	V	H	V			
NTSC	270K	Normal		9.534964	606.7	525	510	485	-	ICX054AK ICX056AK	
	410K	Hi-band		14.318182	910.0		768		-	ICX058AK ICX068AK	
	470K	DIS	DCP	11.926372	758.0		629		20%	ICX059AK	
			CCD	14.318182	910.0		752	582			
		WIDE		14.318182	910.0		752	485	-		14.5 : 9
	630K	Hi-DIS	DCP	13.500000	858.0		711	485	34%	ICX080AK	
			CCD	18.000000	1144.0		948	654			
		Hi-WIDE		18.000000	1144.0		948	485	-		16 : 9
PAL	320K	Normal		9.453125	605.3	625	500	575	-	ICX055AK ICX057AK	
	470K	Hi-band		14.187500	908.0		752		-	ICX059AK ICX069AK	
	570K	DIS	DCP	11.812500	726.4		619		21%	ICX060AK	
			CCD	14.187500	908.0		752	697			
		WIDE		14.187500	908.0		752	575	-		14.7 : 9
	740K	Hi-DIS	DCP	13.500000	864.0		702	575	35%	ICX081AK	
			CCD	18.000000	1152.0		936	774			
		Hi-WIDE		18.000000	1152.0		936	575	-		16 : 9

APPLICATION SYSTEMS

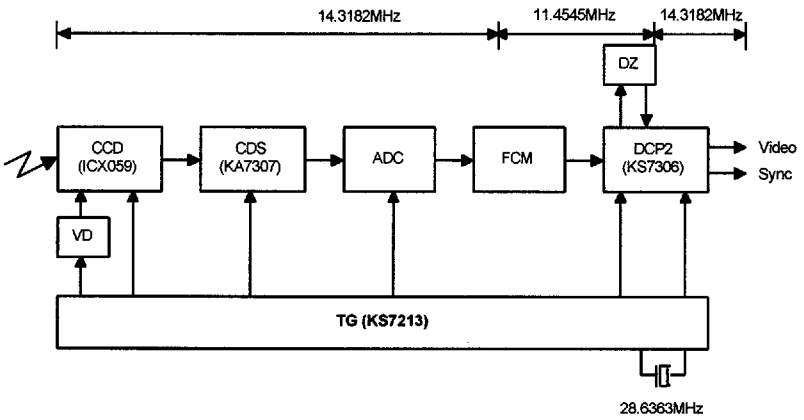
(1) NTSC NORMAL SYSTEM



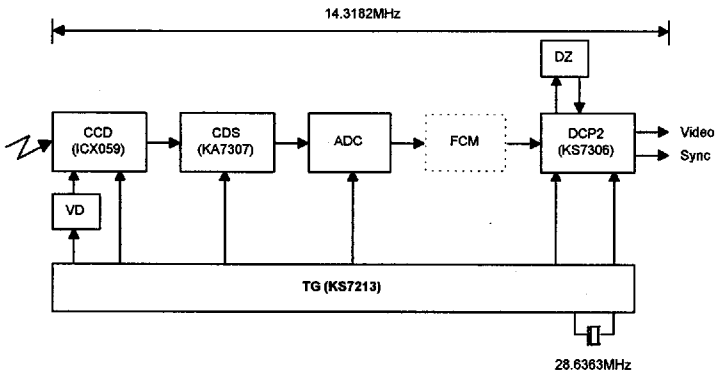
(2) NTSC Hi-BAND SYSTEM



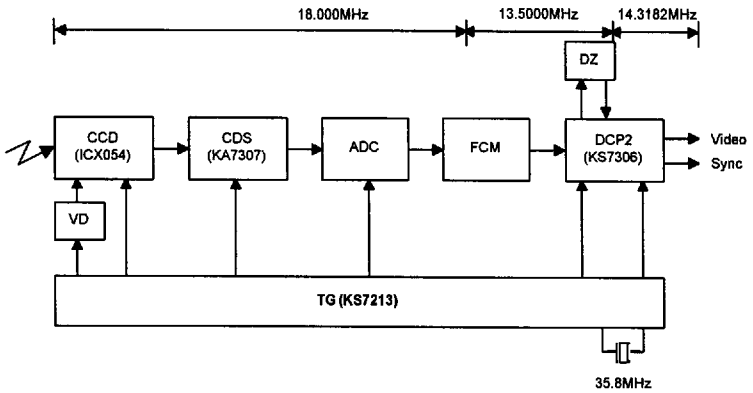
(3) NTSC DIS SYSTEM



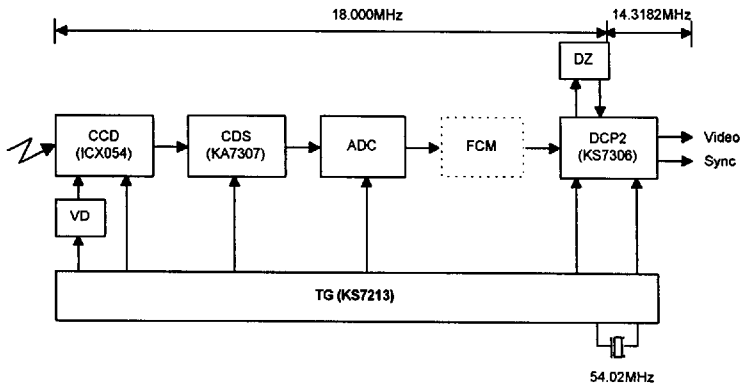
(4) NTSC WIDE SYSTEM



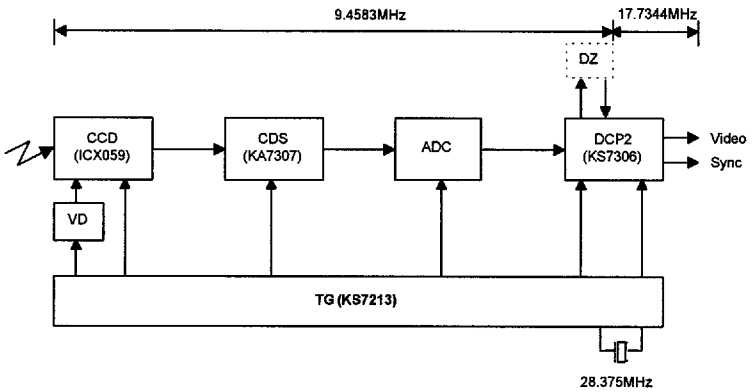
(5) NTSC Hi-DIS SYSTEM



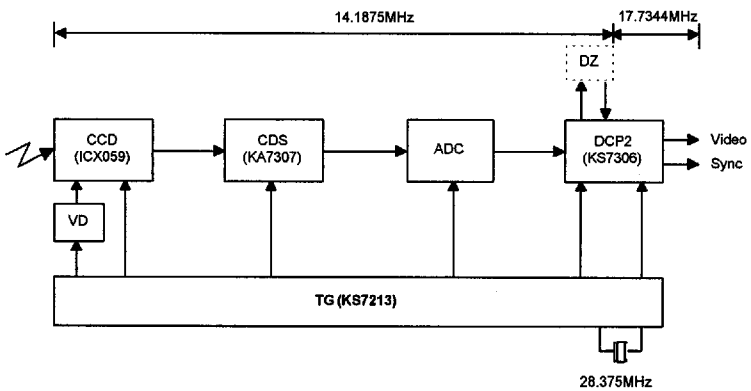
(6) NTSC Hi-WIDE SYSTEM



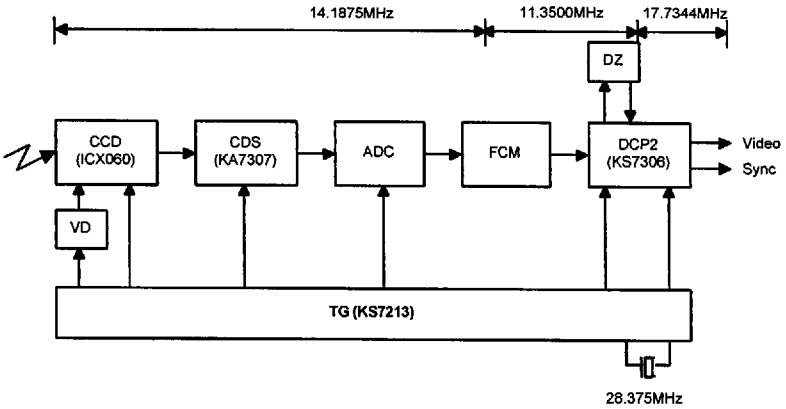
(7) PAL NORMAL SYSTEM



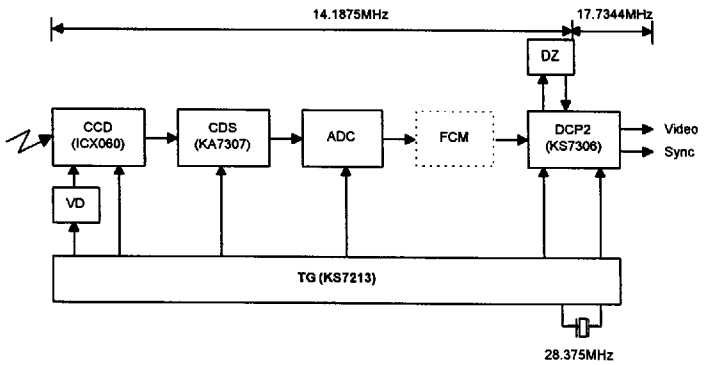
(8) PAL Hi-BAND SYSTEM



(9) PAL DIS SYSTEM

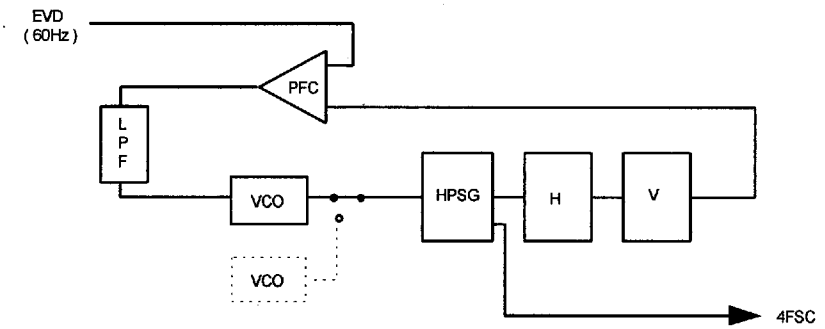


(10) PAL WIDE SYSTEM

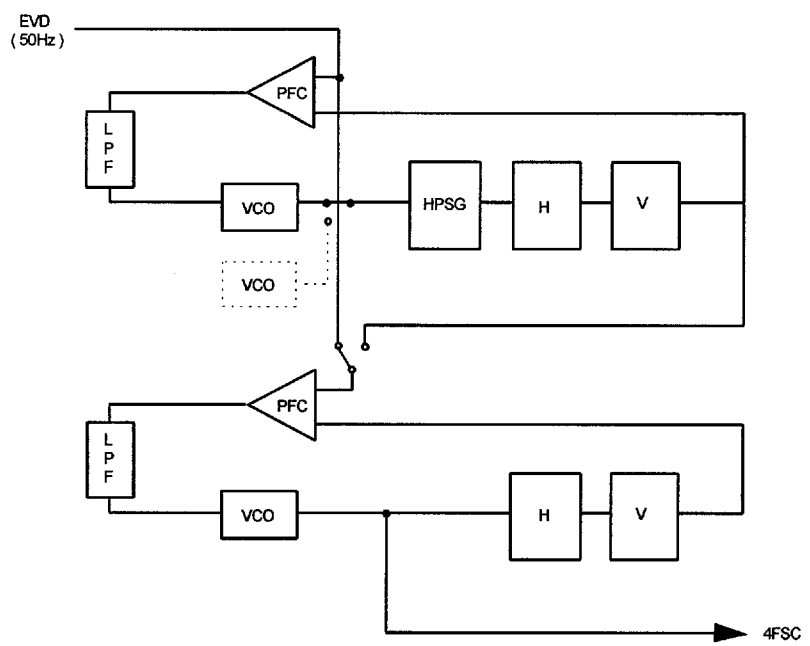


(11) EXTERNAL SYNC

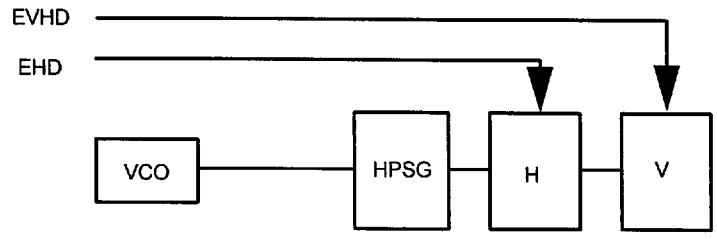
a. Line Lock (NTSC)



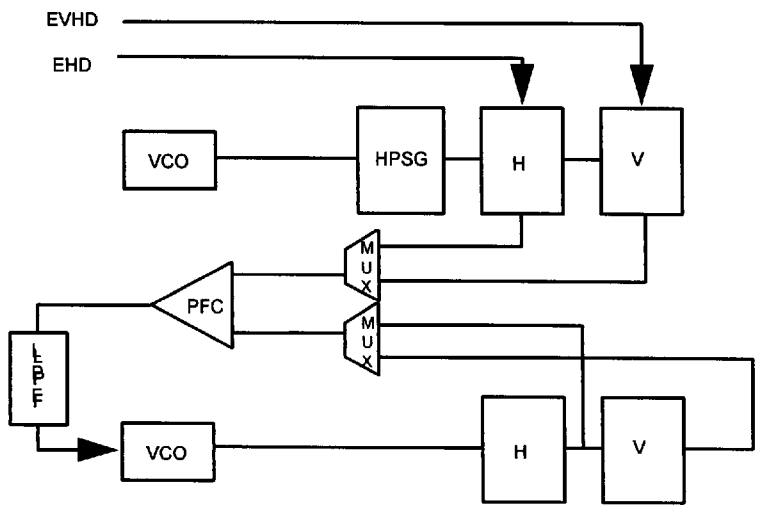
b. Line Lock (PAL)



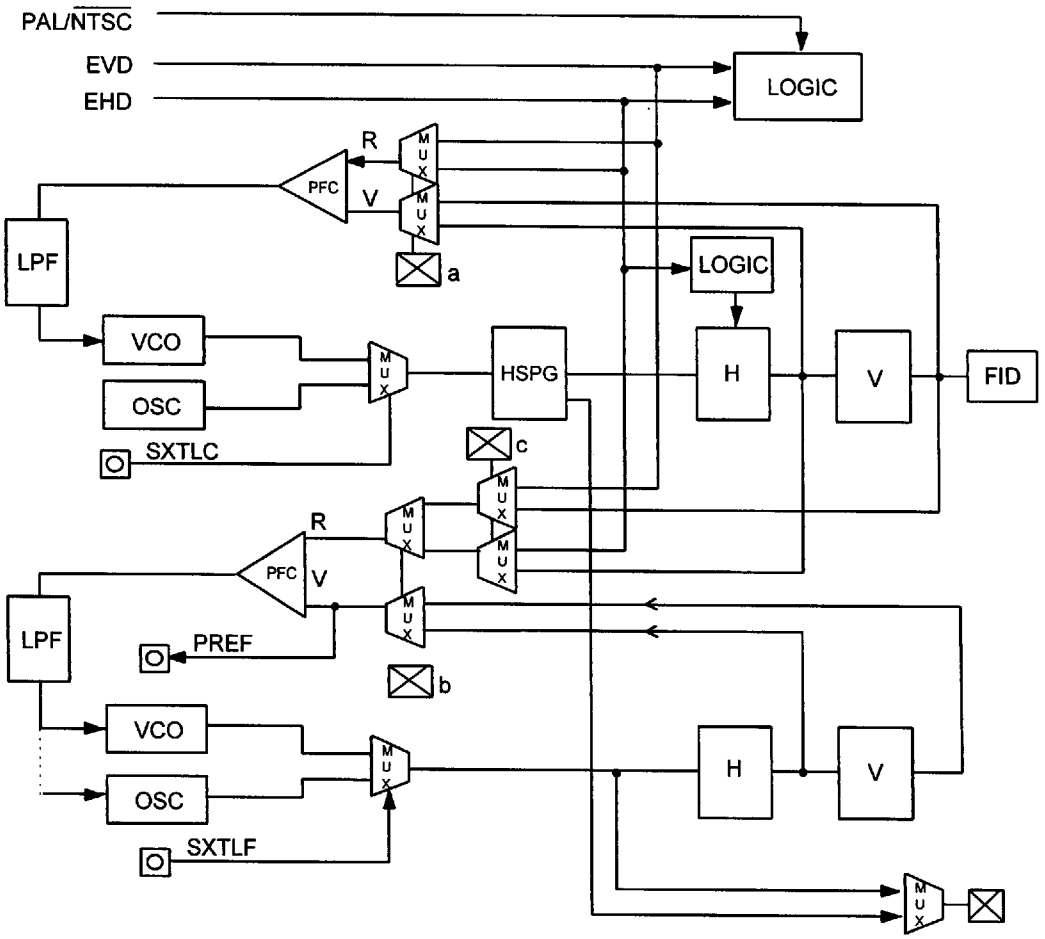
c. V/H Reset (NTSC)



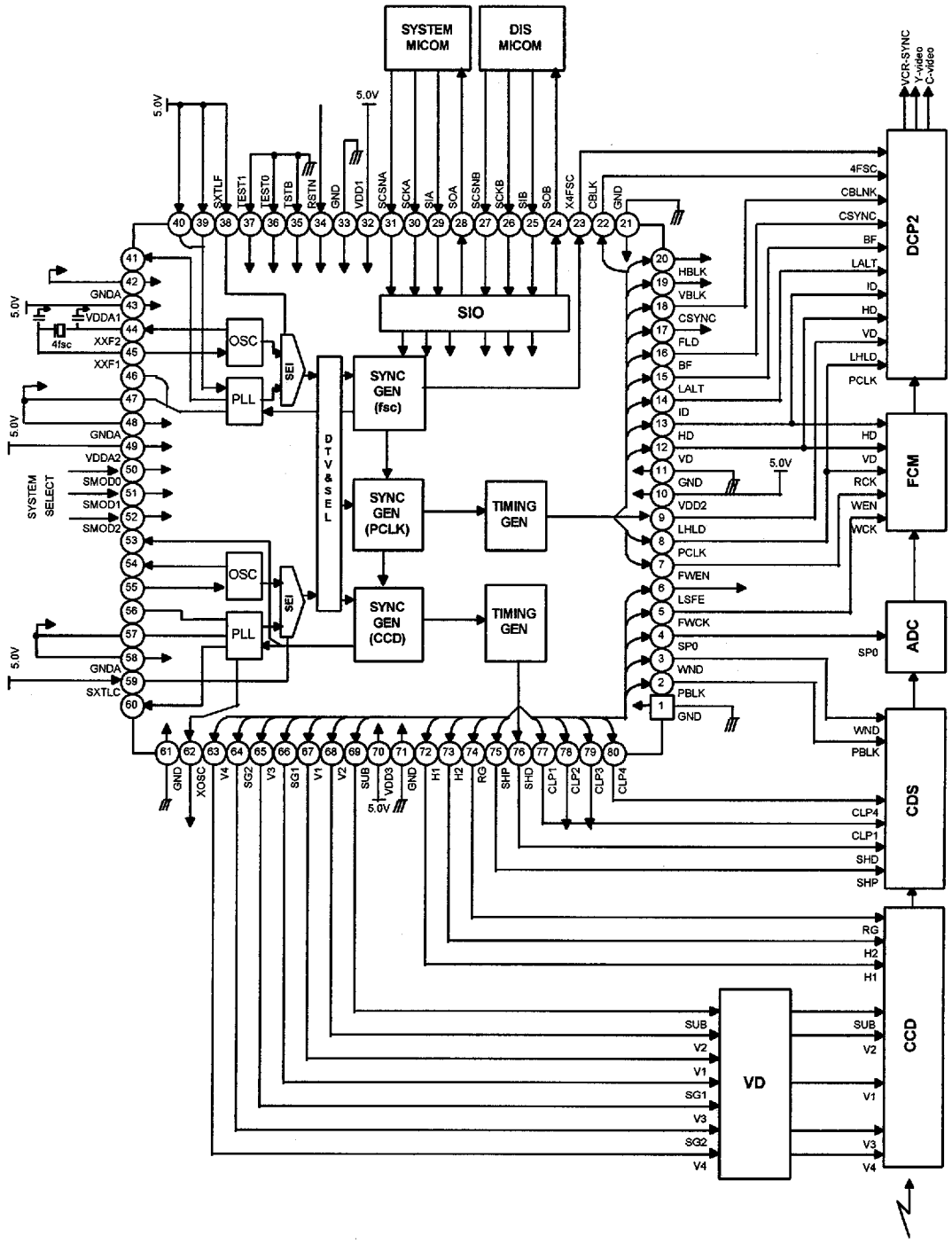
d. V/H Reset (PAL)



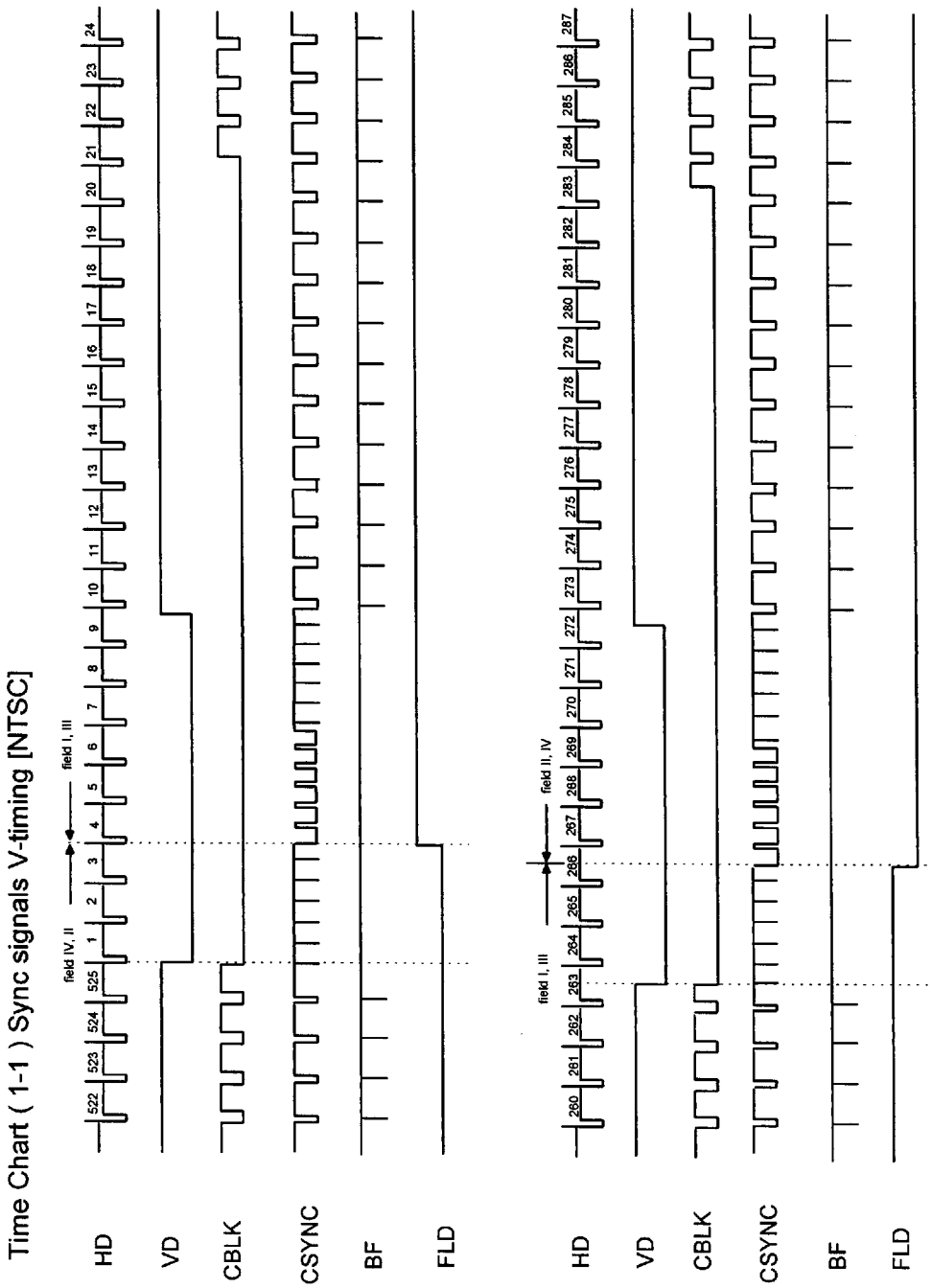
	NTSC				PAL			
	INT	Line Lock	V / HR	VR HPL	ZNT	Line Lock	V /HR	VR HPL
EXTSvnc	0	1	1	1	0	1	1	1
Y VPLL/HPLL	X	1	X	0	X	1	X	0
F VPLL/HPLL	X	X	X	0	0/1	1	same with INT	0
2fv ON/OFF	X	X	X	X	0/1 0/1	0/1	↑	0
EHD/No EHD	X	1	0	1	X	1	0	0
HSYNC EH Reset/ Self Reset	X	X	1	0	X	X	1	0
PALMOD Cas/para	X	X	X	X	X	0/1	1	0/1



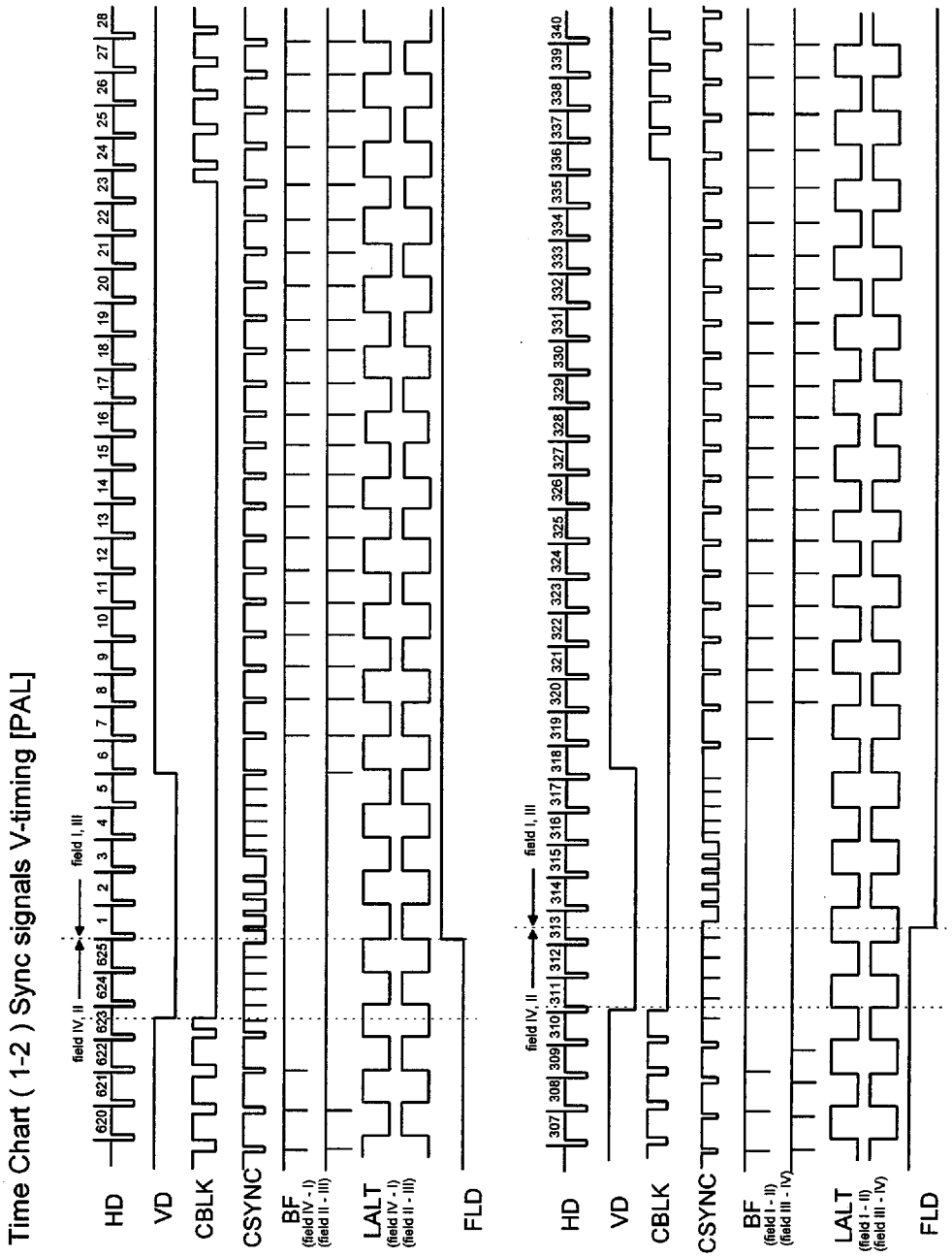
APPLICATION CIRCUIT

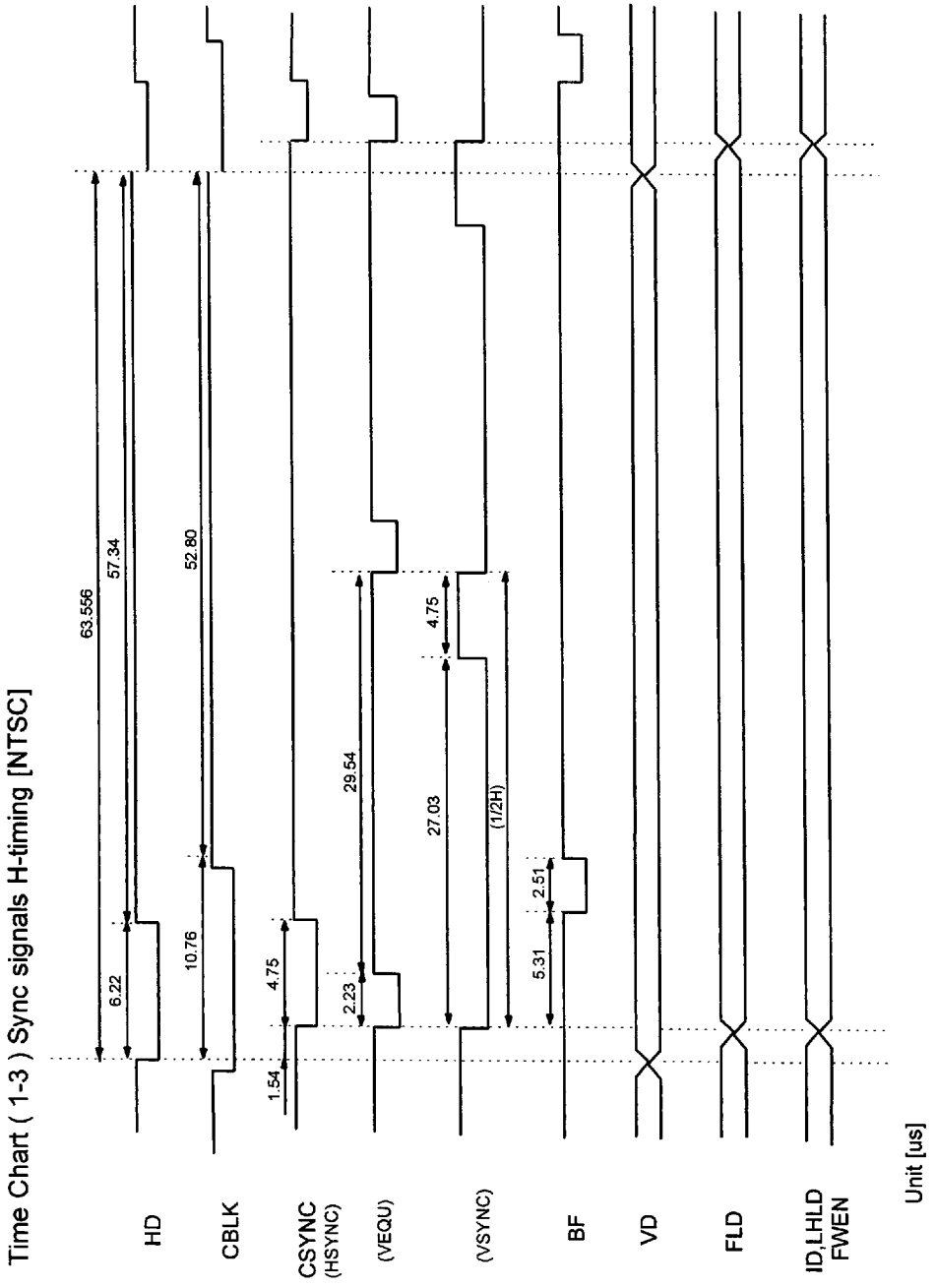


Time Chart (1-1) Sync signals V-timing [NTSC]

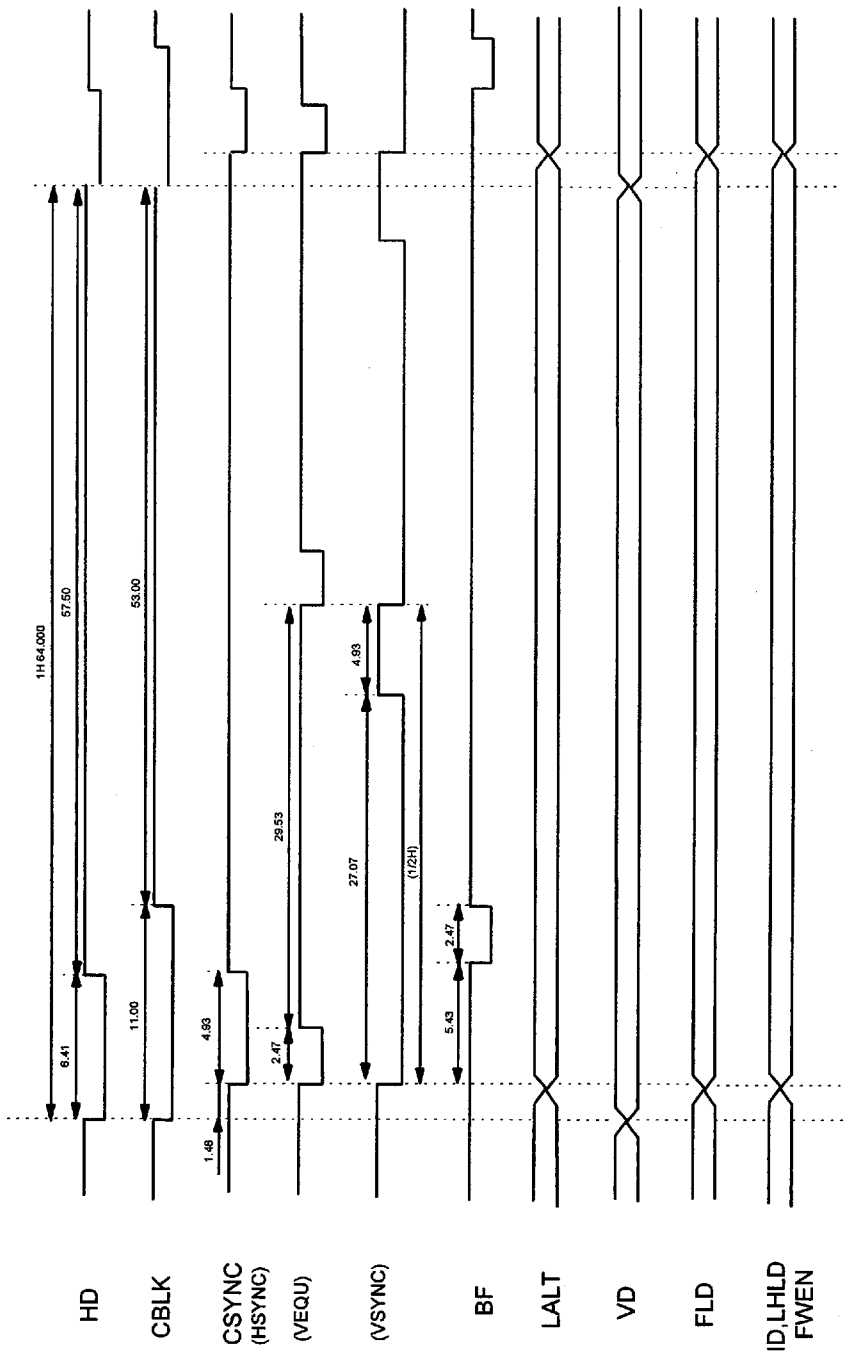


Time Chart (1-2) Sync signals V-timing [PAL]

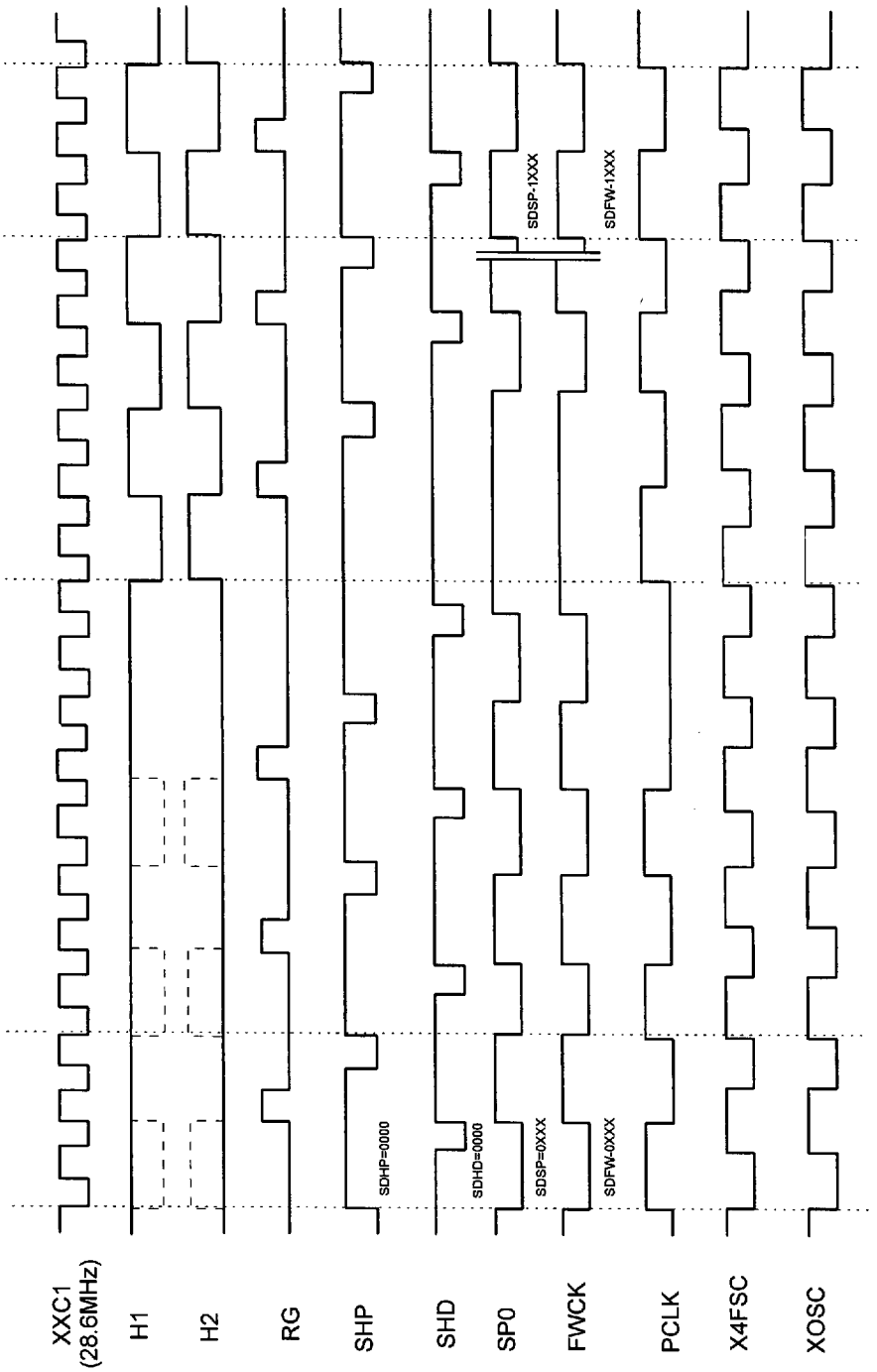




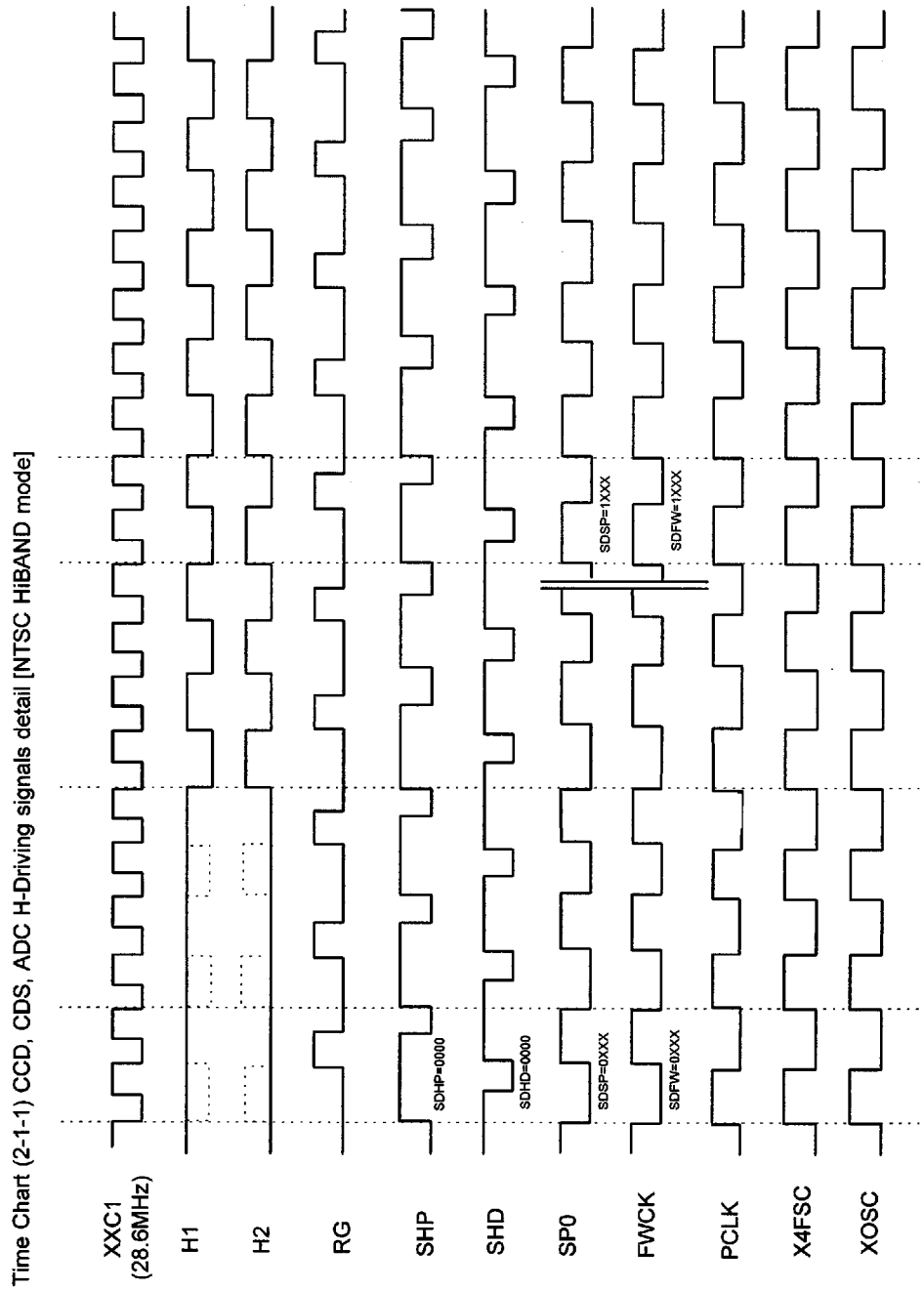
Time Chart (1-4) Sync signals H-timing [PAL]



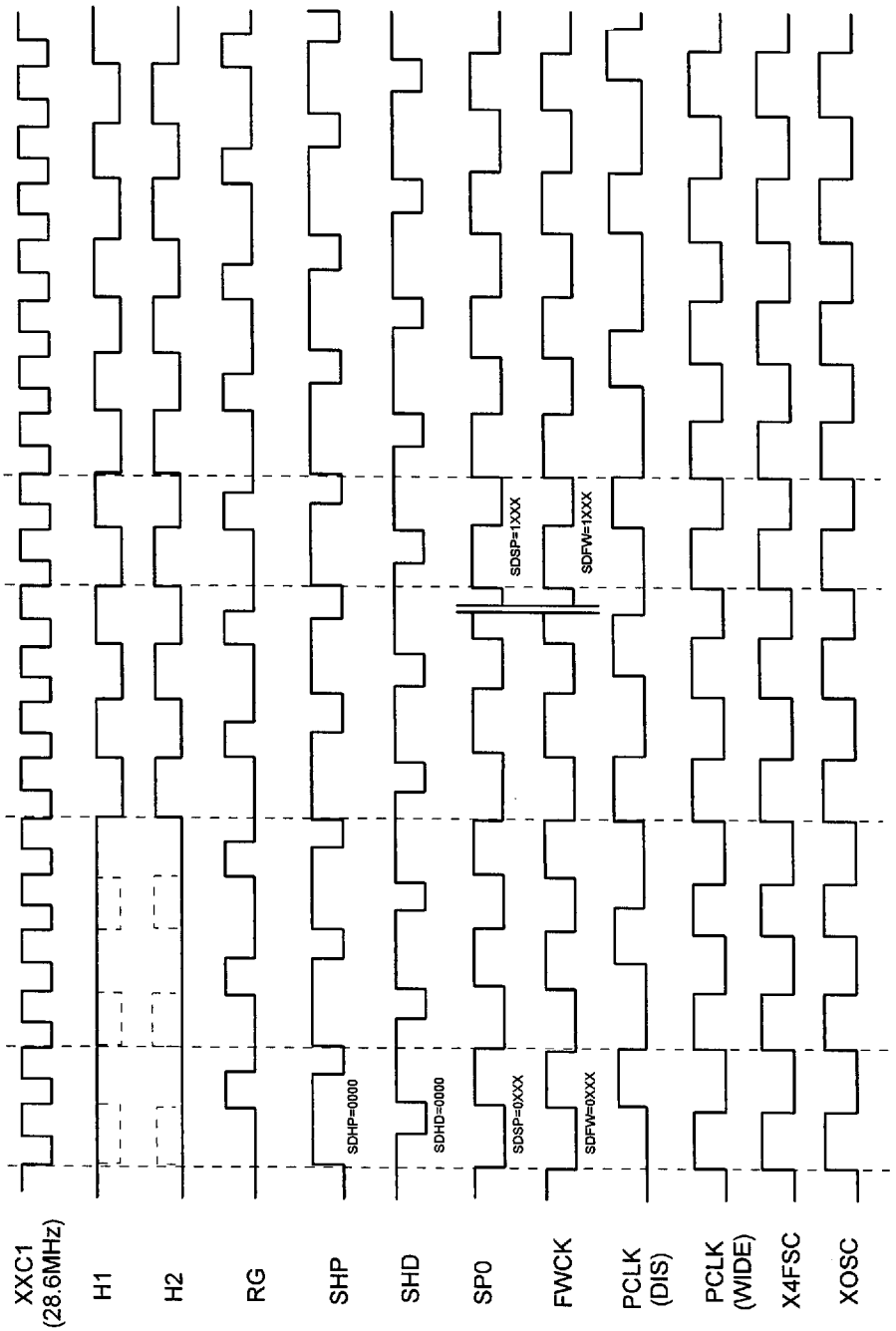
Time Chart (2-1-0) CCD, CDS, ADC H-Driving signals detail [NTSC NORMAL mode]



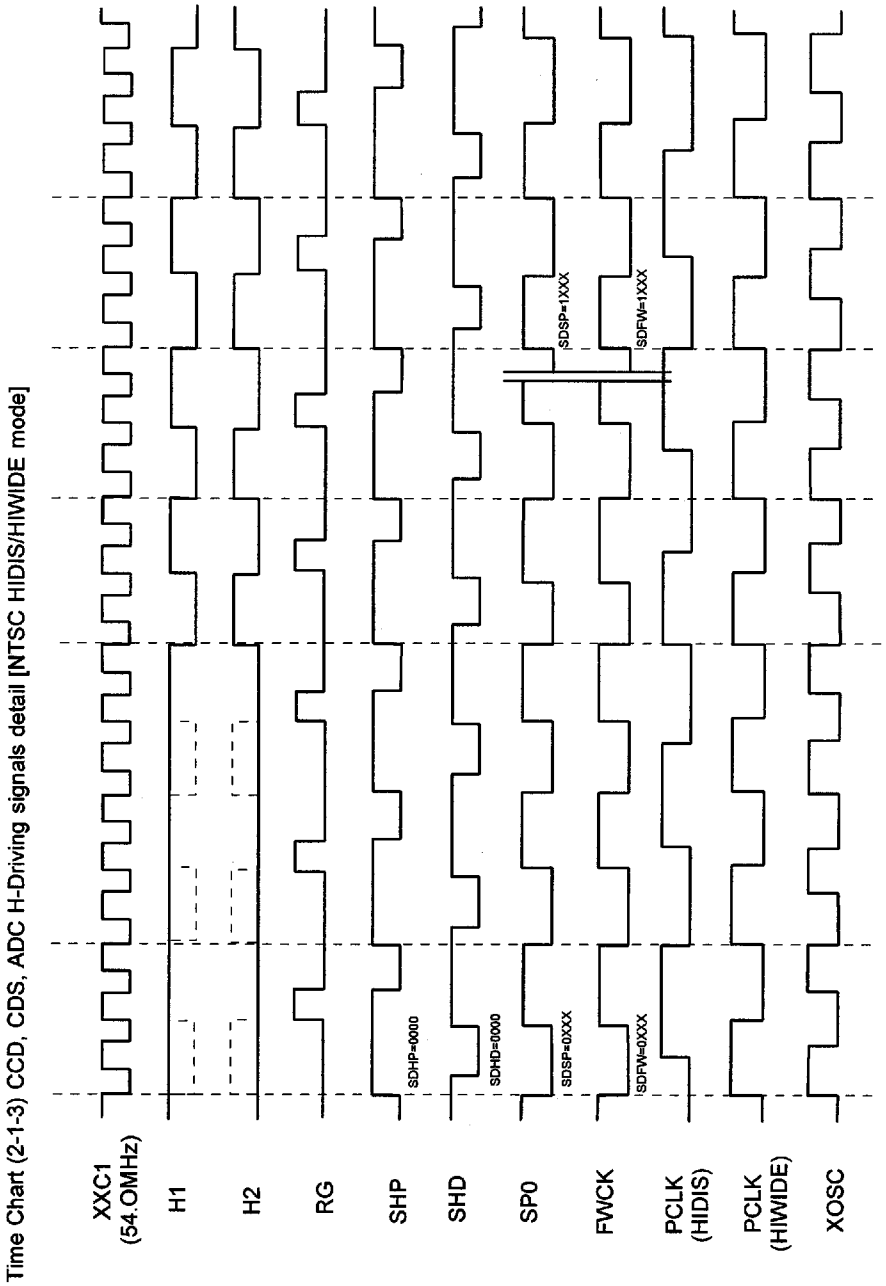
Time Chart (2-1-1) CCD, CDS, ADC H-Driving signals detail [NTSC HiBAND mode]



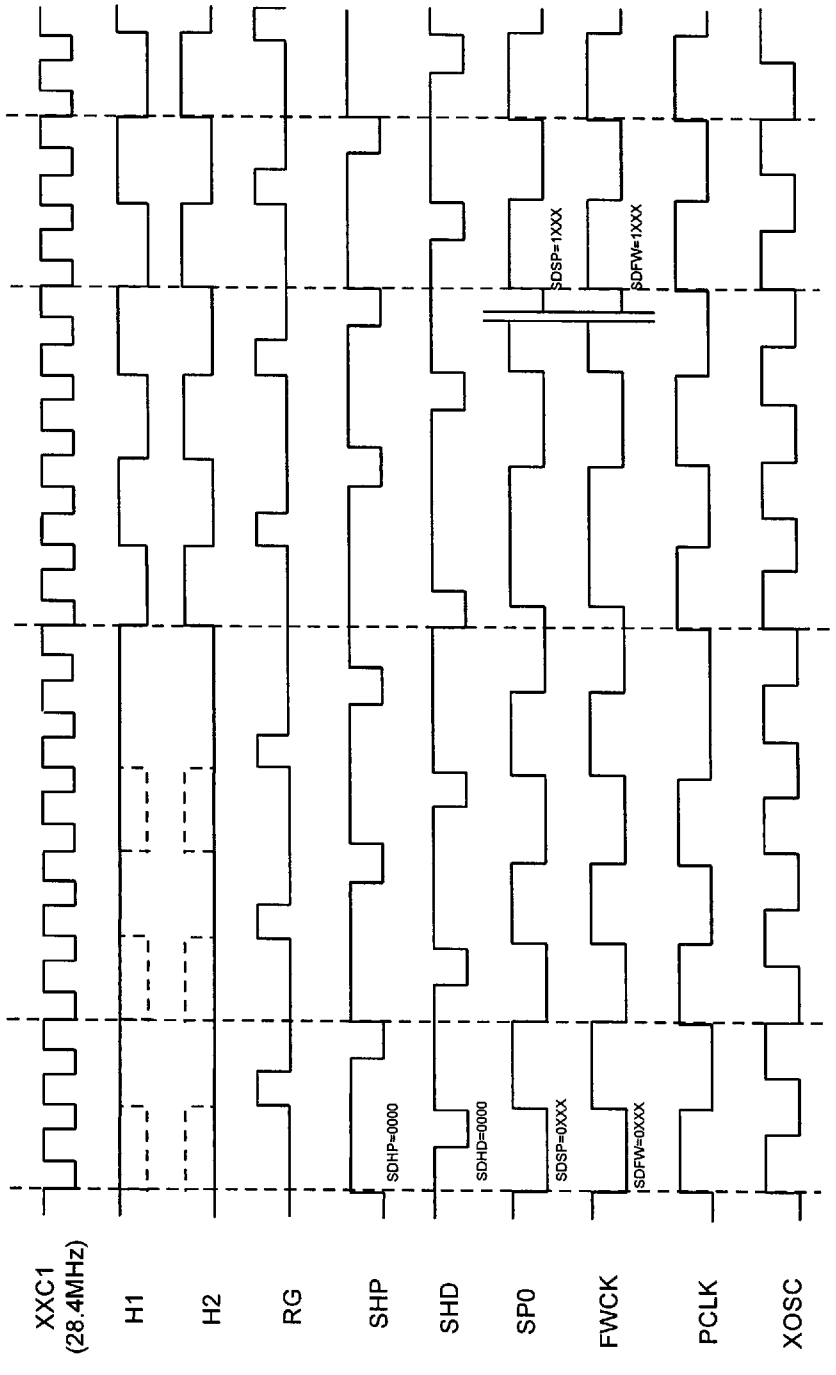
Time Chart (2-1-2) CCD, CDS, ADC H-Driving signals detail [NTSC DIS/WIDE mode]



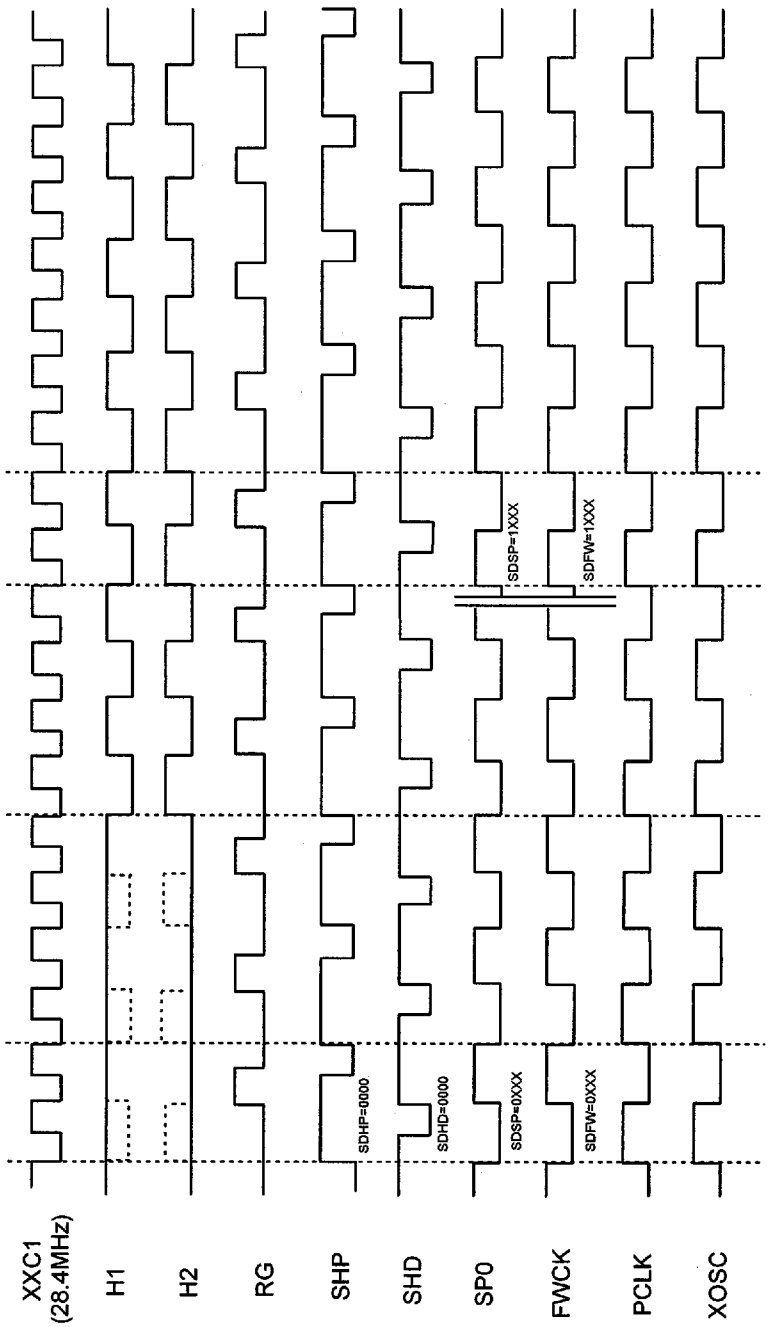
Time Chart (2-1-3) CCD, CDS, ADC H-Driving signals detail [NTSC HIDIS/HIWIDE mode]



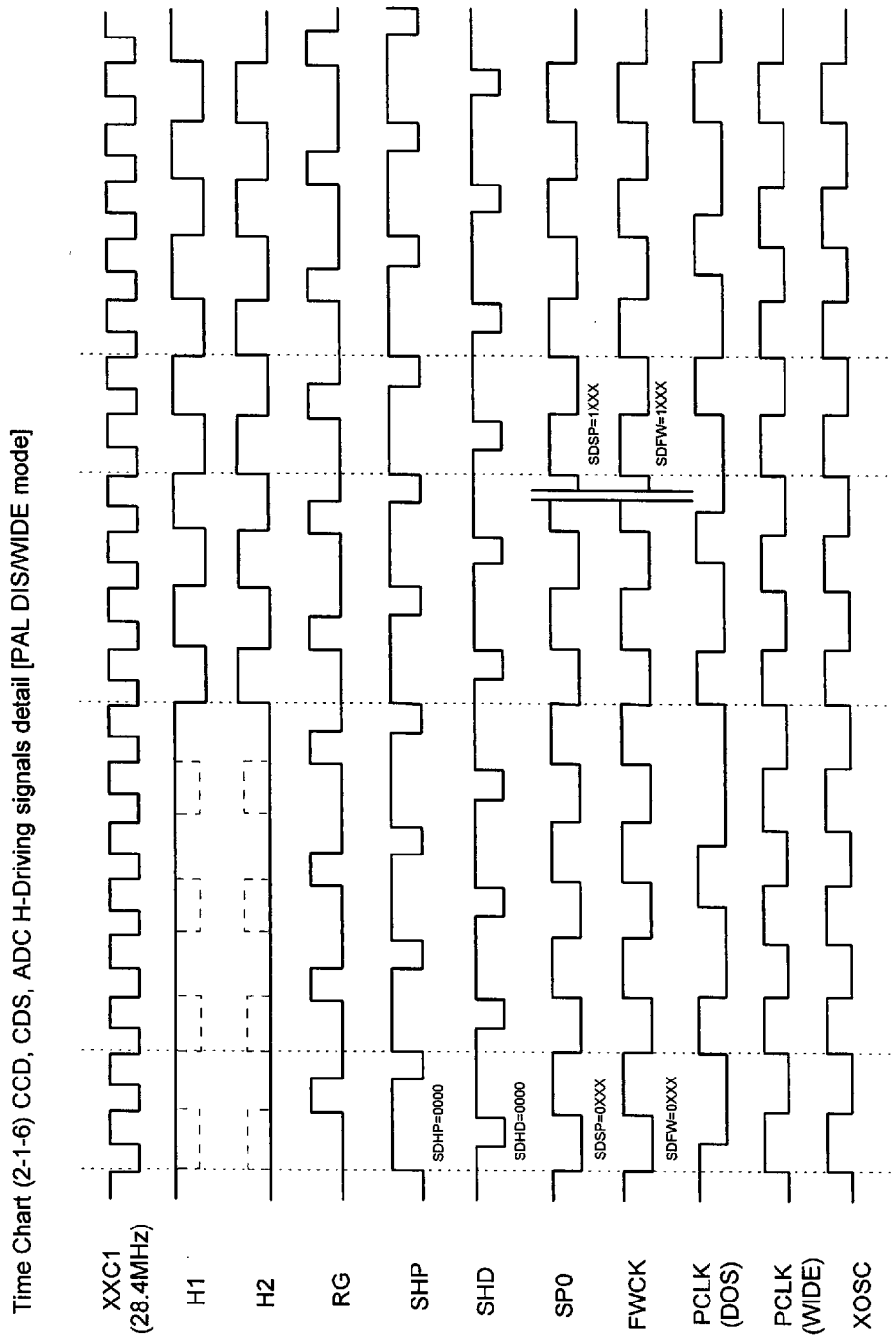
Time Chart (2-1-4) CCD, CDS, ADC H-Driving signals detail [PAL NORMAL mode]



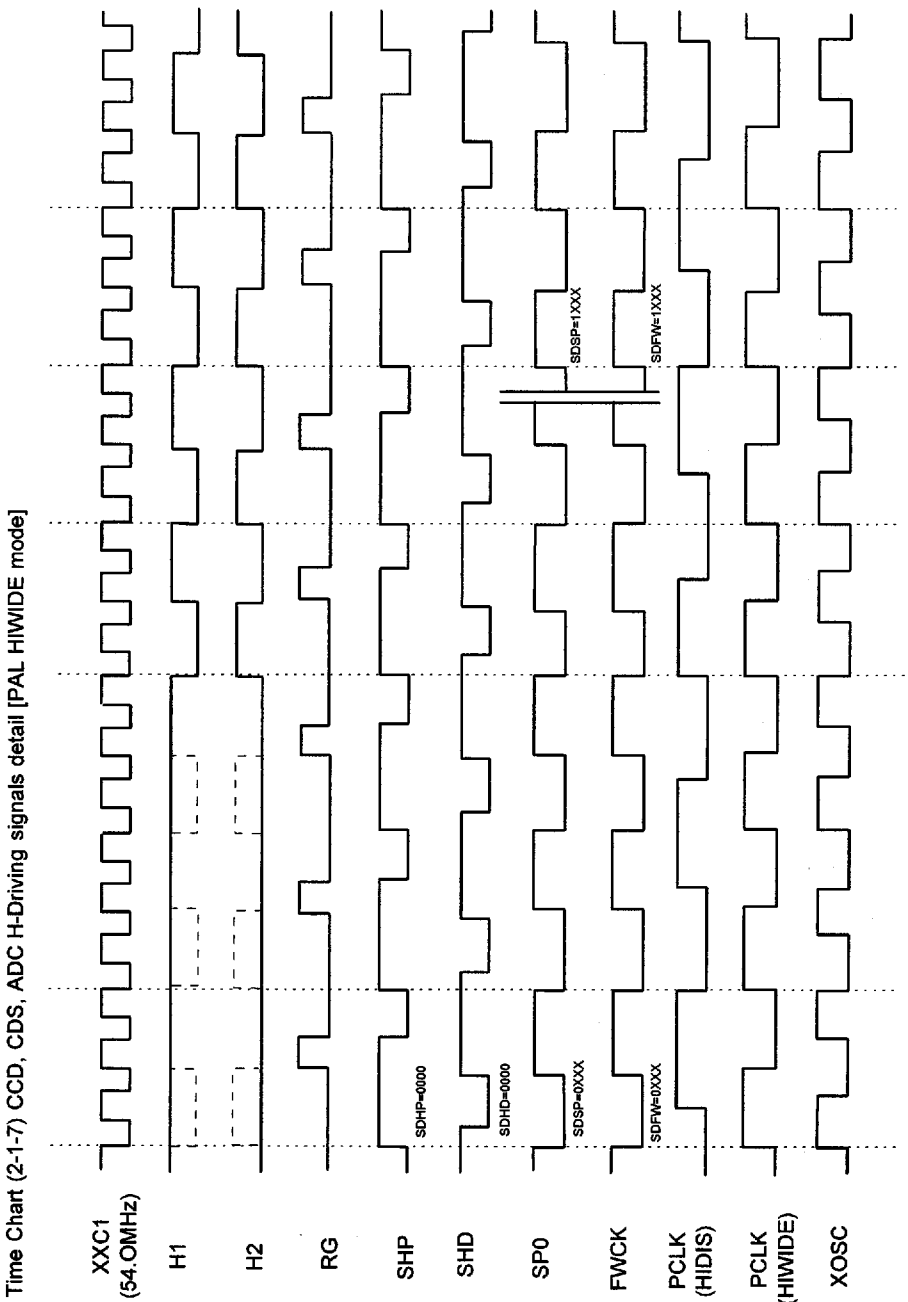
Time Chart (2-1-5) CCD, CDS, ADC H-Driving signals detail [PAL HiBAND mode]



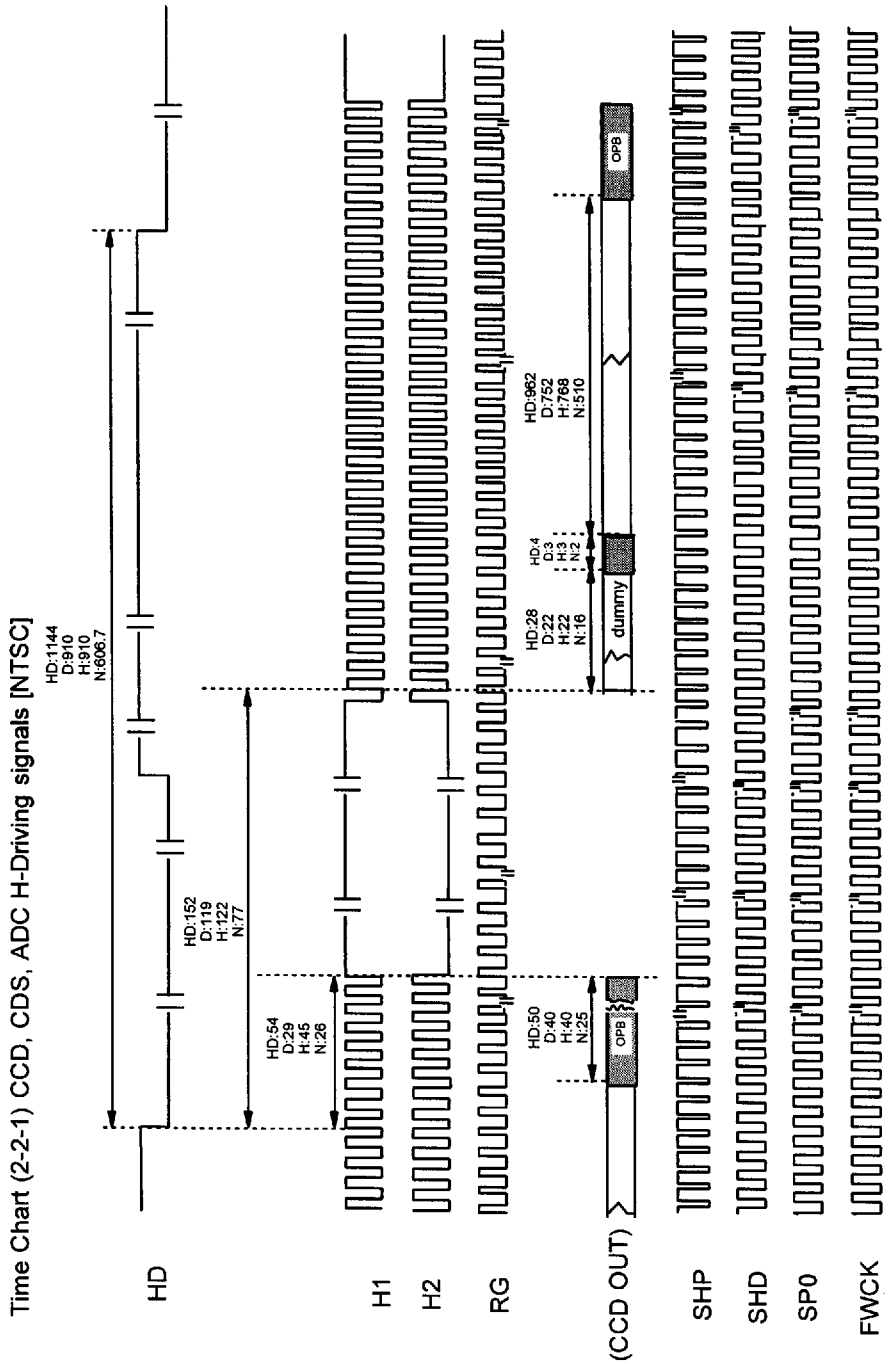
Time Chart (2-1-6) CCD, CDS, ADC H-Driving signals detail [PAL DIS/WIDE mode]

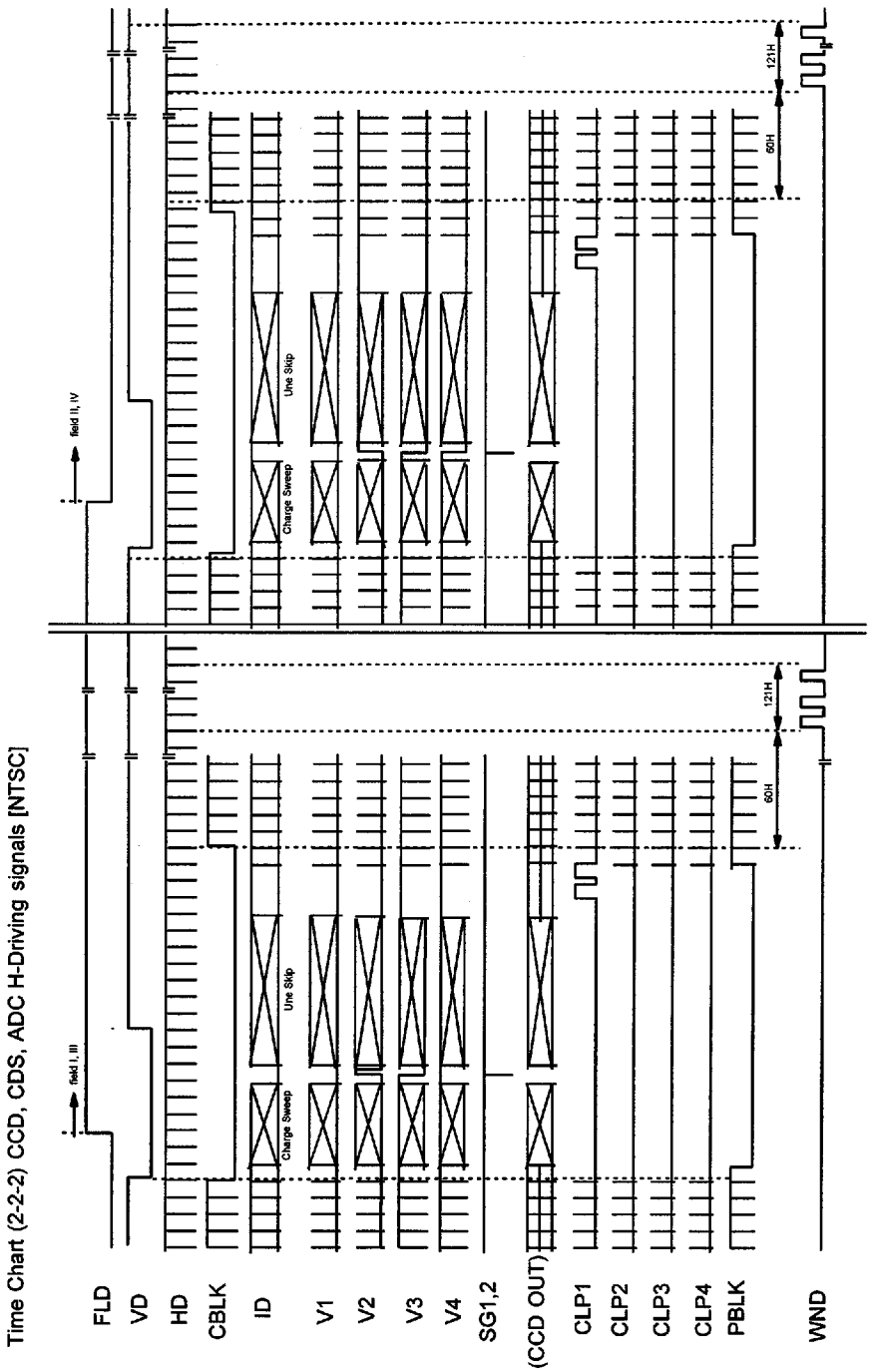


Time Chart (2-1-7) CCD, CDS, ADC H-Driving signals detail [PAL HIWIDE mode]

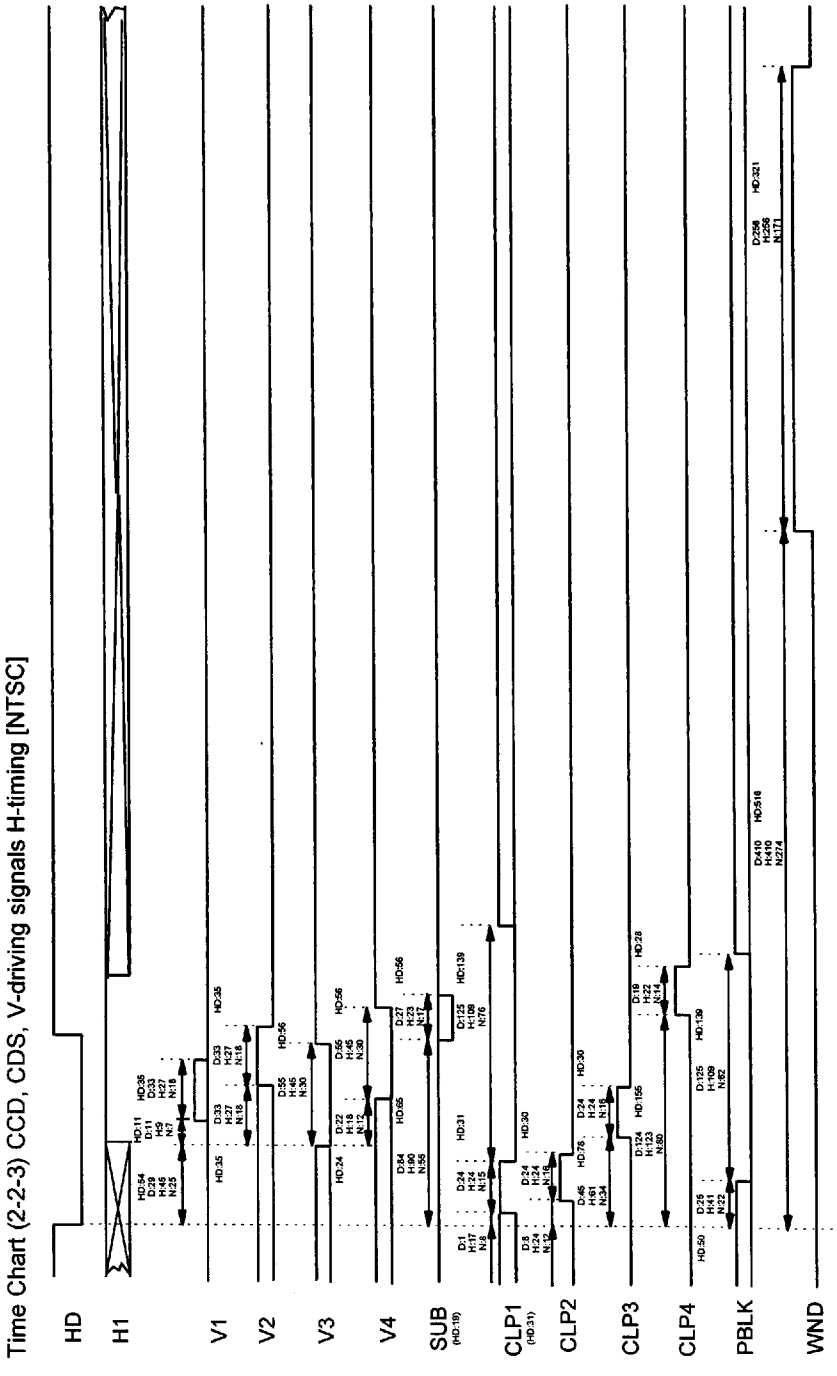


Time Chart (2-2-1) CCD, CDS, ADC H-Driving signals [NTSC]

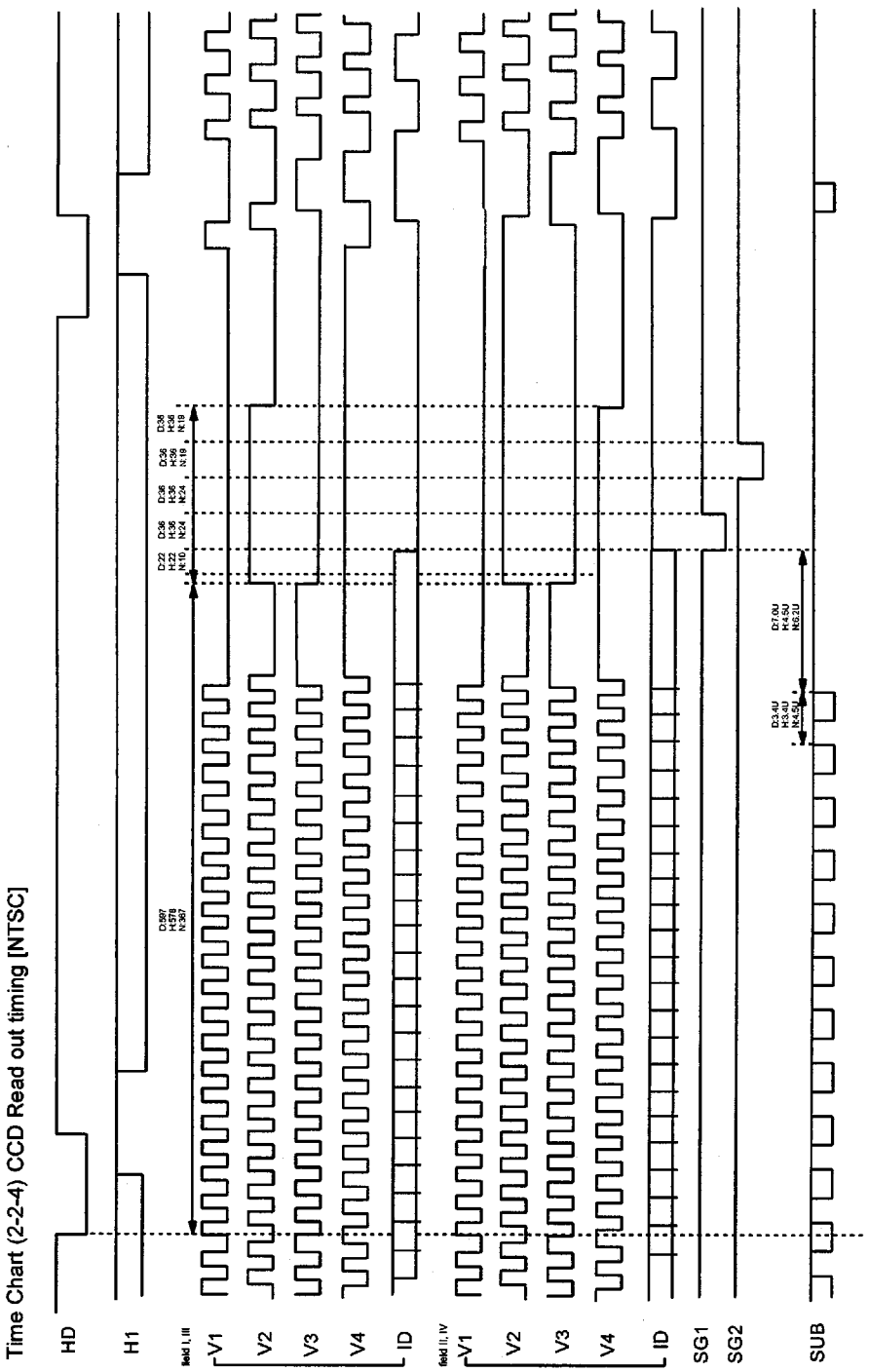




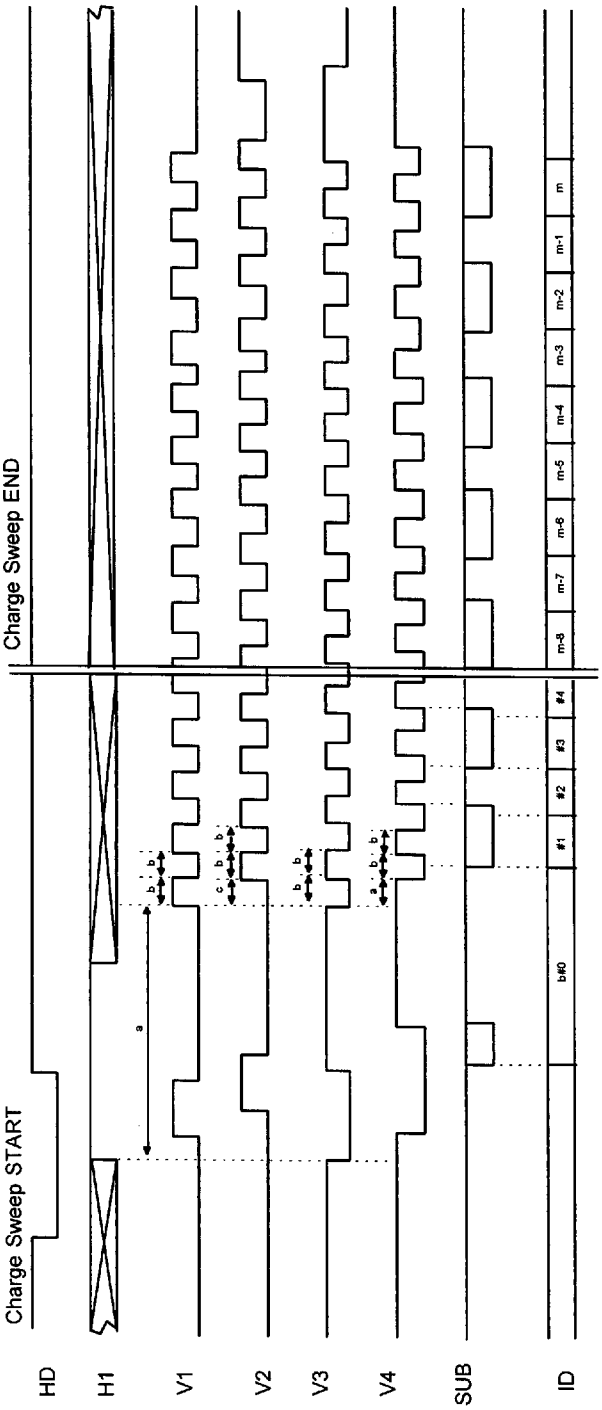
Time Chart (2-2-3) CCD, CDS, V-driving signals H-timing [NTSC]



HD:Number of CCD CLK at HIDIS mode.
D:Number of CCD CLK at DIS mode.
H:Number of CCD CLK at Hi-band mode.
N:Number of CCD CLK at Normal mode.

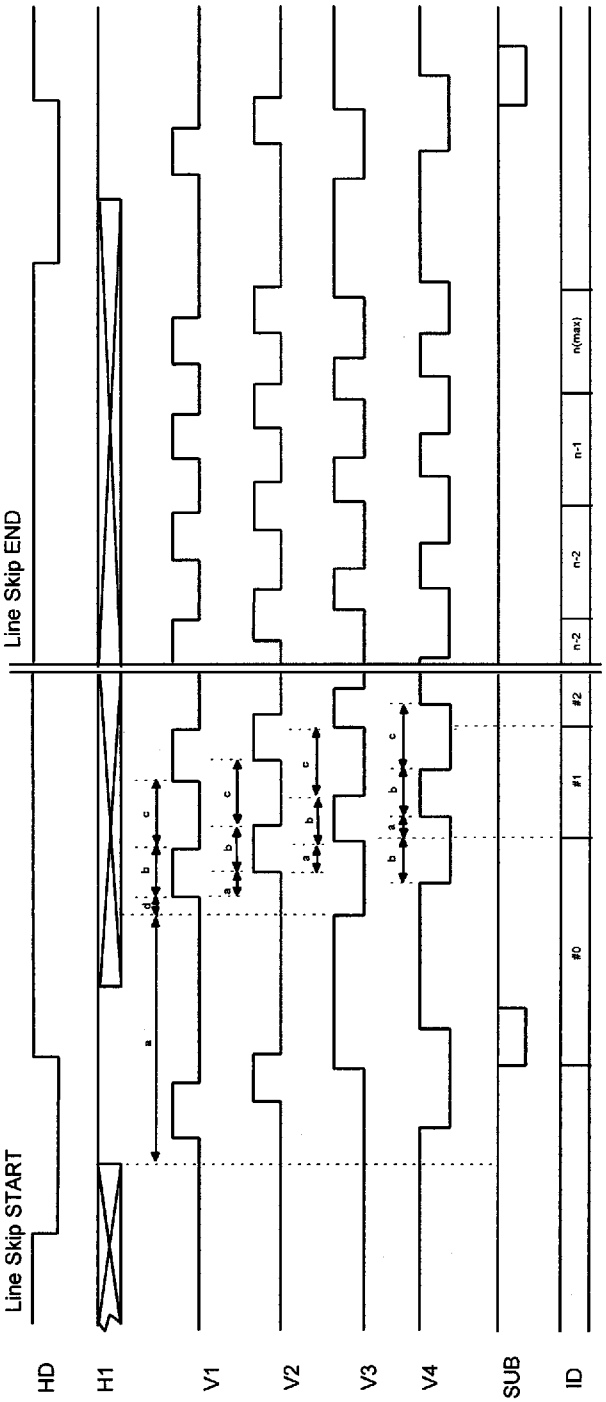


Time Chart (2-2-5) CCD Charge Sweep timing [NTSC]



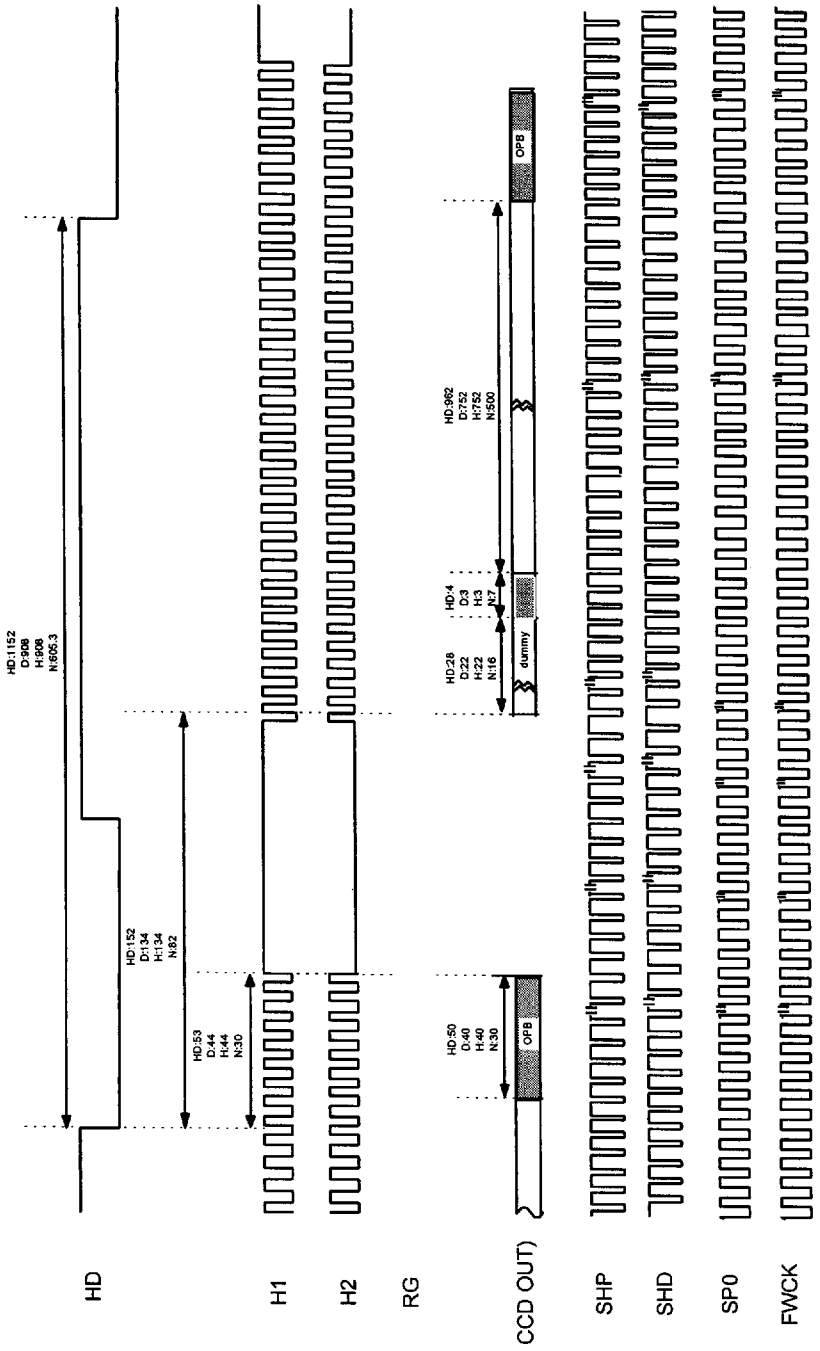
mode	a	b	c	n
NTSC NORMAL	6.50us	1.12us	0.56us	156
NTSC HIBAND	6.50us	1.12us	0.56us	154
NTSC DIS/WIDE	6.5ous	0.84us	0.42us	206
NTSC HIDIS/HIWIDE	6.07us	0.74us	0.37us	211

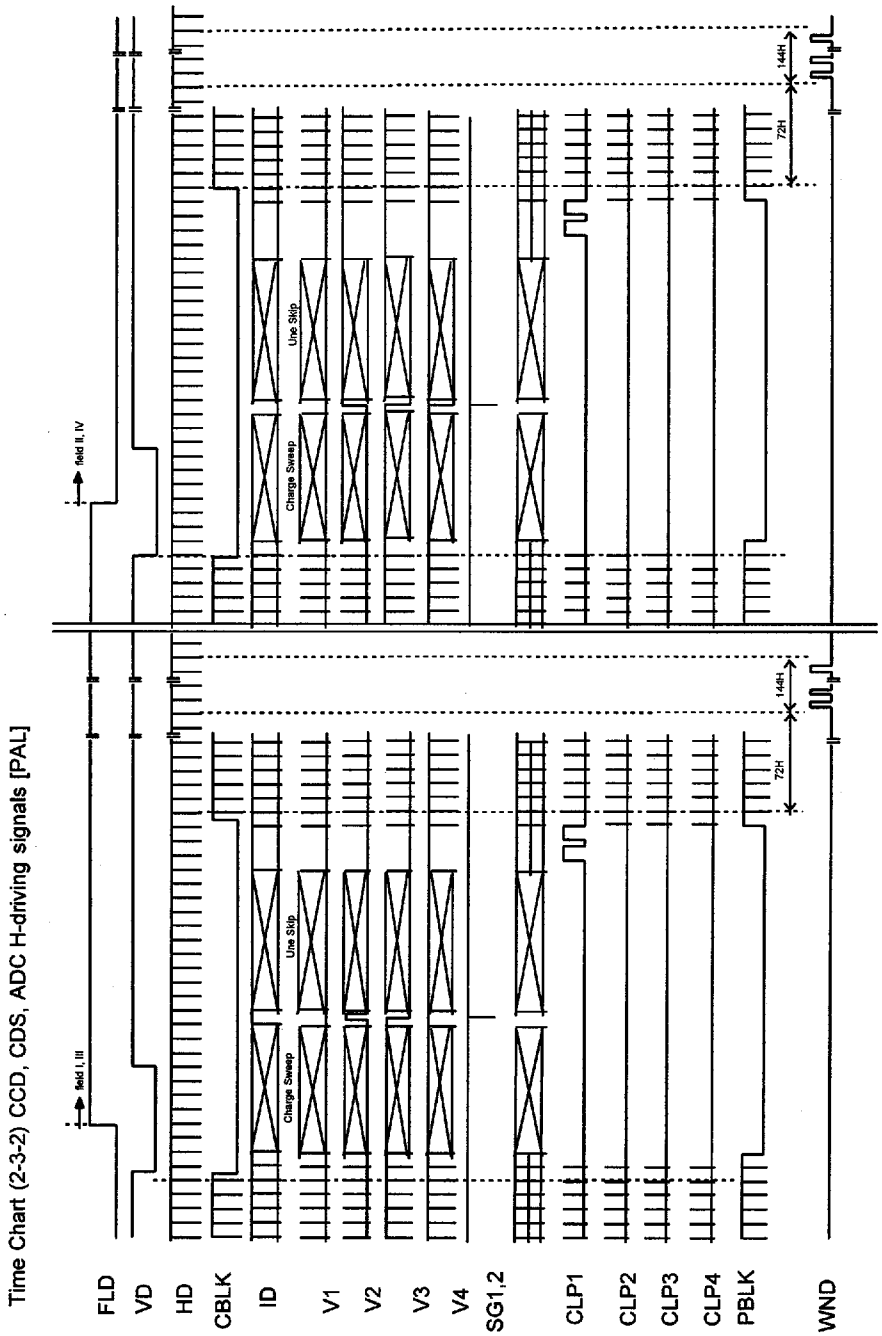
Time Chart (2-2-6) CCD Line Skip timing [NTSC]



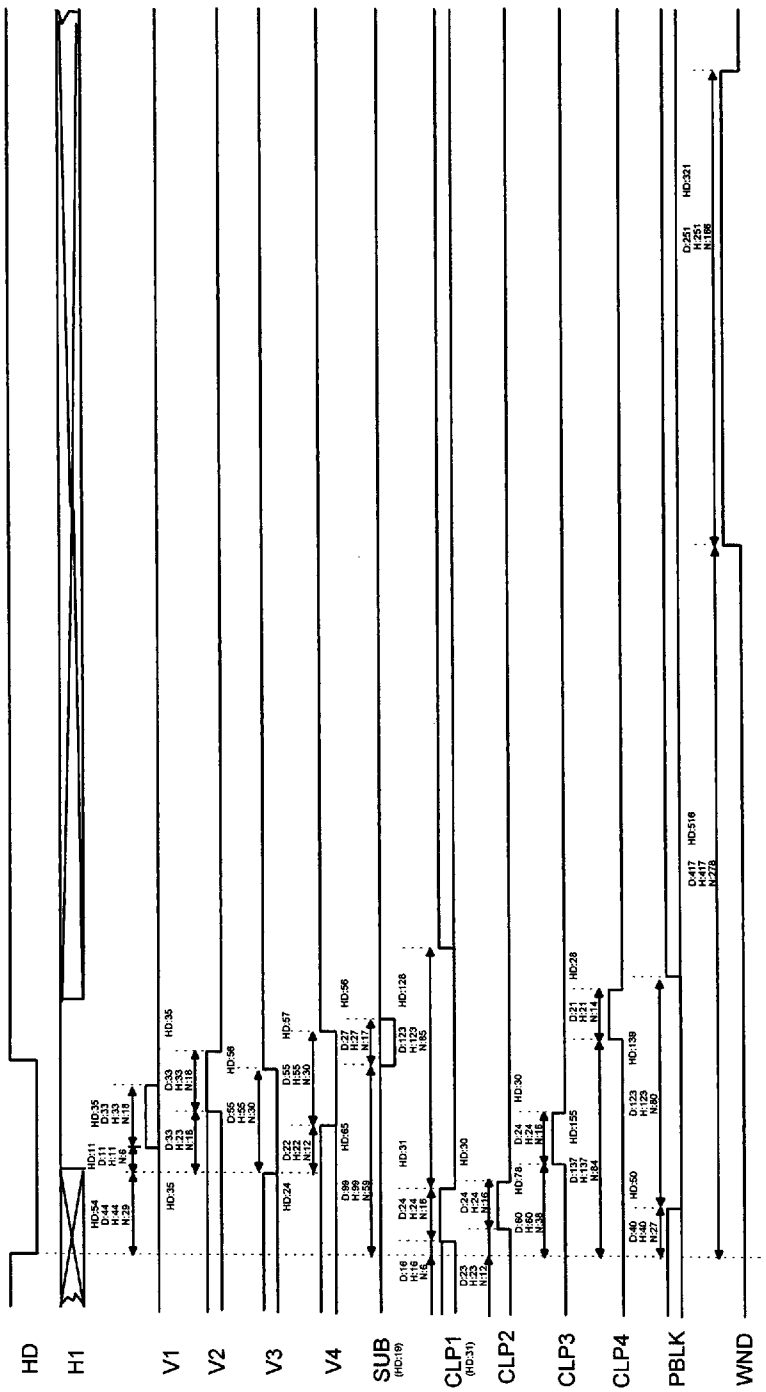
mode	a	b	c	d	e	n
NTSC NORMAL	6.50us	1.68us	2.79us	0.56us	c-b	125
NTSC HiBAND	6.50us	1.68us	2.79us	0.56us	c-b	126
NTSC DIS/WIDE	6.50us	1.26us	2.10us	0.42us	c-b	168
NTSC iDIS/HWIDE	6.07us	1.11us	1.185us	0.37us	c-b	191

Time Chart (2-3-1) CCD, CDS, ADC H-driving signals [PAL]

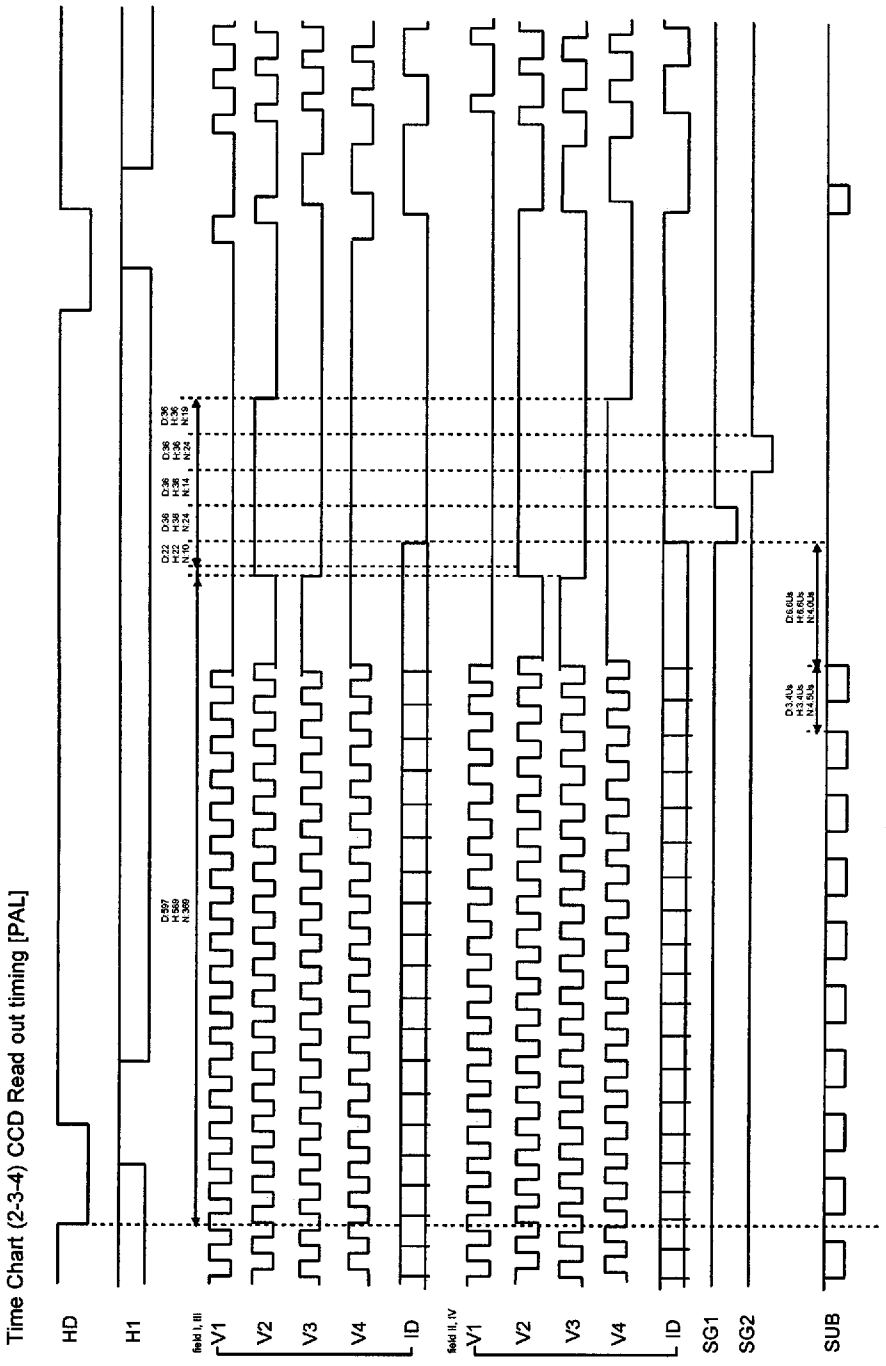




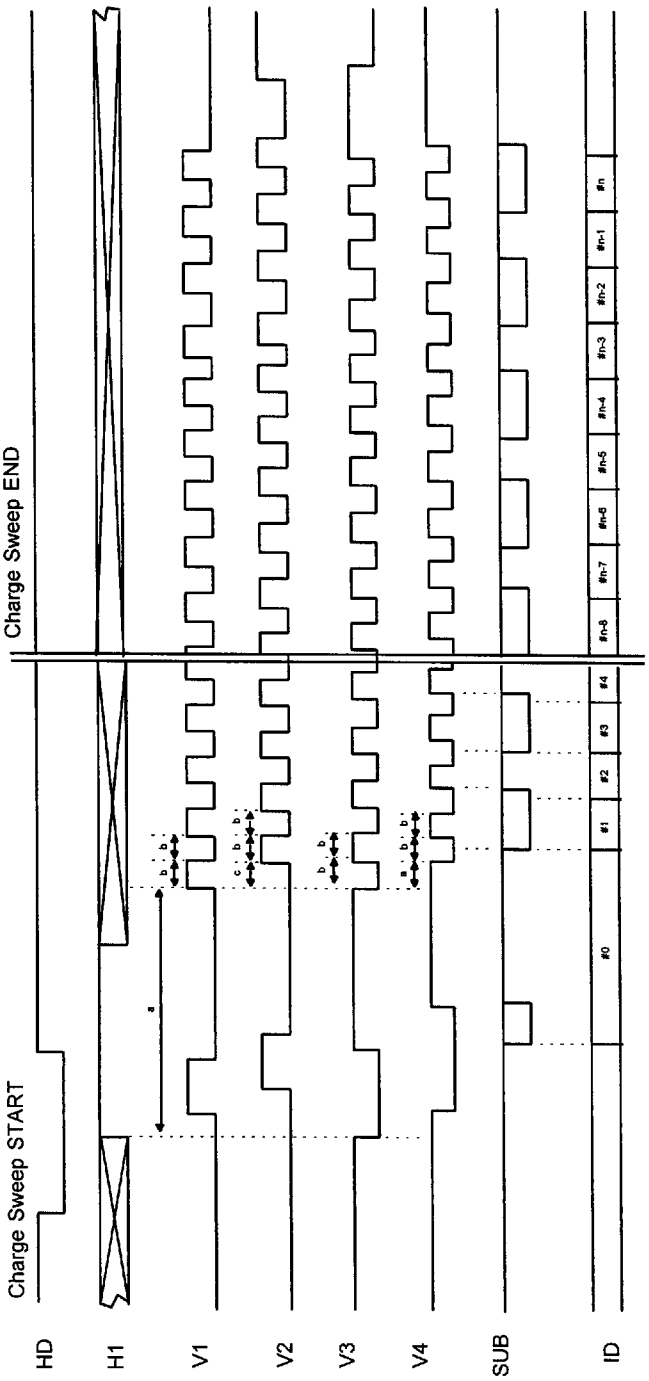
Time Chart (2-3-3) CCD, CDS, V-driving signals H-timing [PAL]



HD:Number of CCD CLK at HIDIS mode.
D:Number of CCD CLK at DIS mode.
H:Number of CCD CLK at Hi-band mode.
N:Number of CCD CLK at Normal mode.

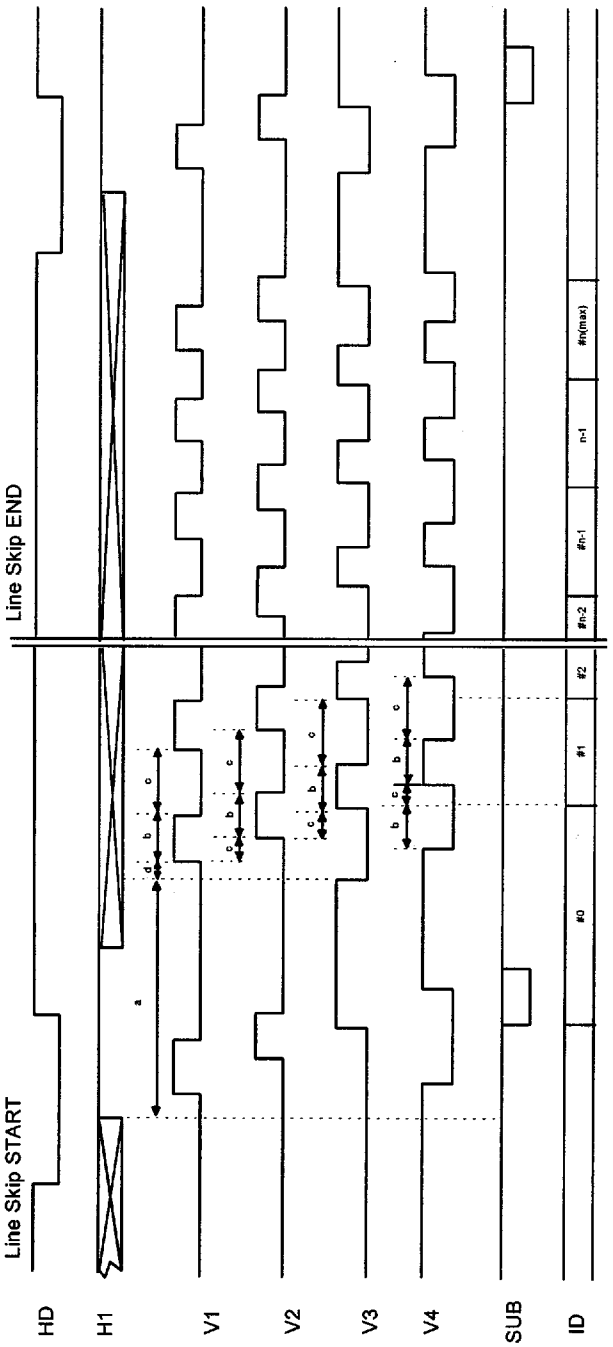


Time Chart (2-3-5) CCD Charge Sweep timing [PAL]



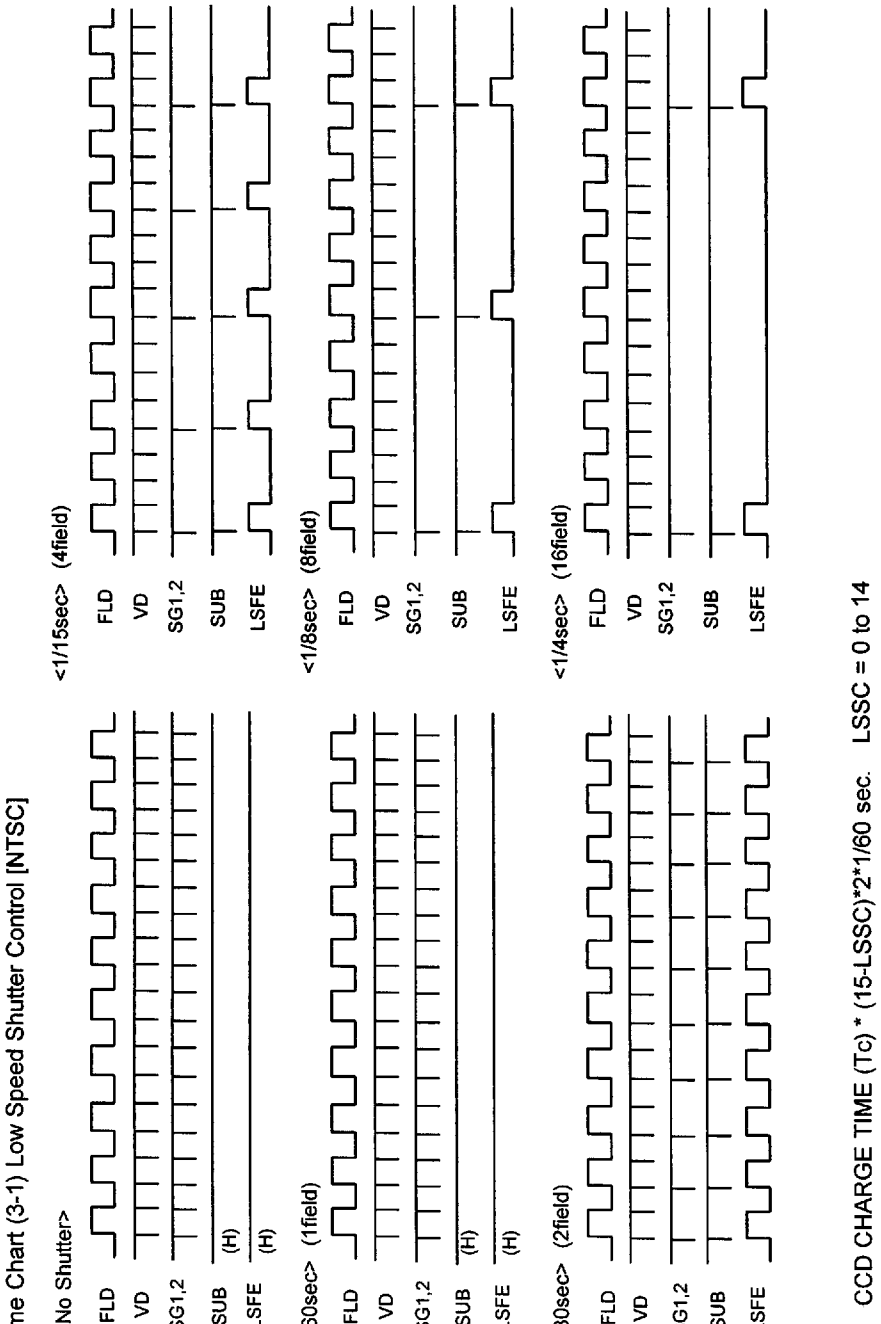
mode	a	b	c	n
PAL NORMAL	6.41us	1.13us	0.56us	260
PAL HIBAND	7.68us	1.13us	0.56us	268
PAL DIS/WIDE	7.68us	0.85us	0.42us	355
PAL HIDIS/HIWIDE	6.07us	0.74us	0.37us	387

Time Chart (2-3-6) CCD Line Skip timing [PAL]



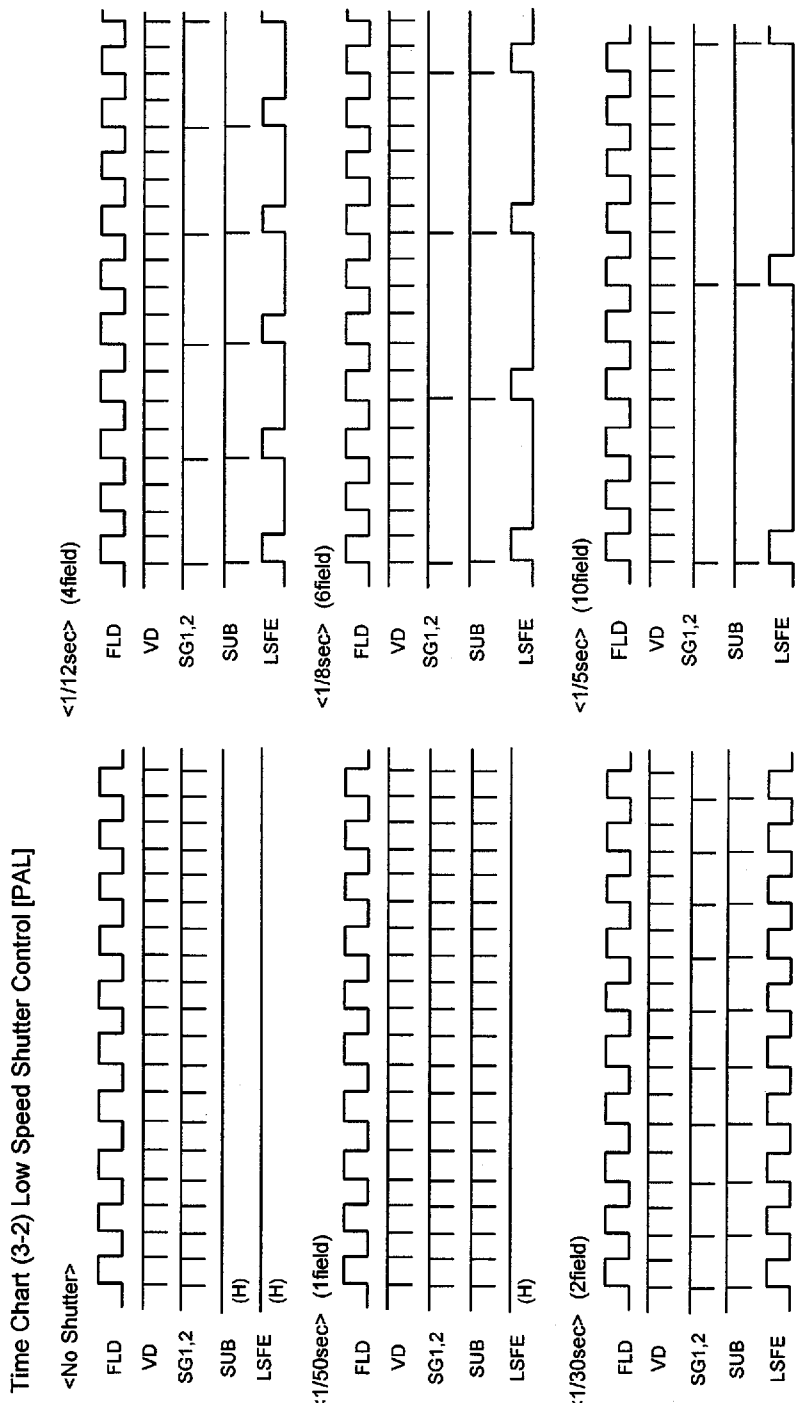
mode	a	b	c	d	e	n
PAL NORMAL	6.41us	1.69us	2.82us	0.56us	c-b	142
PAL HiBAND	7.68us	1.69us	2.82us	0.56us	c-b	139
PAL DIS/WIDE	7.68us	1.27us	2.11us	0.42us	c-b	186
PAL HIDIS/HiWIDE	6.07us	1.11us	1.85us	0.37us	c-b	213

Time Chart (3-1) Low Speed Shutter Control [NTSC]



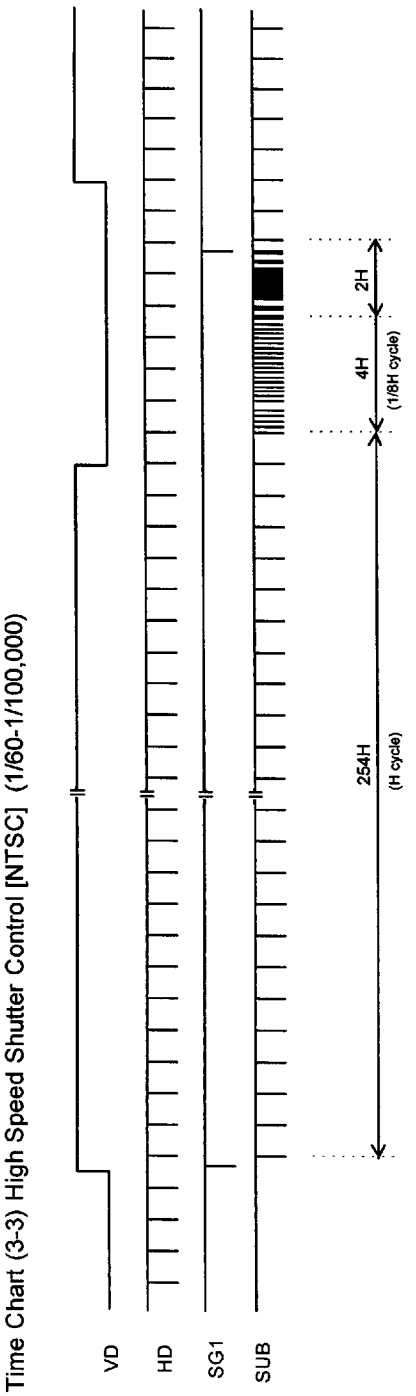
CCD CHARGE TIME (Tc) * (15-LSSC)*2*1/60 sec. LSSC = 0 to 14

Time Chart (3-2) Low Speed Shutter Control [PAL]



CCD CHARGE TIME (Tc) * (15-LSSC)*2*1/50 sec. LSSC = 0 to 14

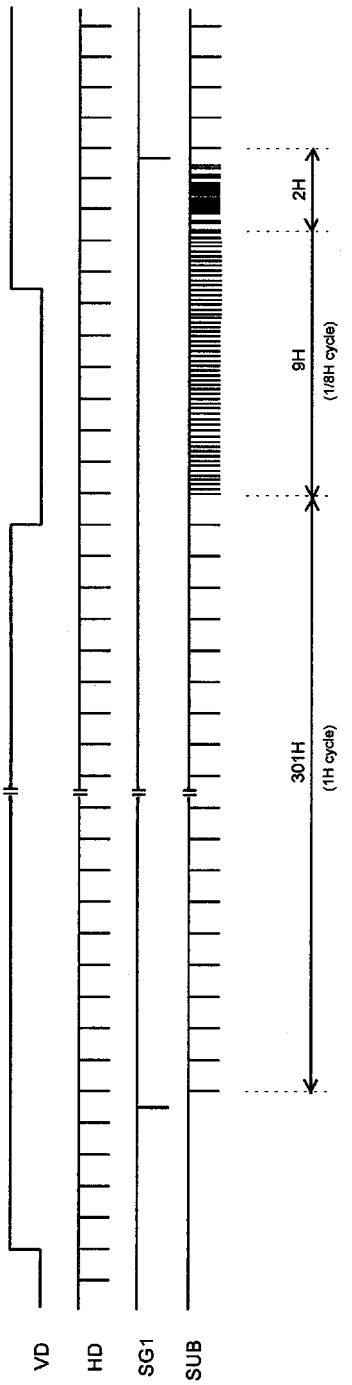
Time Chart (3-3) High Speed Shutter Control [NTSC] (1/60-1/100,000)



CCD CHARGE TIME (Tc)

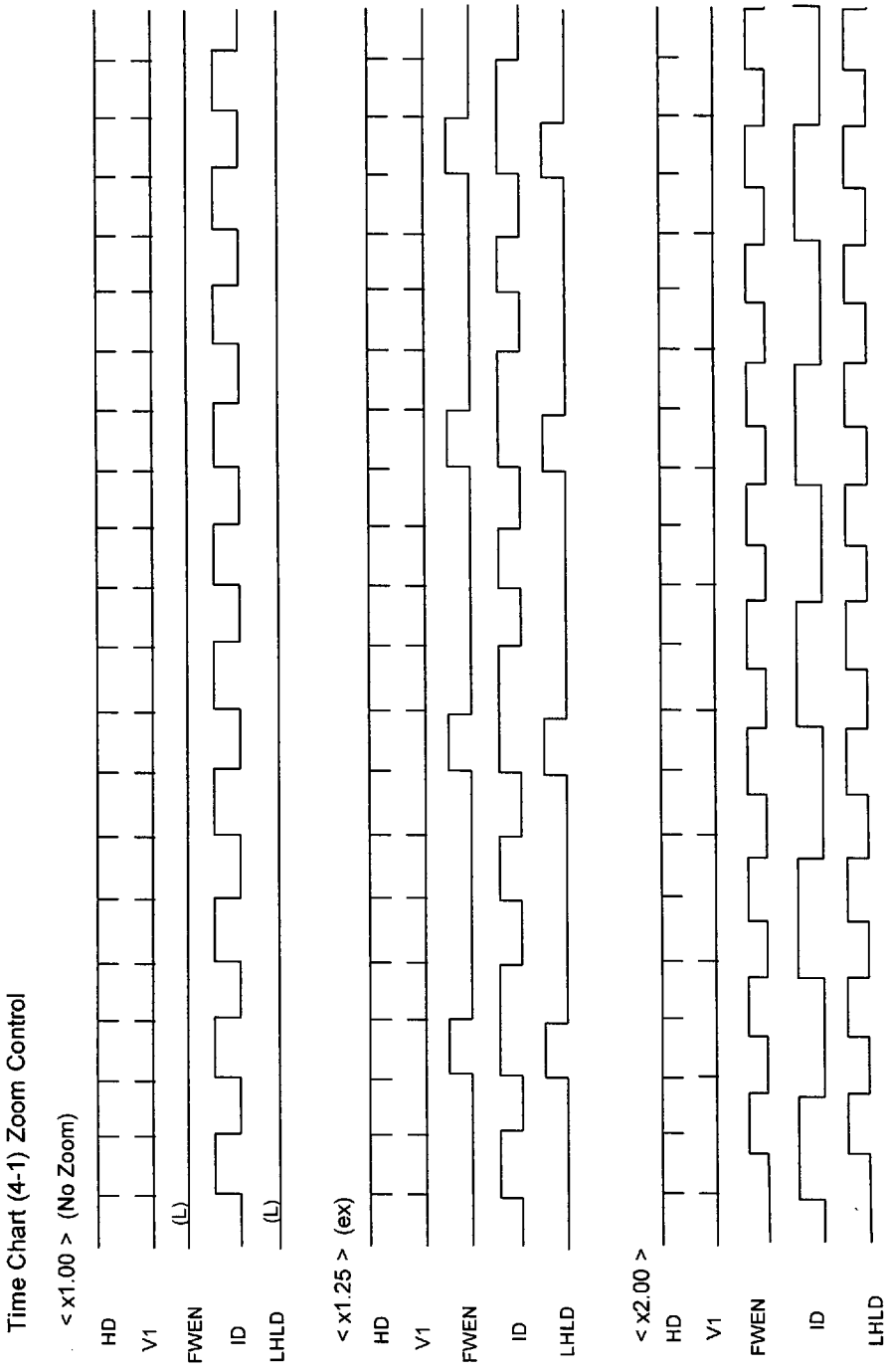
HSSC = 1023 ~ 769	: Tc = (HSSC-769)* 63.556us+359.10us (NORMAL) : Tc = (HSSC-769)*63.556us+362.31us (HIBAND) : Tc = (HSSC-769)*63.556us+361.39us(DIS/WIDE) : Tc = (HSSC-769)*63.556us+334.01us (HIDIS/HIWIDE)	(1/60 sec ~ 1/3000 sec)
HSSC = 768 ~ 736	: Tc = (HSSC-736)* 7.944us+96.943us (NORMAL) : Tc = (HSSC-736)*7.944us+100.156us (HIBAND) : Tc = (HSSC-736)*7.944us+99.234us(DIS/WIDE) : Tc = (HSSC-736)*7.944us+71.853us (HIDIS/HIWIDE)	(1/3000 sec ~ 1/10,000 sec)
HSSC + 735 ~	: Tc = (HSSC-716)* 4.470us+7.543us (NORMAL) : Tc = (HSSC-715)*4.470us+6.286us (HIBAND) : Tc = (HSSC-709)*3.352us+8.730us(DIS/WIDE) : Tc = (HSSC-714)*2.963us+6.667us (HIDIS/HIWIDE)	(1/10,000 sec ~ 1/100,000 sec)

Time Chart (3-4) High Speed Shutter Control [PAL] (1/50-1/100,000)



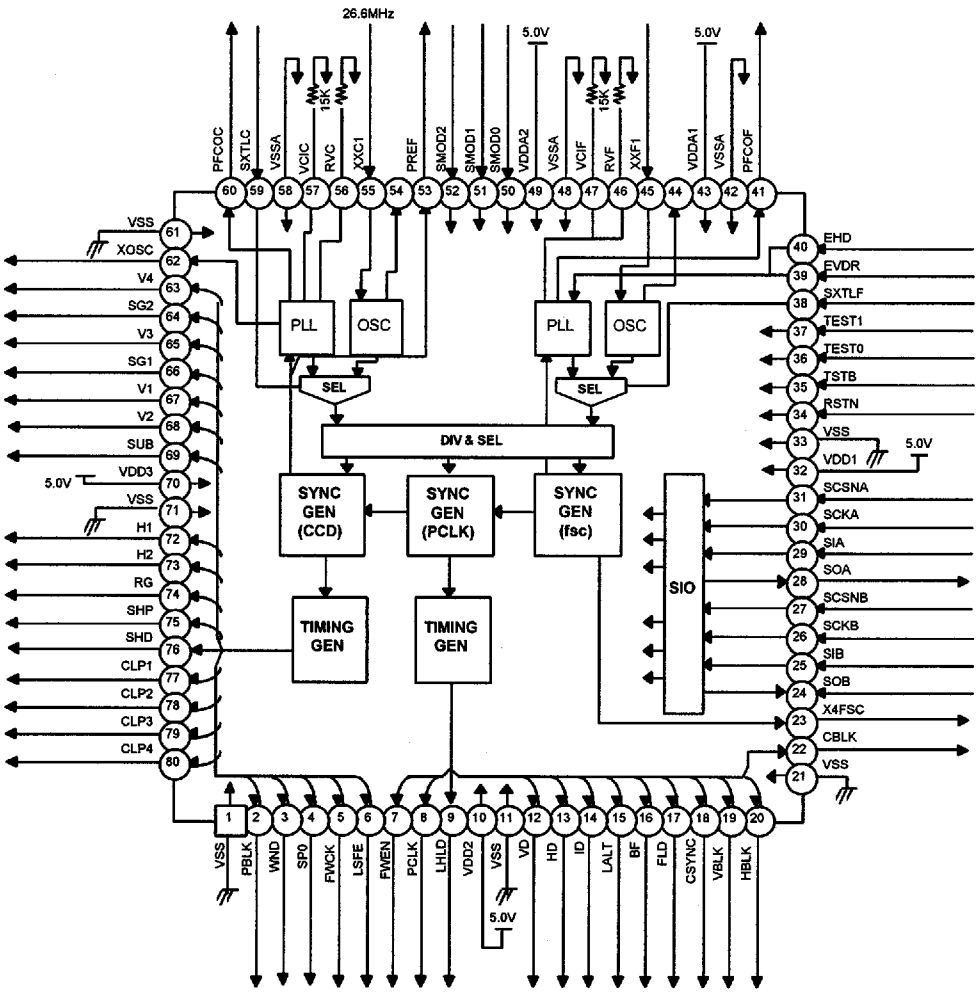
CCD CHARGE TIME (Tc)

HSSC = 1023 ~ 722	: Tc = (HSSC-722)* 64.000us+679.650us (NORMAL)	(1/50 sec ~ 1/15000 sec)
	: Tc = (HSSC-722)*64.000us+682.54us (HIBAND)	
	: Tc = (HSSC-722)*64.000us+683.66us(DIS/WIDE)	
	: Tc = (HSSC-722)*64.000us+655.78us (HIDIS/HIWIDE)	
HSSC = 721 ~ 649	: Tc = (HSSC-649)*8.000us+95.647us (NORMAL)	(1/1500 sec ~ 1/10,000 sec)
	: Tc = (HSSC-649)*8.000us+98.537us (HIBAND)	
	: Tc = (HSSC-649)*8.000us+99.658us (DIS/WIDE)	
	: Tc = (HSSC-649)*8.000us+71.779us (HIDIS/HIWIDE)	
HSSC + 648 ~	: Tc = (HSSC-629)*4.511us+5.427us (NORMAL)	(1/10,000 sec ~ 1/100,000 sec)
	: Tc = (HSSC-629)*4.511us+8.317us (HIBAND)	
	: Tc = (HSSC-622)*3.383us+8.317us(DIS/WIDE)	
	: Tc = (HSSC-627)*2.963us+6.593us (HIDIS/HIWIDE)	

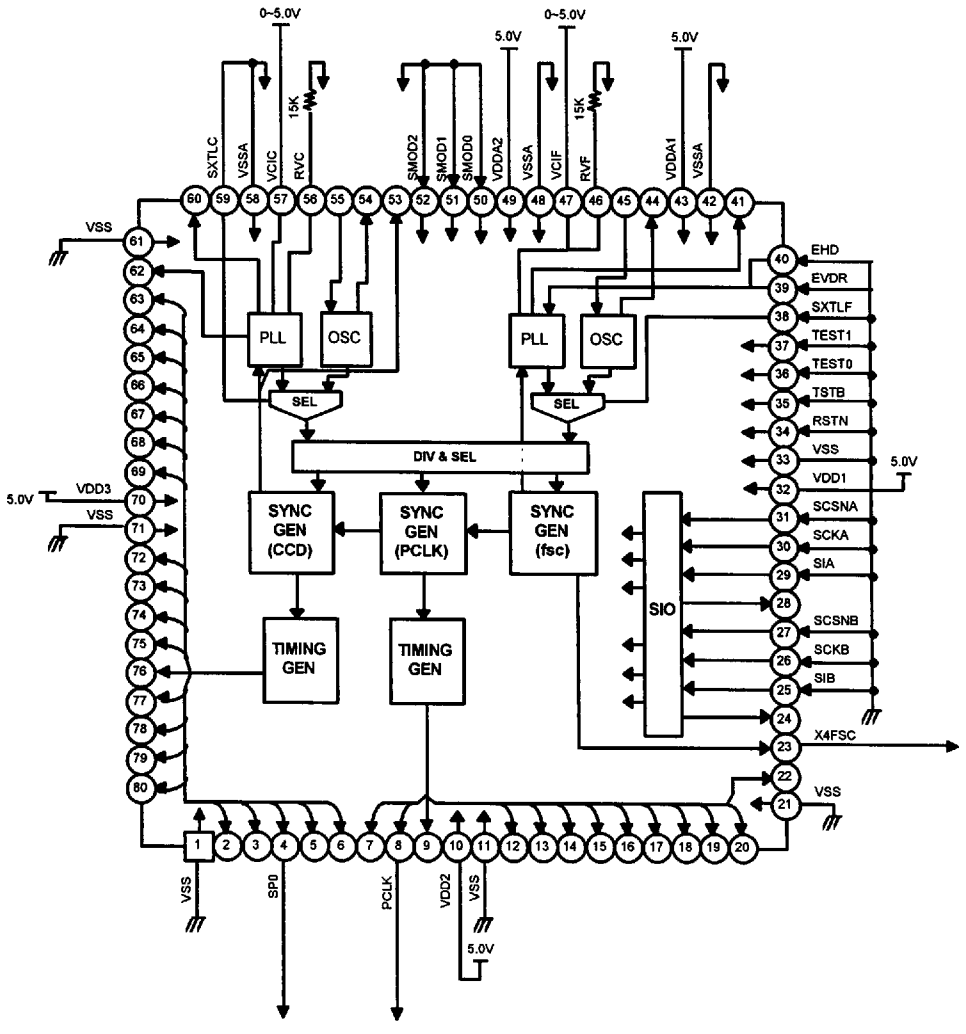


TEST CIRCUITS

(a) LOGIC TEST CIRCUIT



(b) VCO TEST CIRCUIT



PACKAGE DIMENSION

80 - QFP - 1212

unit: mm