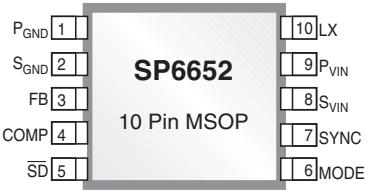
1A, High Efficiency, High Frequency Current Mode PWM Buck Regulator

FEATURES

- 1A Output Current
- 1.2MHz Constant Frequency Operation
- 97% Efficiency Possible
- Pin Selectable Forced PWM or PWM/PFM Modes
- Ultra Low Quiecent Current in PFM Mode: 50μA
- 500nA (Max.) Shutdown Current
- Output Adjustable Down to 0.75V
- No External FET's or Schottky Diode Required
- Uses Small Value Inductors and Ceramic Output Capacitors
- Low Dropout Operation: 100% Duty Cycle
- Soft Start and Thermal Shutdown Protection
- Easy Frequency Synchonization
- Small 10 Pin MSOP and 10 Pin DFN Package



Now Available in Lead Free Packaging

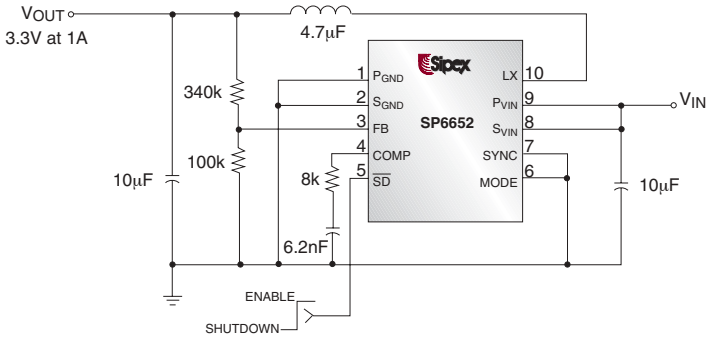
APPLICATIONS

- Mobile Phones
- PDA's
- DSC's
- MP3 Players
- USB Devices
- Point of Use Power

DESCRIPTION

The SP6652 is high efficiency, synchronous buck regulator ideal for portable applications using one Li-Ion cell, with up to 1A output current. The 1.2MHz switching frequency and PWM control loop are optimized for small value inductor and ceramic output capacitor, for space constrained portable designs. At light load, the SP6652 can operate in either PFM mode for high efficiency, or PWM mode for constant frequency. In addition, the input voltage range of 2.7V to 5.5V; excellent transient response, output accuracy, and ability to transition into 100% duty cycle operation, further extending useful battery life, make the SP6652 a superior choice for a wide range of portable power applications. The output voltage is externally programmable down to 0.75V. A logic level shutdown control, external clock synchronization, and forced-PWM or automatic control inputs are provided. Other features include soft-start, over current protection and 140(C over-temperature shutdown.

TYPICAL APPLICATION SCHEMATIC



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ABSOLUTE MAXIMUM RATINGS

PV_{IN},S_{VIN} ..... -0.3V to 0.3V
P_{GND} to S_{GND} ..... -0.3V to 0.3V
LX to P_{GND} ..... - 0.3V to P_{VIN}+0.3V
Storage Temperature ..... -65 °C to 150 °C
Operating Temperature ..... -40°C to +85°C
Lead Temperature (Soldering, 10 sec) ..... 300 °C

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ELECTRICAL CHARACTERISTICS

V_{IN}=UV_{IN}=V_{SDN}=3.6V, V_{OUT}=V_{FB}, I_O = 0mA, T_{AMB} = -40°C to +85°C, typical values at 27°C unless otherwise noted.

PARAMETER	MIN	TYP	MAX	UNITS		CONDITIONS
Input Voltage Operating Range	UVLO		5.5	V		
FB Set Voltage	0.735	0.75	0.765	V		T_A = 27°C, FB = COMP
FB Input Voltage	-1	0.01	1	µA		V_{FB} = 0.8V
Overall FB Accuracy	-4		4	%		FB = COMP
FB Set Voltage (PFM Mode)		0.758		V		
Switching Frequency	1	1.2	1.4	MHz		
SYNC Tracking Frequency	1	1.2	1.4	MHz		
SYNC Input Current	-1	0.01	1	µA		
SYNC Logic Threshold Low		0.3	0.6	Ω		
SYNC Logic Threshold High	1.7					
PWM On-Time Blanking		50		ns		
PMOS Switch Resistance		0.25	0.6	Ω		
NMOS Switch Resistance		0.25	0.6	Ω		
Inductor Current Limit (PWM Mode)	1.2	1.4	1.6	A		
Inductor Current Limit (PFM Mode)		300		mA		
LX Leakage Current		0.1	3	µA		SD\=0V
S_{VIN} Quiecent Current		60	100	µA		PFM Mode
		2	TBD	nA		PWM Mode
		1	500	mA		Shutdown, SD\=0V
P_{VIN} Quiecent Current		102	TBD	µA		V_{COMP} = 0.6V I_{LX} = 0
		1	500			PWM Mode
UVLO Undervoltage Lockout Threshold, V_{IN} falling	2.6	2.7	2.8	V		
UVLO hysteresis		6		%		
Soft Start Current	1	2	3	µV		V_{COMP} = 1V
SD\, MODE Input Current	-1	0.01	1	µA		
SD\, MODE Logic Threshold Low			0.4	V		
SD\, MODE Logic Threshold High	1.6			V		
Slope Compensation		700		mA/µs		
Rising Over-Temperature Trip Point		140		°C		
Over-Temperature Hysteresis		14		°C		
ERROR AMPLIFIER						
Error Amplifier Transconductance	0.5	1	1.5	mS		
Error Amplifier Output Impedance		1		mΩ		
Error Amplifier Max Sink Current	15	40	60	µA		
Error Amplifier Max Source Current	15	40	60	µA		

Note: This thermal Resistance Figure Applies only to a package with the exposed pad soldered to a PCB. Faliure to do this results in, approximately, a three-fold increase in thermal resistance.

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PIN DESCRIPTION

PIN NUMBER	PIN NAME	DESCRIPTION
1	P_{GND}	Power Ground Pin. Synchronous rectifier current returns through this pin.
2	S_{GND}	Internal Ground Pin. Control circuitry returns current to this pin.
3	FB	External feedback network input connection. Connect a resistor from to ground and from FB to output voltage to control the output voltage. Regulation point at FB=0.75V Typical.
4	COMP	Compensation pin for error loop. Connect an R and C in series to ground to control open loop pole and zero.
5	SD\	Shutdown control input. Tie pin to VIN for normal operation, tie to ground for shutdown. TTL input threshold.
6	MODE	Connect this pin to VIN to force PWM operation and to S_{GND} for automatic PWM/PFM selection, for a better light load efficiency.
7	SYNC	An external clock signal can be connected to this to synchronize the switching frequency. The part runs in PWM mode in the precence of a sync clock.
8	S_{VIN}	Internal supply voltage. Control circuitry is powered from from this pin. Use an RC filter close to the pin to cut down supply noise.
9	P_{VIN}	Supply voltage for the output driver stage. Inductor charging current passes through this pin.
10	LX	Inductor switching node. Inductor tied between this pin and the output capacitor to create regulated output voltage.

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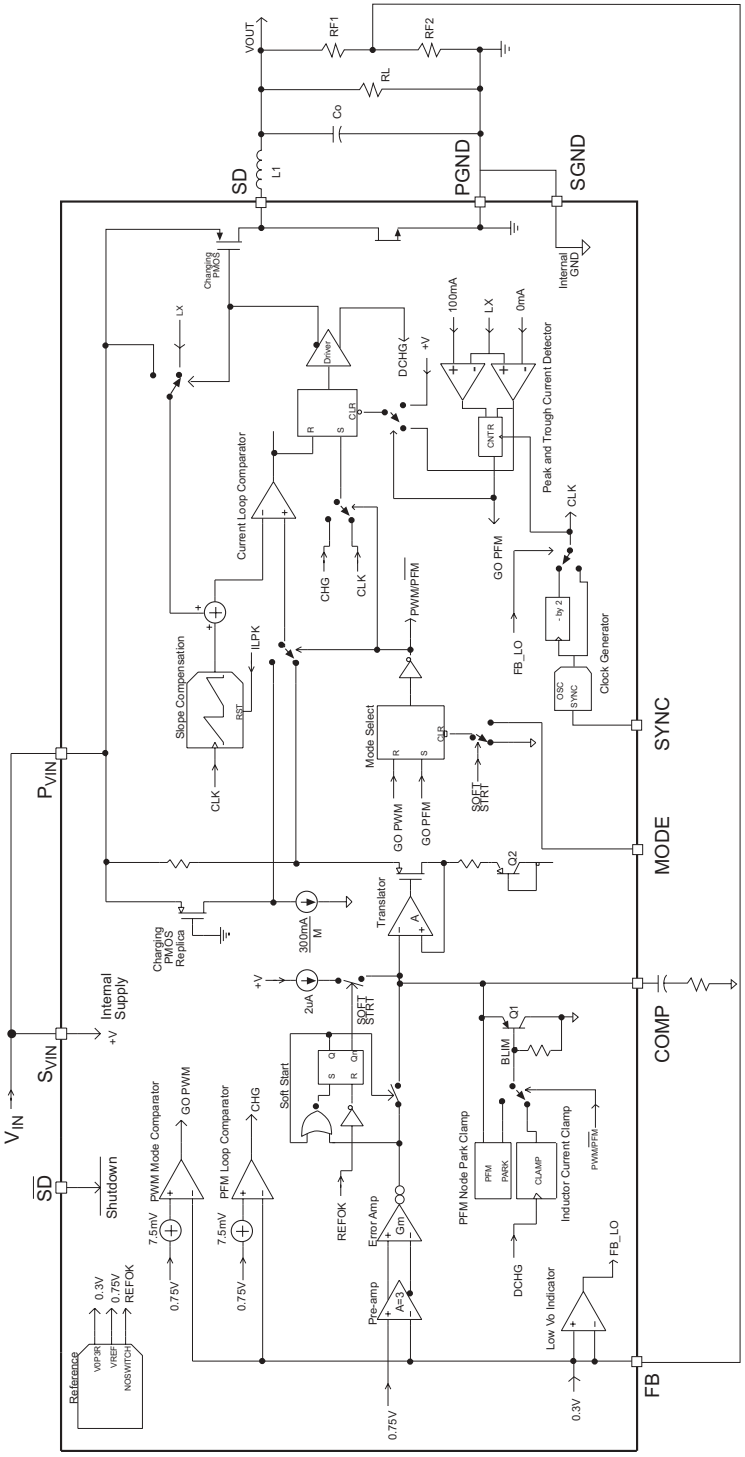

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Current Mode Control and Slope Compensation

The SP6652 is designed to use low value ceramic capacitors and low value inductors, to reduce the converter's volume and cost in portable devices Current mode PWM control was, therefore, chosen for the ease of compensation when using ceramic output capacitors and better transient line rejection, which is important in battery powered applications. Current mode control spreads the two poles of the output power train filter far apart so that the modulator gain crosses over at -20dB/decade instead of the usual -40dB/decade. The external compensation network is, simply, a series RC connected between ground and the output of the internal transconductance error amplifier.

It is well known that an unconditional instability exists for any fixed frequency current-mode converter operating above 50% duty cycle. A simple, constant-slope compensation is chosen to achieve stability under these conditions. The most common high duty cycle application is a Li-Ion battery powered regulator with a 3.3V output (D ≥ 90%). Since the current loop is critically damped when the compensation slope (denoted MC_V) equals the negative discharge slope (denoted $M2_V$), the amount of slope compensation chosen is, therefore:

$M2 = dI_L/dT_{OFF} = -V_{OUT}/L = -3.3V/4.7\mu H = -702mA/\mu s$

$M2_V = M2*R_{PMOS}$

$MC_V = -M2_V = 702mA/\mu s*0.2\Omega = 140mV/\mu s$, for RPMOS = 0.20Ω

The inductor current is sensed as a voltage across the PMOS charging switch and the NMOS synchronous rectifier (see BLOCK DIAGRAM) During inductor current charge, V(PVIN)-V(LX) represents the charging current ramp times the resistance of the PMOS charging switch. To keep the effective current slope compensation constant (remembering current is being compensated, not voltage) the voltage slope must be proportional to R_{PMOS}. To account for this, the slope compensation voltage is internally generated with a bias current that is also proportional to R_{PMOS}.

Over Current Protection

In steady state closed loop operation the voltage at the COMP pin controls the duty cycle. Due to the current mode control and the slope compensation, this voltage will be:

$V(COMP) (I_{LPK}* R_{PMOS} + MC_V *T_{ON} + V_{BE}(Q1)$

The COMP node will be clamped when the its voltage tries to exceed V(BLIM) + V_{BE} (Q1). The V_{BE}(Q1) term is cancelled by V_{BE}(Q2) at the output of the translator. The correct value of clamp voltage is, therefore:

$V(BLIM) = IL(MAX)* RPMOS + MCV *tON$

The $I_{L(MAX)}$ term is generated with a bias current that is proportional to R_{PMOS}, to keep the value of current limit approximately constant over process and temperature variations, while the $MC_V *T_{ON}$ is generated by a peak-holding circuit that senses the amplitude of the slope compensation ramp at the end of T_{ON}.

There is minimum on-time (T_{ON}) generated even if the COMP node is at 0V, since the peak current comparator is reset at the end of a charge cycle and is held low during a blanking time after the start of the next charge cycle. This is necessary to swamp the transients in the inductor current ramp around switching times. The minimum T_{ON} (50ns, nominally) is not sufficient for the COMP node to keep control of the current when the output voltage is low. The inductor current tends to rise until the energy loss from the discharge resistances are equal to

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the energy gained during the charge phase. For this reason, the clock frequency is cut in half when the feedback pin is below 0.3V, effectively reducing the minimum duty cycle in half. Above V(FB)=0.3V the clock frequency is normal (see TYPICAL OPERATIONG CHARACTERISTICS: Inductor current vs. VOUT)

PFM Control for Light Loads

If the MODE pin is connected to S_{GND}, under light load conditions the SP6652 will transition to a PFM regulation mode. In this mode of operation, V(FB) is compared to the reference voltage plus 7.5mV, nominally (see BLOCK DIAGRAM). This sets the regulation point 1% higher than the PWM regulation voltage to prevent bouncing between modes at loading conditions near threshold.

When V_{OUT} falls below the PFM regulation point the voltage loop comparator issues a command to turn on the PMOS switch to the output stage logic. The current sensing comparator compares the voltage across that switch to a reference set up by a biased replica of the PMOS switch, to set the peak PFM inductor current (nominally 300 mA). This comparator stops the charging cycle and initiates the discharge through the synchronous NMOS rectifier.

Any new charging cycles are inhibited until a third comparator, the under-current comparator, which is setup to detect the instant when the inductor is fully discharged (NMOS V_{DS} >0) enables the voltage loop. This keeps the PFM mode in discontinuous conduction mode (DCM).

A timer disables both the Current Loop and Trough Current comparators 7µs after entering DCM, to save supply current under very light load conditions. The normal light load supply current is, nominally, 135µA whereas the very light load supply current is 60µA.

Automatic Mode Selection

If the MODE pin is connected to SVIN, the part will be forced into a PWM-only regulation mode. If the MODE pin is connected to S_{GND}, the mode selection circuitry decides whether the converter should be in PWM or PFM mode, depending on the load. Light loads call for the PFM loop, which is forced into DCM as well. Medium to heavy loads activate the PWM loop.

Starting from a PWM state, the Peak and Trough Current Detector window comparator monitors the peak inductor current during charge and the trough inductor current during discharge. Both the peak and trough are monitored because the ripple current varies considerably across the application spectrum. The lossless inductor current ripple is:

$$I_L(RIPPLE)=(V_{IN}-V_{OUT})*(V_{OUT}/V_{IN})*(1/L*f_{CLK})$$

Where f_{CLK} is the switching frequency (1.2MHz, nominally).

If the peak inductor current is below 100mA or the trough reaches 0mA (or less) during one cycle, then the current is defined as low enough for PFM mode. This has to happen during 32 consecutive clock cycles before the output signal goes high and switches modes. This delay is to avoid prematurely switching into PFM mode during a negative load transient.

Once in PFM mode, the regulated output voltage will be 1% higher than in PWM and continue regulating there, as described in the PFM Control For Light Loads section. When the load increases past the point where the PFM mode can regulate while remaining in DCM (which is l 1/2 of the peak inductor current in PFM, or 1/2*300mA=150mA), the output voltage will start dropping. When it falls 1% below the reference voltage, that is 2% below the PFM regulation point, the PWM Mode Comparator will switch and set the Mode Control latch to PWM mode.

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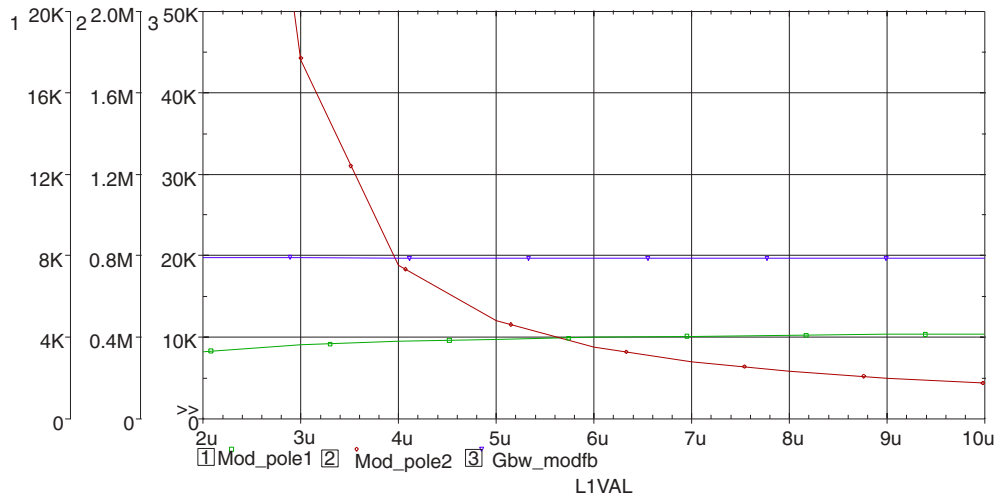
Voltage Loop and Compensation in PWM Mode

The voltage loop section of the circuit consists of the error amplifier and the translator circuits (see functional diagram). The input of the voltage loop is the 0.75V reference voltage minus the divided down output voltage at the feedback pin. The output of the error amplifier is translated from a ground referred signal (the COMP node) to a power input voltage referred signal. The output of the voltage loop is fed to the positive terminal of the Current Loop comparator, and represents the peak inductor current necessary to close the loop.

The total power supply loop is compensated with a series RC network connected from the COMP pin to ground. Compensation is simple due to current-mode control. The modulator has two dominant poles: one at a low frequency, and one above the crossover frequency of the loop, as seen in the graph below, Linearized Modulator Frequency Response vs. Inductor Value.

The low frequency pole for L1=5µH is 4kHz, the second pole is 500kHz, and the gain-bandwidth is 20kHz. The total loop crossover frequency is chosen to be 200kHz, which is 1/6th of the clock frequency. This sets the 2nd modulator pole at 2.5 times the crossover frequency. Therefore the gain of the error amplifier can be 200kHz/20kHz = 10 at the first modulator pole of 4kHz. The error amp transconductance is 1mS, so this sets the RZ resistor value in the compensation network at 10/1mS = 10kΩ. The zero frequency is placed at the first pole to provide at total system response of -20dB/decade (the zero from the error amp cancels the first modulator pole, leaving the 1 pole rolloff from the error amp pole). The compensation capacitor becomes:

$Cc = 1/(2*\pi*Rz*pole1) = 1/(6.28*10k\Omega*4kHz) = 4nF$



Conditions: V_{IN}=5V, V_{OUT}=3.3V, f_{CLK}=1.2MHz, C_{OUT}=10µF, and MC_V=132mV/µs. The inductor is varied from 2µH to 10µH

Linearized Modulator Frequency Response vs. Inductor Value.

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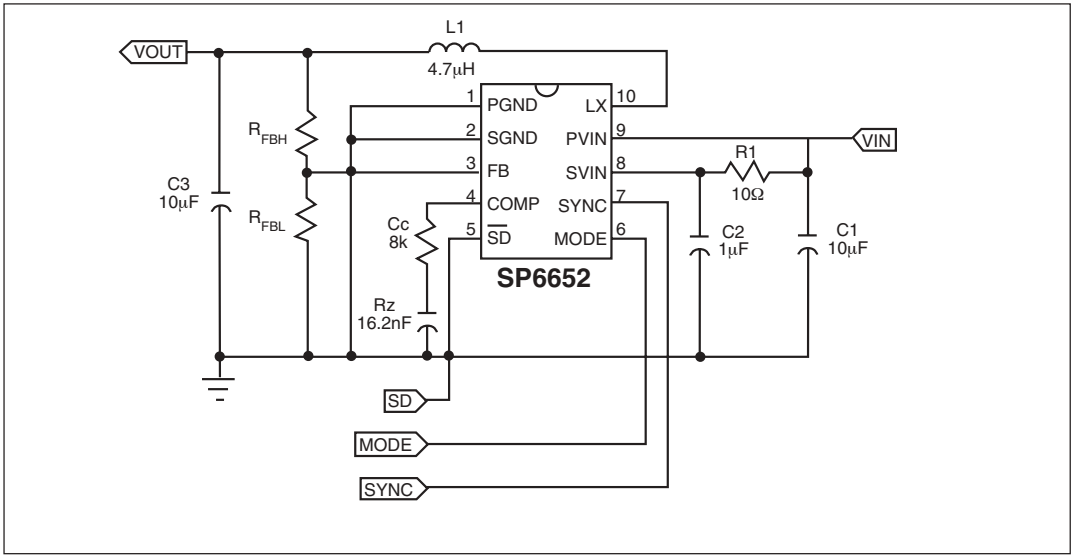

Complete Application Circuit.

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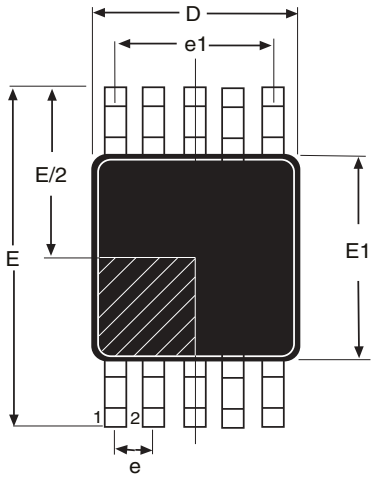
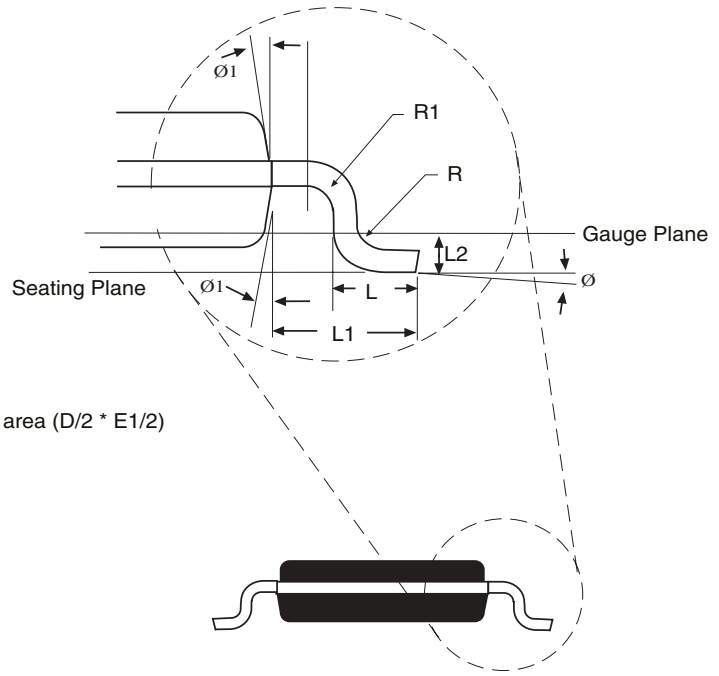
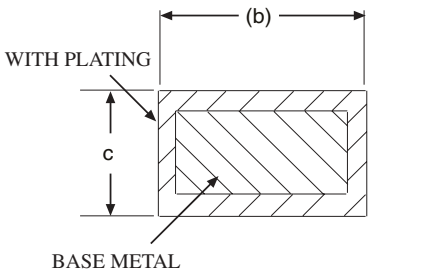
(ALL DIMENSIONS IN MILLIMETERS)

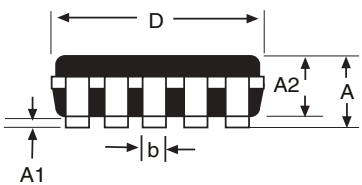


Pin #1 indentifier must be indicated within this shaded area (D/2 * E1/2)



Dimensions in (mm)	10-PIN MSOP JEDEC MO-187 (BA) Variation		
	MIN	NOM	MAX
A	-	-	1.1
A1	0	-	0.15
A2	0.75	0.85	0.95
b	0.17	-	0.27
c	0.08	-	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
e	0.50 BSC		
e1	2.00 BSC		
L	0.4	0.60	0.80
L1	-	0.95	-
L2	-	0.25	-
N	-	10	-
R	0.07	-	-
R1	0.07	-	-
Ø	0º		8º
Ø1	0º	-	15º





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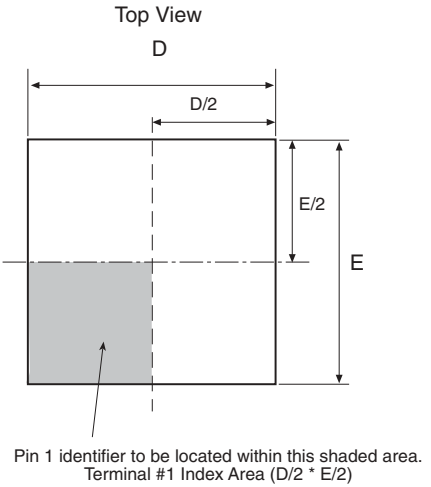

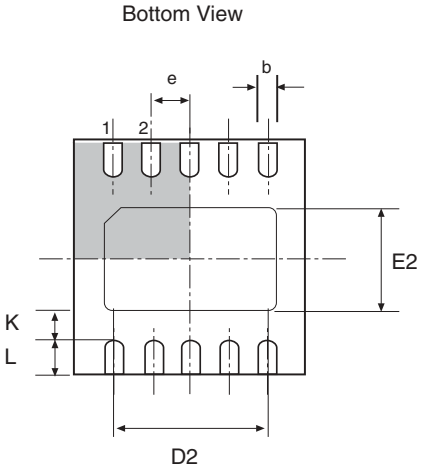

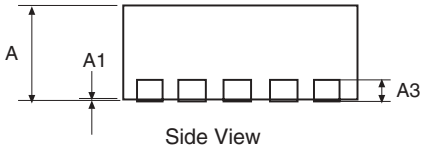

DIMENSIONS Minimum/Maximum (mm)	10 Pin DFN (JEDEC MO-229, VEED-5 VARIATION)		
COMMON HEIGHT DIMENSION			
SYMBOL	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
D	3.00 BSC		
D2	2.20	-	2.70
e	0.50 PITCH		
E	3.00 BSC		
E2	1.40	-	1.75
K	0.20	-	-
L	0.30	0.40	0.50

10 PIN DFN

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ORDERING INFORMATION

Part Number	Operating Temperature Range	Package Type
SP6652EU	-40°C to +85°C	10 Pin MSOP
SP6652EU/TR	-40°C to +85°C	10 Pin MSOP
SP6652ER	-40°C to +85°C	10 Pin DFN
SP6652ER/TR	-40°C to +85°C	10 Pin DFN

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP6652EU/TR = standard; SP6652EU-L/TR = lead free

/TR = Tape and Reel

Pack quantity is 2,500 for MSOP and 3,000 for DFN.

Sipex Corporation

ANALOG EXCELLENCE

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