NEC

MOS INTEGRATED CIRCUIT

μPD161620

432 OUTPUT TFT-LCD SOURCE DRIVER WITH RAM

DESCRIPTION

The μPD161620 is a TFT-LCD source driver that includes display RAM.

This driver has 432 outputs, a display RAM capacity of 304,128 bits (432 dots x 4 bits x 176 lines) and, can provide a 4,096-color display.

FEATURES

- TFT-LCD driver with on-chip display RAM
- Logic supply voltage: 2.5 to 3.6 V
- ★ • Driver supply voltage: 3.6 to 5.5 V
- Display RAM: 432 x 4 x 176 bits
- ★ • Driver outputs: 432 output
- CPU interface: Serial, 4-bit/8-bit parallel interface selectable
- ★ (Parallel interface requires WAIT control via RDY signal)
- Colors: 4,096 colors/pixel
- On-chip VCOM generator
- On-chip timing generator
- On-chip oscillator

ORDERING INFORMATION

Part Number	Package
μPD161620	TCP/Chip

Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representatives.

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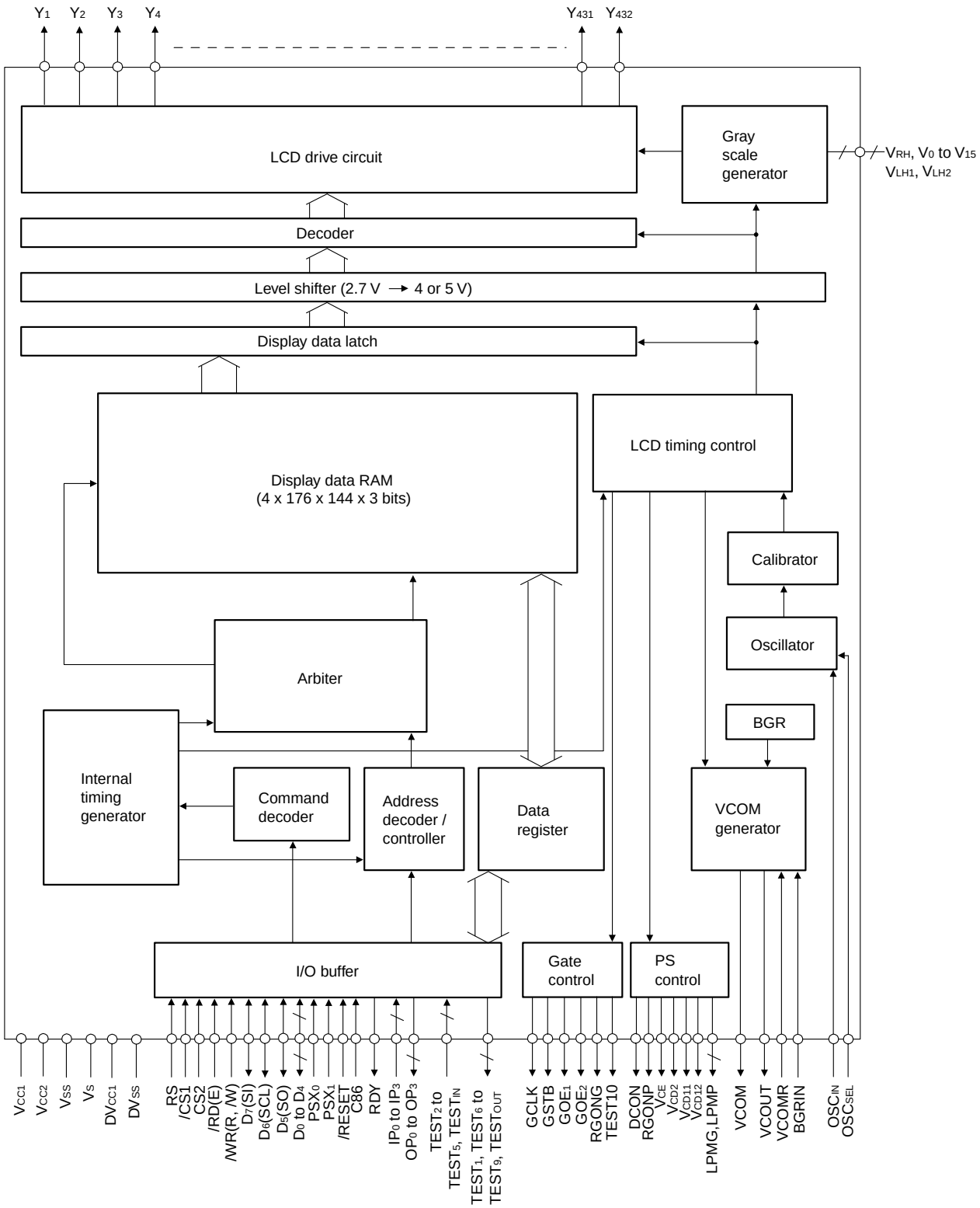
Printed in Japan

The mark ★ shows the major revised points.

★ 1. BLOCK DIAGRAM



Remark /xxx indicates active low signal.

★ 2. PIN CONFIGURATION (PAD LAYOUT)

Chip size: 16800 x 3060 μm^2

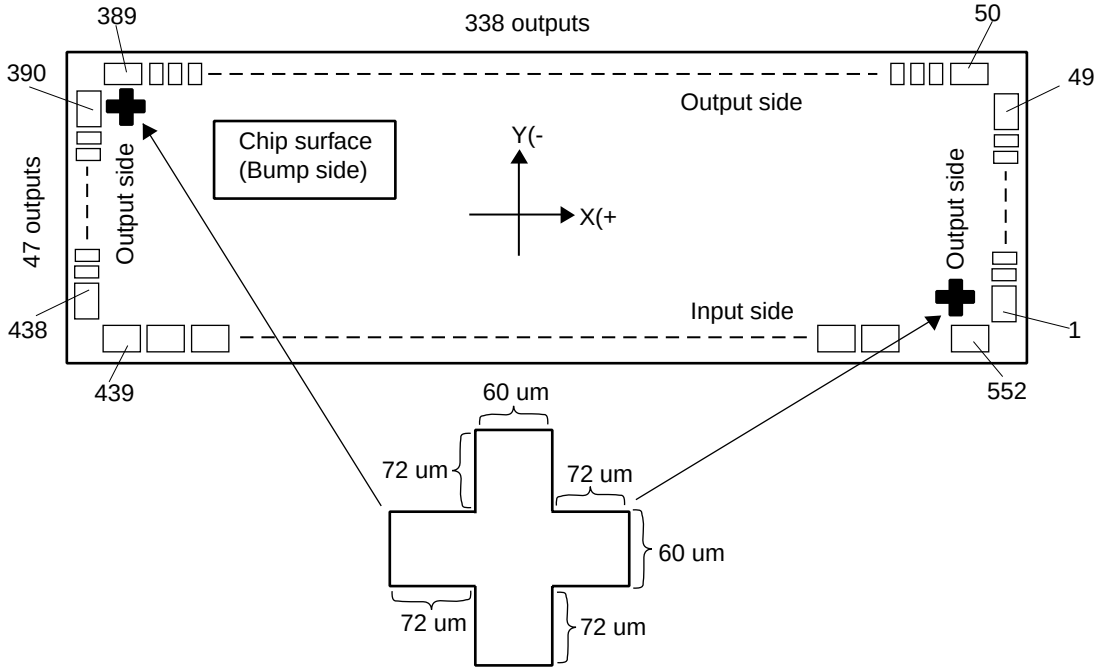
Bump size (output): 33 x 60 μm^2

Bump size (input & dummy): 87 x 60 μm^2

Alignment Mark

X: –7806.06 Y: 858.24

X: 7783.83 Y: –914.43



★ **Table 2–1. Pad Layout (1/4)**

Pad No.	Pad name	X[μm]	Y[μm]
1	DUMMY	8287.08	-1182
2	Y1	8287.08	-1104
3	Y2	8287.08	-1056
4	Y3	8287.08	-1008
5	Y4	8287.08	-960
6	Y5	8287.08	-912
7	Y6	8287.08	-864
8	Y7	8287.08	-816
9	Y8	8287.08	-768
10	Y9	8287.08	-720
11	Y10	8287.08	-672
12	Y11	8287.08	-624
13	Y12	8287.08	-576
14	Y13	8287.08	-528
15	Y14	8287.08	-480
16	Y15	8287.08	-432
17	Y16	8287.08	-384
18	Y17	8287.08	-336
19	Y18	8287.08	-288
20	Y19	8287.08	-240
21	Y20	8287.08	-192
22	Y21	8287.08	-144
23	Y22	8287.08	-96
24	Y23	8287.08	-48
25	Y24	8287.08	0
26	Y25	8287.08	48
27	Y26	8287.08	96
28	Y27	8287.08	144
29	Y28	8287.08	192
30	Y29	8287.08	240
31	Y30	8287.08	288
32	Y31	8287.08	336
33	Y32	8287.08	384
34	Y33	8287.08	432
35	Y34	8287.08	480
36	Y35	8287.08	528
37	Y36	8287.08	576
38	Y37	8287.08	624
39	Y38	8287.08	672
40	Y39	8287.08	720
41	Y40	8287.08	768
42	Y41	8287.08	816
43	Y42	8287.08	864
44	Y43	8287.08	912
45	Y44	8287.08	960
46	Y45	8287.08	1008
47	Y46	8287.08	1056
48	Y47	8287.08	1104
49	DUMMY	8287.08	1182
50	DUMMY	8166	1417.08
51	Y48	8088	1417.08
52	Y49	8040	1417.08
53	Y50	7992	1417.08
54	Y51	7944	1417.08
55	Y52	7896	1417.08
56	Y53	7848	1417.08
57	Y54	7800	1417.08
58	Y55	7752	1417.08
59	Y56	7704	1417.08
60	Y57	7656	1417.08
61	Y58	7608	1417.08
62	Y59	7560	1417.08
63	Y60	7512	1417.08
64	Y61	7464	1417.08
65	Y62	7416	1417.08
66	Y63	7368	1417.08
67	Y64	7320	1417.08
68	Y65	7272	1417.08
69	Y66	7224	1417.08
70	Y67	7176	1417.08
71	Y68	7128	1417.08
72	Y69	7080	1417.08
73	Y70	7032	1417.08
74	Y71	6984	1417.08
75	Y72	6936	1417.08
76	Y73	6888	1417.08
77	Y74	6840	1417.08
78	Y75	6792	1417.08
79	Y76	6744	1417.08
80	Y77	6696	1417.08
81	Y78	6648	1417.08
82	Y79	6600	1417.08
83	Y80	6552	1417.08
84	Y81	6504	1417.08
85	Y82	6456	1417.08
86	Y83	6408	1417.08
87	Y84	6360	1417.08
88	Y85	6312	1417.08
89	Y86	6264	1417.08
90	Y87	6216	1417.08
91	Y88	6168	1417.08
92	Y89	6120	1417.08
93	Y90	6072	1417.08
94	Y91	6024	1417.08
95	Y92	5976	1417.08
96	Y93	5928	1417.08
97	Y94	5880	1417.08
98	Y95	5832	1417.08
99	Y96	5784	1417.08
100	Y97	5736	1417.08
101	Y98	5688	1417.08
102	Y99	5640	1417.08
103	Y100	5592	1417.08
104	Y101	5544	1417.08
105	Y102	5496	1417.08
106	Y103	5448	1417.08
107	Y104	5400	1417.08
108	Y105	5352	1417.08
109	Y106	5304	1417.08
110	Y107	5256	1417.08
111	Y108	5208	1417.08
112	Y109	5160	1417.08
113	Y110	5112	1417.08
114	Y111	5064	1417.08
115	Y112	5016	1417.08
116	Y113	4968	1417.08
117	Y114	4920	1417.08
118	Y115	4872	1417.08
119	Y116	4824	1417.08
120	Y117	4776	1417.08
121	Y118	4728	1417.08
122	Y119	4680	1417.08
123	Y120	4632	1417.08
124	Y121	4584	1417.08
125	Y122	4536	1417.08
126	Y123	4488	1417.08
127	Y124	4440	1417.08
128	Y125	4392	1417.08
129	Y126	4344	1417.08
130	Y127	4296	1417.08
131	Y128	4248	1417.08
132	Y129	4200	1417.08
133	Y130	4152	1417.08
134	Y131	4104	1417.08
135	Y132	4056	1417.08
136	Y133	4008	1417.08
137	Y134	3960	1417.08
138	Y135	3912	1417.08
139	Y136	3864	1417.08
140	Y137	3816	1417.08
141	Y138	3768	1417.08
142	Y139	3720	1417.08
143	Y140	3672	1417.08
144	Y141	3624	1417.08
145	Y142	3576	1417.08
146	Y143	3528	1417.08
147	Y144	3480	1417.08
148	Y145	3432	1417.08
149	Y146	3384	1417.08
150	Y147	3336	1417.08
151	Y148	3288	1417.08
152	Y149	3240	1417.08
153	Y150	3192	1417.08
154	Y151	3144	1417.08
155	Y152	3096	1417.08
156	Y153	3048	1417.08
157	Y154	3000	1417.08
158	Y155	2952	1417.08
159	Y156	2904	1417.08
160	Y157	2856	1417.08

★ **Table 2–1. Pad Layout (2/4)**

Pad No.	Pad name	X[μm]	Y[μm]	Pad No.	Pad name	X[μm]	Y[μm]
161	Y158	2808	1417.08	241	Y238	-1032	1417.08
162	Y159	2760	1417.08	242	Y239	-1080	1417.08
163	Y160	2712	1417.08	243	Y240	-1128	1417.08
164	Y161	2664	1417.08	244	Y241	-1176	1417.08
165	Y162	2616	1417.08	245	Y242	-1224	1417.08
166	Y163	2568	1417.08	246	Y243	-1272	1417.08
167	Y164	2520	1417.08	247	Y244	-1320	1417.08
168	Y165	2472	1417.08	248	Y245	-1368	1417.08
169	Y166	2424	1417.08	249	Y246	-1416	1417.08
170	Y167	2376	1417.08	250	Y247	-1464	1417.08
171	Y168	2328	1417.08	251	Y248	-1512	1417.08
172	Y169	2280	1417.08	252	Y249	-1560	1417.08
173	Y170	2232	1417.08	253	Y250	-1608	1417.08
174	Y171	2184	1417.08	254	Y251	-1656	1417.08
175	Y172	2136	1417.08	255	Y252	-1704	1417.08
176	Y173	2088	1417.08	256	Y253	-1752	1417.08
177	Y174	2040	1417.08	257	Y254	-1800	1417.08
178	Y175	1992	1417.08	258	Y255	-1848	1417.08
179	Y176	1944	1417.08	259	Y256	-1896	1417.08
180	Y177	1896	1417.08	260	Y257	-1944	1417.08
181	Y178	1848	1417.08	261	Y258	-1992	1417.08
182	Y179	1800	1417.08	262	Y259	-2040	1417.08
183	Y180	1752	1417.08	263	Y260	-2088	1417.08
184	Y181	1704	1417.08	264	Y261	-2136	1417.08
185	Y182	1656	1417.08	265	Y262	-2184	1417.08
186	Y183	1608	1417.08	266	Y263	-2232	1417.08
187	Y184	1560	1417.08	267	Y264	-2280	1417.08
188	Y185	1512	1417.08	268	Y265	-2328	1417.08
189	Y186	1464	1417.08	269	Y266	-2376	1417.08
190	Y187	1416	1417.08	270	Y267	-2424	1417.08
191	Y188	1368	1417.08	271	Y268	-2472	1417.08
192	Y189	1320	1417.08	272	Y269	-2520	1417.08
193	Y190	1272	1417.08	273	Y270	-2568	1417.08
194	Y191	1224	1417.08	274	Y271	-2616	1417.08
195	Y192	1176	1417.08	275	Y272	-2664	1417.08
196	Y193	1128	1417.08	276	Y273	-2712	1417.08
197	Y194	1080	1417.08	277	Y274	-2760	1417.08
198	Y195	1032	1417.08	278	Y275	-2808	1417.08
199	Y196	984	1417.08	279	Y276	-2856	1417.08
200	Y197	936	1417.08	280	Y277	-2904	1417.08
201	Y198	888	1417.08	281	Y278	-2952	1417.08
202	Y199	840	1417.08	282	Y279	-3000	1417.08
203	Y200	792	1417.08	283	Y280	-3048	1417.08
204	Y201	744	1417.08	284	Y281	-3096	1417.08
205	Y202	696	1417.08	285	Y282	-3144	1417.08
206	Y203	648	1417.08	286	Y283	-3192	1417.08
207	Y204	600	1417.08	287	Y284	-3240	1417.08
208	Y205	552	1417.08	288	Y285	-3288	1417.08
209	Y206	504	1417.08	289	Y286	-3336	1417.08
210	Y207	456	1417.08	290	Y287	-3384	1417.08
211	Y208	408	1417.08	291	Y288	-3432	1417.08
212	Y209	360	1417.08	292	Y289	-3480	1417.08
213	Y210	312	1417.08	293	Y290	-3528	1417.08
214	Y211	264	1417.08	294	Y291	-3576	1417.08
215	Y212	216	1417.08	295	Y292	-3624	1417.08
216	Y213	168	1417.08	296	Y293	-3672	1417.08
217	Y214	120	1417.08	297	Y294	-3720	1417.08
218	Y215	72	1417.08	298	Y295	-3768	1417.08
219	Y216	24	1417.08	299	Y296	-3816	1417.08
220	Y217	-24	1417.08	300	Y297	-3864	1417.08
221	Y218	-72	1417.08	301	Y298	-3912	1417.08
222	Y219	-120	1417.08	302	Y299	-3960	1417.08
223	Y220	-168	1417.08	303	Y300	-4008	1417.08
224	Y221	-216	1417.08	304	Y301	-4056	1417.08
225	Y222	-264	1417.08	305	Y302	-4104	1417.08
226	Y223	-312	1417.08	306	Y303	-4152	1417.08
227	Y224	-360	1417.08	307	Y304	-4200	1417.08
228	Y225	-408	1417.08	308	Y305	-4248	1417.08
229	Y226	-456	1417.08	309	Y306	-4296	1417.08
230	Y227	-504	1417.08	310	Y307	-4344	1417.08
231	Y228	-552	1417.08	311	Y308	-4392	1417.08
232	Y229	-600	1417.08	312	Y309	-4440	1417.08
233	Y230	-648	1417.08	313	Y310	-4488	1417.08
234	Y231	-696	1417.08	314	Y311	-4536	1417.08
235	Y232	-744	1417.08	315	Y312	-4584	1417.08
236	Y233	-792	1417.08	316	Y313	-4632	1417.08
237	Y234	-840	1417.08	317	Y314	-4680	1417.08
238	Y235	-888	1417.08	318	Y315	-4728	1417.08
239	Y236	-936	1417.08	319	Y316	-4776	1417.08
240	Y237	-984	1417.08	320	Y317	-4824	1417.08

★ **Table 2–1. Pad Layout (3/4)**

Pad No.	Pad name	X[μm]	Y[μm]
321	Y318	-4872	1417.08
322	Y319	-4920	1417.08
323	Y320	-4968	1417.08
324	Y321	-5016	1417.08
325	Y322	-5064	1417.08
326	Y323	-5112	1417.08
327	Y324	-5160	1417.08
328	Y325	-5208	1417.08
329	Y326	-5256	1417.08
330	Y327	-5304	1417.08
331	Y328	-5352	1417.08
332	Y329	-5400	1417.08
333	Y330	-5448	1417.08
334	Y331	-5496	1417.08
335	Y332	-5544	1417.08
336	Y333	-5592	1417.08
337	Y334	-5640	1417.08
338	Y335	-5688	1417.08
339	Y336	-5736	1417.08
340	Y337	-5784	1417.08
341	Y338	-5832	1417.08
342	Y339	-5880	1417.08
343	Y340	-5928	1417.08
344	Y341	-5976	1417.08
345	Y342	-6024	1417.08
346	Y343	-6072	1417.08
347	Y344	-6120	1417.08
348	Y345	-6168	1417.08
349	Y346	-6216	1417.08
350	Y347	-6264	1417.08
351	Y348	-6312	1417.08
352	Y349	-6360	1417.08
353	Y350	-6408	1417.08
354	Y351	-6456	1417.08
355	Y352	-6504	1417.08
356	Y353	-6552	1417.08
357	Y354	-6600	1417.08
358	Y355	-6648	1417.08
359	Y356	-6696	1417.08
360	Y357	-6744	1417.08
361	Y358	-6792	1417.08
362	Y359	-6840	1417.08
363	Y360	-6888	1417.08
364	Y361	-6936	1417.08
365	Y362	-6984	1417.08
366	Y363	-7032	1417.08
367	Y364	-7080	1417.08
368	Y365	-7128	1417.08
369	Y366	-7176	1417.08
370	Y367	-7224	1417.08
371	Y368	-7272	1417.08
372	Y369	-7320	1417.08
373	Y370	-7368	1417.08
374	Y371	-7416	1417.08
375	Y372	-7464	1417.08
376	Y373	-7512	1417.08
377	Y374	-7560	1417.08
378	Y375	-7608	1417.08
379	Y376	-7656	1417.08
380	Y377	-7704	1417.08
381	Y378	-7752	1417.08
382	Y379	-7800	1417.08
383	Y380	-7848	1417.08
384	Y381	-7896	1417.08
385	Y382	-7944	1417.08
386	Y383	-7992	1417.08
387	Y384	-8040	1417.08
388	Y385	-8088	1417.08
389	DUMMY	-8166	1417.08
390	DUMMY	-8287.08	1182
391	Y386	-8287.08	1104
392	Y387	-8287.08	1056
393	Y388	-8287.08	1008
394	Y389	-8287.08	960
395	Y390	-8287.08	912
396	Y391	-8287.08	864
397	Y392	-8287.08	816
398	Y393	-8287.08	768
399	Y394	-8287.08	720
400	Y395	-8287.08	672
401	Y396	-8287.08	624
402	Y397	-8287.08	576
403	Y398	-8287.08	528
404	Y399	-8287.08	480
405	Y400	-8287.08	432
406	Y401	-8287.08	384
407	Y402	-8287.08	336
408	Y403	-8287.08	288
409	Y404	-8287.08	240
410	Y405	-8287.08	192
411	Y406	-8287.08	144
412	Y407	-8287.08	96
413	Y408	-8287.08	48
414	Y409	-8287.08	0
415	Y410	-8287.08	-48
416	Y411	-8287.08	-96
417	Y412	-8287.08	-144
418	Y413	-8287.08	-192
419	Y414	-8287.08	-240
420	Y415	-8287.08	-288
421	Y416	-8287.08	-336
422	Y417	-8287.08	-384
423	Y418	-8287.08	-432
424	Y419	-8287.08	-480
425	Y420	-8287.08	-528
426	Y421	-8287.08	-576
427	Y422	-8287.08	-624
428	Y423	-8287.08	-672
429	Y424	-8287.08	-720
430	Y425	-8287.08	-768
431	Y426	-8287.08	-816
432	Y427	-8287.08	-864
433	Y428	-8287.08	-912
434	Y429	-8287.08	-960
435	Y430	-8287.08	-1008
436	Y431	-8287.08	-1056
437	Y432	-8287.08	-1104
438	DUMMY	-8287.08	-1182
439	DUMMY	-8204.46	-1417.08
440	DUMMY	-8060.46	-1417.08
441	TEST10	-7916.46	-1417.08
442	LPMG	-7772.46	-1417.08
443	RGONG	-7628.46	-1417.08
444	GOE2	-7484.46	-1417.08
445	GOE1	-7340.46	-1417.08
446	GCLK	-7196.46	-1417.08
447	GSTB	-7052.46	-1417.08
448	DVCC1	-6908.46	-1417.08
449	IP3	-6764.46	-1417.08
450	IP2	-6620.46	-1417.08
451	IP1	-6476.46	-1417.08
452	IP0	-6332.46	-1417.08
453	DVSS	-6188.46	-1417.08
454	OP3	-6044.46	-1417.08
455	OP2	-5900.46	-1417.08
456	OP1	-5756.46	-1417.08
457	OP0	-5612.46	-1417.08
458	DUMMY	-5468.46	-1417.08
459	VRL2	-5324.46	-1417.08
460	VRL1	-5180.46	-1417.08
461	V15	-5036.46	-1417.08
462	V14	-4892.46	-1417.08
463	V13	-4748.46	-1417.08
464	V12	-4604.46	-1417.08
465	V11	-4460.46	-1417.08
466	V10	-4316.46	-1417.08
467	V9	-4172.46	-1417.08
468	V8	-4028.46	-1417.08
469	V7	-3884.46	-1417.08
470	V6	-3740.46	-1417.08
471	V5	-3596.46	-1417.08
472	V4	-3452.46	-1417.08
473	V3	-3308.46	-1417.08
474	V2	-3164.46	-1417.08
475	V1	-3020.46	-1417.08
476	V0	-2876.46	-1417.08
477	VRH	-2732.46	-1417.08
478	DUMMY	-2588.46	-1417.08
479	TEST6	-2444.46	-1417.08
480	DVCC1	-2300.46	-1417.08

★ **Table 2–1. Pad Layout (4/4)**

Pad No.	Pad name	X[μm]	Y[μm]
481	DVSS	-2156.46	-1417.08
482	BGRIN	-2012.46	-1417.08
483	VCOMR	-1868.46	-1417.08
484	VS	-1724.46	-1417.08
485	VS	-1580.46	-1417.08
486	VS	-1436.46	-1417.08
487	VSS	-1292.46	-1417.08
488	VSS	-1148.46	-1417.08
489	VSS	-1004.46	-1417.08
490	VCC1	-860.46	-1417.08
491	VCC1	-716.46	-1417.08
492	VCC1	-572.46	-1417.08
493	DUMMY	-428.46	-1417.08
494	DUMMY	-284.46	-1417.08
495	DUMMY	-140.46	-1417.08
496	VCOM	3.54	-1417.08
497	VCOUT	147.54	-1417.08
498	DUMMY	291.54	-1417.08
499	DCON	435.54	-1417.08
500	RGONP	579.54	-1417.08
501	LPMP	723.54	-1417.08
502	VCD11	867.54	-1417.08
503	VCD12	1011.54	-1417.08
504	VCD2	1155.54	-1417.08
505	VCE	1299.54	-1417.08
506	TESTOUT	1443.54	-1417.08
507	TESTIN	1587.54	-1417.08
508	DUMMY	1731.54	-1417.08
509	VCC2	1875.54	-1417.08
510	VCC2	2019.54	-1417.08
511	VCC2	2163.54	-1417.08
512	CS2	2307.54	-1417.08
513	DUMMY	2451.54	-1417.08
514	/RD(E)	2595.54	-1417.08
515	/WR(R,/W)	2739.54	-1417.08
516	RS	2883.54	-1417.08
517	D0	3027.54	-1417.08
518	D1	3171.54	-1417.08
519	D2	3315.54	-1417.08
520	D3	3459.54	-1417.08
521	D4	3603.54	-1417.08
522	D5(SO)	3747.54	-1417.08
523	D6(SCL)	3891.54	-1417.08
524	D7(SI)	4035.54	-1417.08
525	/CS1	4179.54	-1417.08
526	/RESET	4323.54	-1417.08
527	RDY	4467.54	-1417.08
528	OSCIN	4611.54	-1417.08
529	DVSS	4755.54	-1417.08
530	DUMMY	4899.54	-1417.08
531	DVCC1	5043.54	-1417.08
532	PSX1	5187.54	-1417.08
533	DVSS	5331.54	-1417.08
534	PSX0	5475.54	-1417.08
535	DVCC1	5619.54	-1417.08
536	C86	5763.54	-1417.08
537	DVSS	5907.54	-1417.08
538	OSCSEL	6051.54	-1417.08
539	DVCC1	6195.54	-1417.08
540	TEST5	6339.54	-1417.08
541	TEST4	6483.54	-1417.08
542	DVSS	6627.54	-1417.08
543	TEST3	6771.54	-1417.08
544	DVCC1	6915.54	-1417.08
545	TEST2	7059.54	-1417.08
546	DVSS	7203.54	-1417.08
547	TEST1	7347.54	-1417.08
548	TEST9	7491.54	-1417.08
549	TEST8	7779.54	-1417.08
550	TEST7	7779.54	-1417.08
551	DUMMY	7923.54	-1417.08
552	DUMMY	8204.46	-1417.08

3. PIN FUNCTIONS

3.1 Power Supply System Pins

Symbol	Pin Name	Pad No.	I/O	Function
V_{CC1}	Logic power supply pin	490 to 492	-	Power supply pin for logic circuit
V_{CC2}	I/O power supply pin	509 to 511	-	Power supply pin for I/O buffer
V_S	Driver power supply pin	484 to 486	-	Power supply pin for driver circuit
V_{SS}	Ground pin	487 to 489	-	Ground pin for logic and driver circuits
★ V_0 to V_{15} V_{RH} V_{RL1}, V_{RL2}	Power supply for γ-curve correction	476 to 461 477, 460, 459	-	The μPD161620 includes power supplies and resistors for the γ-curve, so if the characteristics of the γ-curve and LCD panel in the μPD161620 match, leave V_0 to V_{15}, V_{RH}, V_{RL1}, V_{RL2} open. If some kind of correction is required, adjust the γ-curve by connecting resistors between the V_0 to V_{15}, V_{RH}, V_{RL1}, V_{RL2} pins (see **5.9 γ-Curve Correction Power Supply Circuit for Cases of Unbalanced Driving**).
★ DV_{CC1}	Mode setting pull-up power-supply pin	448,480,531, 535,539,544	-	Pull-up power-supply pin for mode setting
★ DV_{SS}	Mode setting pull-down power-supply pin	453,481,529, 533,537,542, 546	-	Pull-down power-supply pin for mode setting

3.2 Logic System Pins (1/3)

Symbol	Pin Name	Pad No.	I/O	Function
PSX_0, PSX_1	CPU interface selection	534, 532	Input	These pins are used to select the CPU interface mode. PSX_0 = H: 8-bit parallel interface PSX_0 = L: 4-bit parallel interface PSX_1 = H: Parallel interface PSX_1 = L: Serial interface
/CS1, CS2	Chip select	525, 512	Input	This pin is used for chip select signals. When /CS1 = L (CS2 = H), the chip is active and can perform data input/output operations including command and data I/O.
/RD (E)	Read (enable)	514	Input	When i80 series parallel data transfer (/RD) has been selected, the signal at this pin is used to enable read operations. Data is output to the data bus only when this pin is low. When M68 series parallel data transfer (E) has been selected, the signal at this pin is used to enable read/write operations.
★ /WR (R, /W)	Write(read/write)	515	Input	When i80 series parallel data transfer (/WR) has been selected, the signal at this pin is used to enable write operations. Data is written at the rising edge of this signal. When M68 series parallel data transfer (R, /W) and serial data has been selected, this pin is used to determine the direction of data transfer. L: Write H: Read
C86	Select interface	536	Input	This pin is used to switch between interface modes (i80 series CPU or M68 series CPU). L: Selects i80 series CPU mode H: Selects M68 series CPU mode

(2/3)

	Symbol	Pin Name	Pad No.	I/O	Function
★	RDY	Ready signal	527	Output	This pin is the ready signal output. When in 4-bit or 8-bit parallel mode, connect this pin to external WAIT pin of the CPU. When in serial mode, this pin is not used, so leave it open.
★	D_0 to D_7 (SI) (SO) (SCL)	Data bus (Serial data Input) (Serial data output) (Serial clock)	517 to 524	I/O	These pins comprise 8-bit bi-directional data. When the serial interface has been selected (PSX_1 = L), D_7 functions as a serial data input pin (SI), D_6 functions as a serial clock input pin (SCL), and D_5 functions as a serial data output pin (SO). In either case, pins D_0 to D_4 are in high impedance mode. When the chip is not selected, D_0 to D_7 are in high impedance mode.
★	RS	Index register/data, command selection	516	Input	When parallel data transfer has been selected, this pin is usually connected to the LSB of the standard CPU address bus and is used to distinguish between data from index registers and data/commands. RS = H: Indicates that data from D_0 to D_7 is data/command RS = L: Indicates that data from D_0 to D_7 is index register contents Also, when serial data transfer is selected, the level of the RS pin is fetched at the rising edge of the eighth clock of the serial clock and whether the data is index register contents or data/command is distinguished. RS = H: Indicates that the data input to SI is data/command. RS= L: Indicates that the data input to SI is index register contents.
	$TEST_{OUT}$	Test output	506	Output	This test output pin is used when the IC is in test mode, otherwise, it is left unconnected.
	/RESET	Reset	526	Input	When /RESET is low, an internal reset is performed. The reset operation is executed at the /RESET signal level. Be sure to perform reset via this pin at power application.
★	$TEST_4$, $TEST_5$	Test	540, 541	Input	Input low level.
	$TEST_2$, $TEST_3$		545, 543		
★	IP_0 to IP_3	Input port	452 to 449	Input	This is a general-purpose input port. The status of these pins (H or L) can be read via a command. Because this is CMOS input, do not leave these pins open.
★	OP_0 to OP_3	Output port	457 to 459	Output	This is a general-purpose output port. The status of these pins (H or L) can be write via a command.
★	$TEST_6$	Test	479	Output	Leave open.
★	$TEST_1$		547		
★	$TEST_{10}$		441		Connect this pin to the SB pin of the gate driver.
★	LPMG	Low power mode signal	442	Output	This is an output pin for low power mode (for the gate driver). Connect this pin to the LPM pin of the gate driver.
★	LPMP		501		This is an output pin for the low power mode (for the power-supply IC). Connect this pin to the LPM pin of the power-supply IC.
★	GOE_1	OE_1 output for gate driver	445	Output	This pin is an output pin for the low power mode (for the OE_1). Connect to the OE_1 pin of the gate driver. For the signal output timing, refer to **5.4 Display Timing Generator.**
★	GOE_2	OE_2 output for gate driver	444	Output	This pin is the OE_2 output for the gate driver. Connect to the OE_2 pin of the gate driver. For the signal output timing, refer to **5.4 Display Timing Generator.**

(3/3)

	Symbol	Pin Name	Pad No.	I/O	Function
★	GSTB	STB output for gate driver	447	Output	This pin is the STB output for the gate driver. Connect to the STVR or STVL pin of the gate driver. For the signal output timing, refer to **5.4 Display Timing Generator.**
	GCLK	CLK output for gate driver	446	Output	This pin is the CLK output for the gate driver. Connect this pin to the CLK pin of the gate driver.
★	DCON	DC/DC converter control	499	Output	DC/DC converter ON/OFF control of power supply IC Connect this pinto the DCON pin of the power-supply IC.
★	RGONP	Regulator control	500	Output	Regulator ON/OFF control of power supply IC Connect this pin to the RGONP pin of the power-supply IC.
★	RGONG	Regulator control	443	Output	Regulator ON/OFF control of gate driver IC Connect this pin to the RGONG pin of the gate driver.
★	V_{CD11}, V_{CD12}	V_{DD1} booster select	502, 503	Output	Control signal to select x4/x5/x6/x7 booster of power supply IC for V_{DD1}. Connect this pin to the V_{CD11} and V_{CD12} pins of the power-supply IC.
★	V_{CD2}	V_{DD2} booster select	504	Output	Control signal to select x2/x3 booster of power supply IC for V_{DD2}. Connect this pin to the V_{CD2} pin of the power-supply IC.
★	V_{CE}	V_O level select	505	Output	Signal for selecting the level of the power supply IC booster voltage, to be used for the maximum voltage of V_O. Selects that the booster voltage level is either the same level as V_{DD1} or a multiple of minus 1. Connect this pin to the V_{CE} pin of the power-supply IC.
★	$TEST_7$	Test	550	I/O	Leave open.
★	$TEST_8$		549	I/O	
★	$TEST_9$		548	I/O	
★	OSC_{IN}	Oscillation signal pins	528	Input	This pin is for oscillation signal input. OSC_{IN} = H: Input oscillation signal OSC_{IN} = L: This pin is left open.
	OSC_{SEL}	Oscillation signal select	538	Input	This pin is the oscillation signal select. When an external oscillation circuit is used, set this pin to H. When an internal oscillation circuit is used, set this pin to L.
★	BGRIN	External-power-supply connection pin	482	Input	This is an external-power-supply input pin for VCOM. For more detail, refer to **5.5 Common Adjustment Circuit.**
★	VCOMR	VCOM setting resistor connection pin	483	Input	Connects an external resistor for VCOM setting. For more detail, refer to **5.5 Common Adjustment Circuit.**
★	$TEST_{IN}$	Test input pins	507	Input	These pins are used to set a test mode for the IC. Normally, this setting is open.

3.3 Driver-Related Pins

	Symbol	Pin Name	Pad No.	I/O	Function
	Y_1 to Y_{432}	Source output	2 to 48, 51 to 388, 391 to 519	Output	Source output pins
★	VCOM	COM center voltage adjustment	514	Output	This pin is the common center voltage adjustment output. For more detail, refer to **5.5 Common Adjustment Circuit.**
★	VCOUT	Center rectangle signal output	515	Output	This pin is the center rectangle signal output (4 V_{p-p} or 5 V_{p-p}) for common modulation. For more detail, refer to **5.5 Common Adjustment Circuit.**
	DUMMY	Dummy pin	1, 49, 50, 389, 390, 438 to 441, 449, 477 to 480, 498 to 500, 524, 541, 546 to 552		Dummy pin

★ 4. PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The I/O circuit types of each pin and recommended connection of unused pins are described below.

Pin Name	Input Type	I/O	Power supply	Recommended Connection of Unused Pins	
				Parallel Interface	Serial Interface
PSX_0, PSX_1	Schmitt trigger	Input	V_{CC1}	Mode setting pin[Note]	
CS2	Filter	Input	V_{CC2}	Connect to V_{CC2}	
/RD(E)	Filter	Input	V_{CC2}	Connect to V_{CC2} (when i80 series interface)	Connect to V_{CC2} or V_{SS}
C86	Schmitt trigger	Input	V_{CC1}	Mode setting pin[Note]	Connect to V_{CC1} or V_{SS}[Note]
RDY	-	Output	V_{CC2}	-	Leave open
D_0 to D_4	Filter	I/O	V_{CC2}	-	Leave open
D_5 (SO)	Filter	I/O	V_{CC2}	-	
D_6 (SCL)	Filter	I/O	V_{CC2}	-	
D_7 (SI)	Filter	I/O	V_{CC2}	-	
$TEST_{OUT}$	-	Output	V_{CC1}	Leave open	
/RESET	Filter	Input	V_{CC2}	Always reset on power application	
IP_0 to IP_3	Schmitt trigger	Input	V_{CC1}	Connect to V_{CC1} or V_{SS1}.	
OP_0 to OP_3	-	Output	V_{CC1}	Leave open	
$TEST_{10}$	-	Output	V_{CC1}	Leave open	
LPMG, LPMP	-	Output	V_{CC1}	Leave open	
GOE_1	-	Output	V_{CC1}	Always connect to the gate driver	
GOE_2	-	Output	V_{CC1}	Always connect to the gate driver	
GSTB	-	Output	V_{CC1}	Always connect to the gate driver	
GCLK	-	Output	V_{CC1}	Always connect to the gate driver	
DCON	-	Output	V_{CC1}	Always connect to the power IC	
RGONP	-	Output	V_{CC1}	Always connect to the power IC	
RGONG	-	Output	V_{CC1}	Always connect to the gate driver	
V_{CD11}, V_{CD12}	-	Output	V_{CC1}	Always connect to the power IC	
V_{CD2}	-	Output	V_{CC1}	Always connect to the power IC	
V_{CE}	-	Output	V_{CC1}	Always connect to the power IC	
$TEST_1$	CMOS	Output	V_{CC1}	Leave open	
$TEST_2$	CMOS	Input	V_{CC1}	Connect to V_{SS}	
$TEST_3$	CMOS	Input	V_{CC1}	Connect to V_{SS}	
$TEST_4$	CMOS	Input	V_{CC1}	Connect to V_{SS}	
$TEST_5$	CMOS	Input	V_{CC1}	Connect to V_{SS}	
$TEST_6$	CMOS	Output	V_{CC1}	Leave open	
$TEST_7$	CMOS	Output	V_{CC1}	Leave open	
$TEST_8$	CMOS	Output	V_{CC1}	Leave open	
$TEST_9$	CMOS	Output	V_{CC1}	Leave open	
OSC_{IN}	CMOS	Input	V_{CC2}	Leave open (in OSC_{SEL} = L mode)	
OSC_{SEL}	Schmitt trigger	Input	V_{CC1}	Mode setting pin[Note]	
BGRIN	-	Input	V_S	Connect to V_{SS} (in BGRS = L mode)	
VCOMR	-	Input	V_S	Connect to V_{SS}	
VCOM	-	Output	V_S	Leave open	
VCOUT	-	Output	V_S	Leave open	

Note Connect to V_{CC1} or V_{SS}, depending on the mode selected.

5. DESCRIPTION OF FUNCTIONS

5.1 CPU interface

5.1.1 Selection of interface type

The μPD161620 chip transfers data using an 8-bit bidirectional data bus (D_7 to D_0), 4-bit bi-directional data bus (D_7 to D_4) or a serial data input (SI) or a serial date output (SO). Setting the polarity of the PSX0-1 pins as either H (high) or L (low) enables the selections shown in Table 5–1 below.

★ **Table 5–1.**

PSX_1	PSX_0	Mode	/CS1	RDY	RS	/RD (E)	/WR (R, /W)	C86	D_7	D_6	D_5	D_4	D_3 to D_0
H	H	8-bit parallel	/CS1	RDY	RS	/RD (E)	/WR (R, /W)	C86	D_7	D_6	D_5	D_4	D_3 to D_0
H	L	4-bit parallel	/CS1	RDY	RS	/RD (E)	/WR (R, /W)	C86	D_7	D_6	D_5	D_4	Hi-Z Note1
L	X Note2	serial Note3	/CS1	Hi-Z Note1	RS	Note2	/WR (R, /W)	Note2	SI	SCL	SO	Hi-Z Note1	Hi-Z Note1

Notes 1. Hi-Z: High impedance

2. X: Don't care (H or L)

★ **3.** In serial mode, only commands can be read. Internal RAM data cannot be read.

★ #### 5.1.2 Selection of data transfer mode

In the μPD161620, when the 8-bit parallel interface and serial interface are selected, there are tow types of modes to transfer data to display RAM. The mode can be selected as follows with the DTX command.

In the 1-pixel/2-byte mode, 1 pixel of data is written at one time to the internal RAM each time 2 bytes of data are transferred. If only 1 byte of data has been transferred, writing to the internal RAM is not possible. Similarly, in the 2-pixel/3-byte mode, 2 pixels of data are written at one time to the internal RAM each time 3 bytes of data are transferred. Execute data transfer taking into consideration the above.

Table 5–2.

DTX	Mode
1	1-pixel / 2-byte
0	2-pixel / 3-byte

★ **Caution In the 4-bit parallel mode, the DTXX command is disabled. One pixel gets written by transferring 4 bits of data 3 times. The transfer order and relationship between command data and display data are as follows.**

<When transferring command data>

First 4 -bit transfer = Higher 4 bits of command data

Second 4-bit transfer = Lower 4 bits of command data

<When transferring display data>

First 4-bit transfer = Corresponds to display data D_{11} to D_8

Second 4-bit transfer = Corresponds to display data D_7 to D_4

Third 4-bit transfer = Corresponds to display data D_3 to D_0

Figure 5–1. Correspondence Between Data Bus and Display RAM (When DTX = 1)

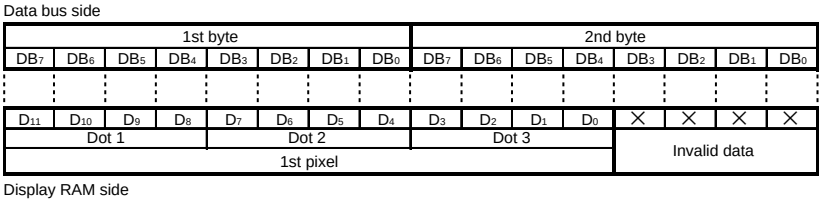
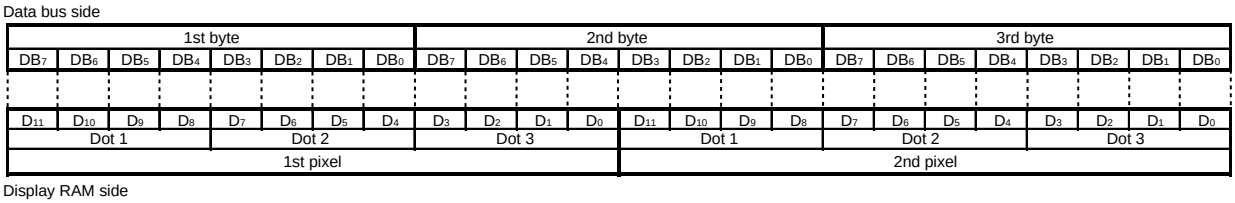


Figure 5–2. Correspondence Between Data Bus and Display RAM (When DTX = 0)



5.1.3 Parallel interface

When the parallel interface has been selected (PSX_1 = H), setting the C86 pin as either H or L enables a direct ★ connection to an i80 series or M68 series CPU (see table below). When the parallel interface is used, wait control for the bus is required. To execute wait control, connect the RDY pin to the external WAIT pin of the CPU.

Table 5–3.

C86	Mode	/RD(E)	/WR(R, /W)
H	M68 series CPU	E	R, /W
L	i80 series CPU	/RD	/WR

The data bus signal is identified according to the combination of the RS, /RD(E), and /WR(R,/W) signals, as shown in the following table.

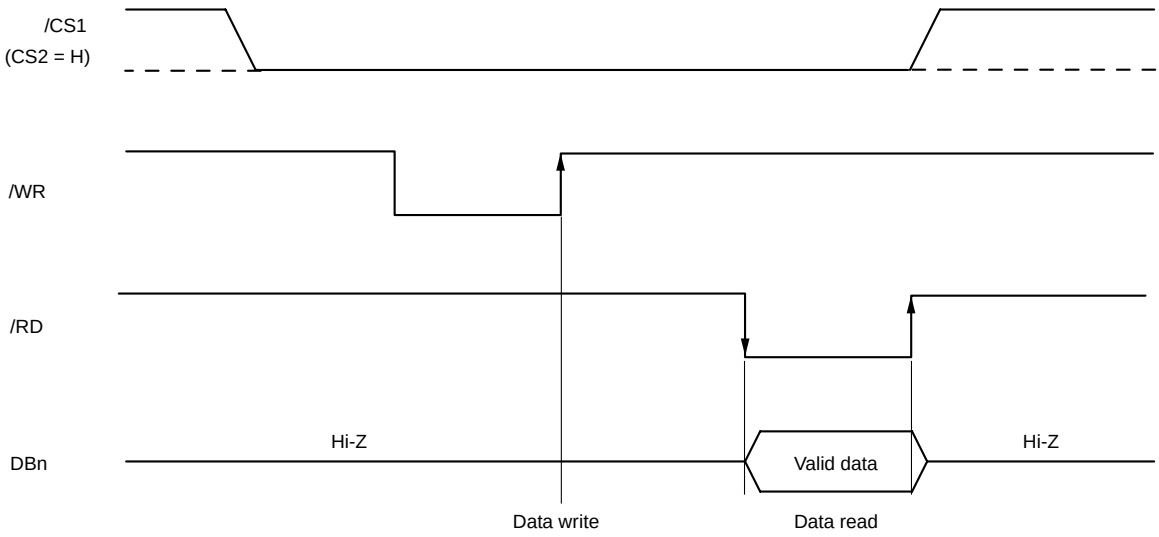
Table 5–4.

Common	M68 series CPU	i80 series CPU		Function
RS	R, /W	/RD	/WR	
H	H	L	H	Read display data and registers
H	L	H	L	Write display data and registers
L	H	L	H	Prohibited
L	L	H	L	Write to control index register

(1) i80 Series Parallel Interface

When i80 series parallel data transfer has been selected, data is written to the μPD161620 at the rising edge of the /WR signal. The data is output to the data bus when the /RD signal is L.

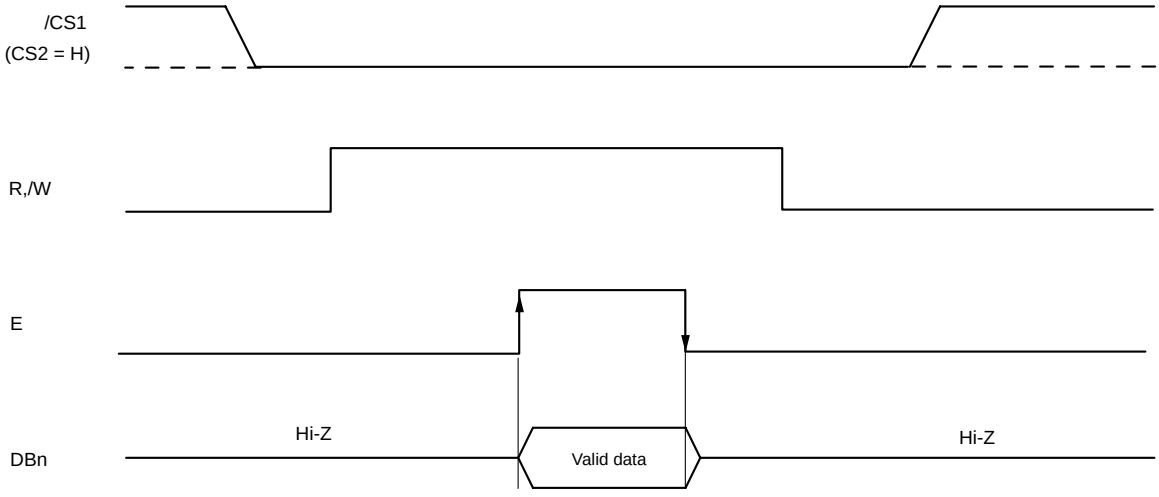
Figure 5–3. i80 Series Interface Data Bus Status



(2) M68 Series Parallel Interface

When M68 series parallel data transfer has been selected, data is written at the falling edge of the E signal when the R,/W signal is L. In a data read operation, data is output at the rising edge of the E signal in a period when the R,/W signal is H. The data bus is released (Hi-Z) at the falling edge of the E signal.

Figure 5–4. M68 Series Interface Data Bus Status (When data read)



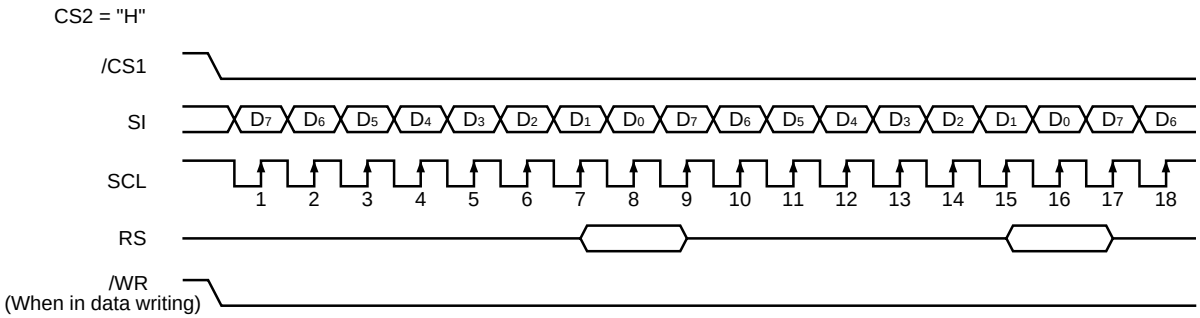
★ **5.1.4 Serial interface**

When the serial interface has been selected (PSX = L), if the chip is active (/CS1 = L, CS2 = H), serial data input (SI), serial data output (SO), and serial clock input (SCL) can be received. Serial data is read from D_7 and then from D_6 to D_0 on the rising edge of the serial clock, via the serial input pin. This data is synchronized on the eighth serial clock's rising edge and is then converted to parallel data for processing. Also, set /WR = L during write and /WR = H during read.

Note that in the 1-pixel/2-byte mode, make /CS1 active (/CS1 = L) during transfer of 1pixel of data (2 bytes). Similarly in the 2-pixel/3-byte mode, make CS1 active (/CS1 = L) during transfer of 2 pixels of data (3 bytes). IF /CS1 = H is set during data transfer, the data may not be transferred normally.

RS input is used to judge serial input data as display data or command data when RS = H the data is display data and when RS = L the data is command data. When the chip enters active mode, RS input is read at the rising edge after every eighth serial clock and is then used to judge the serial input data. The serial interface signal chart is shown below.

★ **Figure 5–5. Serial Interface Signal Chart**



Remarks 1. If the chip is not active, the shift register and counter are reset to their initial settings.

★ **2.** The data read function is disabled during serial interface mode (command register is enabled).

3. When using SCL wiring, take care concerning the possible effects of terminating reflection and noise from external sources. Our recommends checking operation with the actual device.

5.1.5 Chip select

The μPD161620 has two chip select pins (/CS1 and CS2). The CPU parallel and serial interfaces can be used only when /CS1 = L and CS2 = H. When the chip select pin is inactive, D_0 to D_7 are set to high impedance (invalid) and input of RS, /RD, or /WR is not active. If a serial interface mode has been set, the shift register and counter are both initialized.

★ Note that when using the serial interface, in the 1-pixel/2-byte mode, /CS1 must be made active (/CS1 =L) during transfer of 1 pixel of data (2 bytes). Similarly in the 2-pixel/3-byte mode, /CS1 must be made active (/CS1 = L) during transfer of 2 pixels of data (3 bytes). If /CS1 = H is set during data transfer, the data may not be transferred normally. However, if the parallel interface is used, transfer is performed normally as long as /CS1 is active only during data transfer in 1-byte units, regardless of whether the 1-pixel/2-byte mode or the 2-pixel/3-byte mode is selected.

★ **5.1.6 Wait control in parallel interface mode**

When the parallel interface mode is selected, wait control for the bus is required. Connect the RDY pin of the μPD161620 to the external WAIT pin of the CPU to execute wait control. An example of the connection to the CPU is described in **10. EXAMPLE of μPD161620 and CPU CONNECTION.**

Note that when serial interface mode is selected, wait control via the RDY signal is not required.

5.2 Display Data RAM

This is the RAM that is used to store the display's dot data. The RAM configuration is 1,728 bits (144 x 12 bits) x 176 bits. Any specified pixel can be accessed by selecting the corresponding X address and Y address.

Figure 5-6 shows the structure of display data RAM.

Figure 5–6.

D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Dot 1				Dot 2				Dot 3			
One pixel (= one X address)											

5.2.1 X address circuit

As shown in Figure 5–7, the display data RAM's X address is specified via the X address register. When using the X address increment mode, the specified X address is incremented by one each time a display data read or write operation is executed. The CPU is able to continuously access the display data.

Following incrementation up to the final X address, executing a display data read or write operation will cause the Y address to be incremented, and the X address to return to 000H. For the reset value of the address counter, see Table 5–6.

It is also possible to invert the relationship between the X address and the source output using the ADX flag of control register 1, as shown in Figure 5–7.

5.2.2 Column address circuit

When displaying the contents of the display data RAM, the column address corresponds to source output, as is shown Figure 5–7. As is shown in Table 5–5, the correspondence between the display RAM's column address and source output can be inverted using the ADC flag in control register 1 (source driver direction selection flag). This reduces the constraints on chip layout when assembling the LCD module.

Table 5–5.

Source Output		Y_1	Y_2	→	Y_{431}	Y_{432}
ADC	0	000H	001H	→ Column address →	1AEH	1AFH
	1	1AFH	1AEH	← Column address ←	001H	000H

★ 5.2.3 Y address circuit

As is shown in Figure 5–7, the Y address register is used to specify the display data RAM's Y address. When using the Y address increment mode, the specified Y address is incremented by one each time a display data read or write operation is executed. The CPU is able to continuously access the display data. The Y address is incremented up to AFH, after which the X address is incremented after each read or write operation and the Y address is set back to 00H.

In the case of the 8-bit parallel interface mode and serial interface mode, only the 1-pixel/2-byte mode can be used as the transfer mode.

Table 5–6. Counter reset for RAM increment

X-address	Y-address
08FH	AFH

★ **Figure 5–7. μPD161620 RAM addressing**

ADM0=L,ADM1=L

ADX=0

Source output															
	ADC=0	Y1	Y2	Y3	Y4	Y5	Y6	---	---	Y427	Y428	Y429	Y430	Y431	Y432
	ADC=1	Y432	Y431	Y430	Y429	Y428	Y427	---	---	Y6	Y5	Y4	Y3	Y2	Y1
	X-address	000H			001H			---	---	08EH			08FH		
	Column address	000H	001H	002H	003H	004H	005H	---	---	1AAH	1ABH	1ACH	1ADH	1AEH	1AFH
		D11---D8	D7---D4	D3---D0	D11---D8	D7---D4	D3---D0			D11---D8	D7---D4	D3---D0	D11---D8	D7---D4	D3---D0
		1st Pixel			2nd Pixel					1st Pixel			2nd Pixel		

Gate output		Y-address
R,/L=H	R,/L=L	
O1	O176	00H
O2	O175	01H
|	|	|
|	|	|
O87	O90	56H
O88	O89	57H
O89	O88	58H
O90	O87	59H
|	|	|
|	|	|
O175	O2	AEH
O176	O1	AFH

Display area

ADX=1

Source output															
	ADC=0	Y1	Y2	Y3	Y4	Y5	Y6	---	---	Y427	Y428	Y429	Y430	Y431	Y432
	ADC=1	Y432	Y431	Y430	Y429	Y428	Y427	---	---	Y6	Y5	Y4	Y3	Y2	Y1
	X-address	08FH			08EH			---	---	001H			000H		
	Column address	1AFH	1AEH	1ADH	1ACH	1ABH	1AAH	---	---	005H	004H	003H	002H	001H	000H
		D11---D8	D7---D4	D3---D0	D11---D8	D7---D4	D3---D0			D11---D8	D7---D4	D3---D0	D11---D8	D7---D4	D3---D0
		2nd Pixel			1st Pixel					2nd Pixel			1st Pixel		

Gate output		Y-address
R,/L=H	R,/L=L	
O1	O176	00H
O2	O175	01H
|	|	|
|	|	|
O87	O90	56H
O88	O89	57H
O89	O88	58H
O90	O87	59H
|	|	|
|	|	|
O175	O2	AEH
O176	O1	AFH

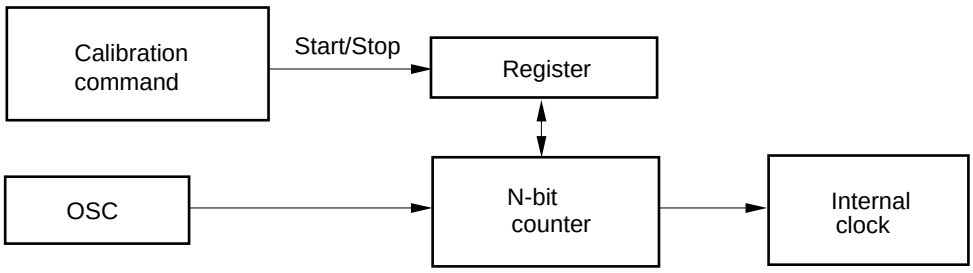
Display area

5.3 Oscillator

The μPD161620 includes a CR-type oscillator, which generate the display clock. When OSC_{SEL} is L, an internal oscillator is selected. When OSC_{SEL} is H, the internal oscillator is stopped, making it necessary to input the clock from an external oscillator.

This oscillator also has a calibration function. The time to select one line is set by the calibration start and stop commands.

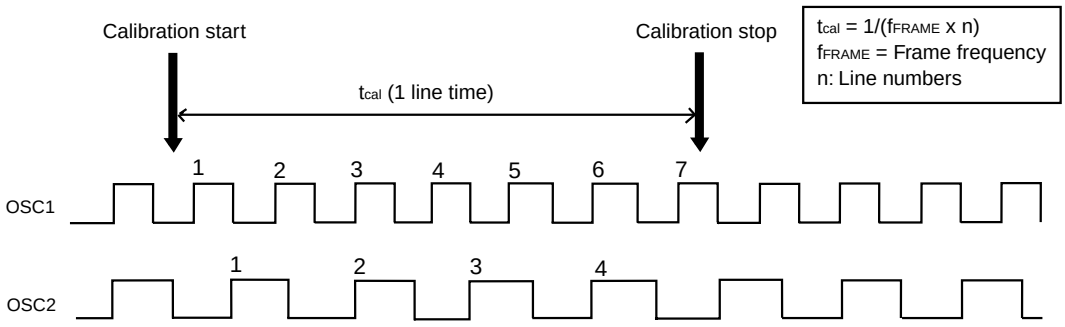
Figure 5–8. Frame Frequency Calibration



The calibration function involves counting the number of oscillation clocks generated between the start and stop signals and storing that number in a register. The number of oscillation clocks is then continually compared with this register value in subsequent operations, and the time of the clock number stored in the register is set as 1 line selection time, and used as the internal reference clock.

Using this function allows the frame frequency to be held at a constant value, even when the oscillation frequency is irregular.

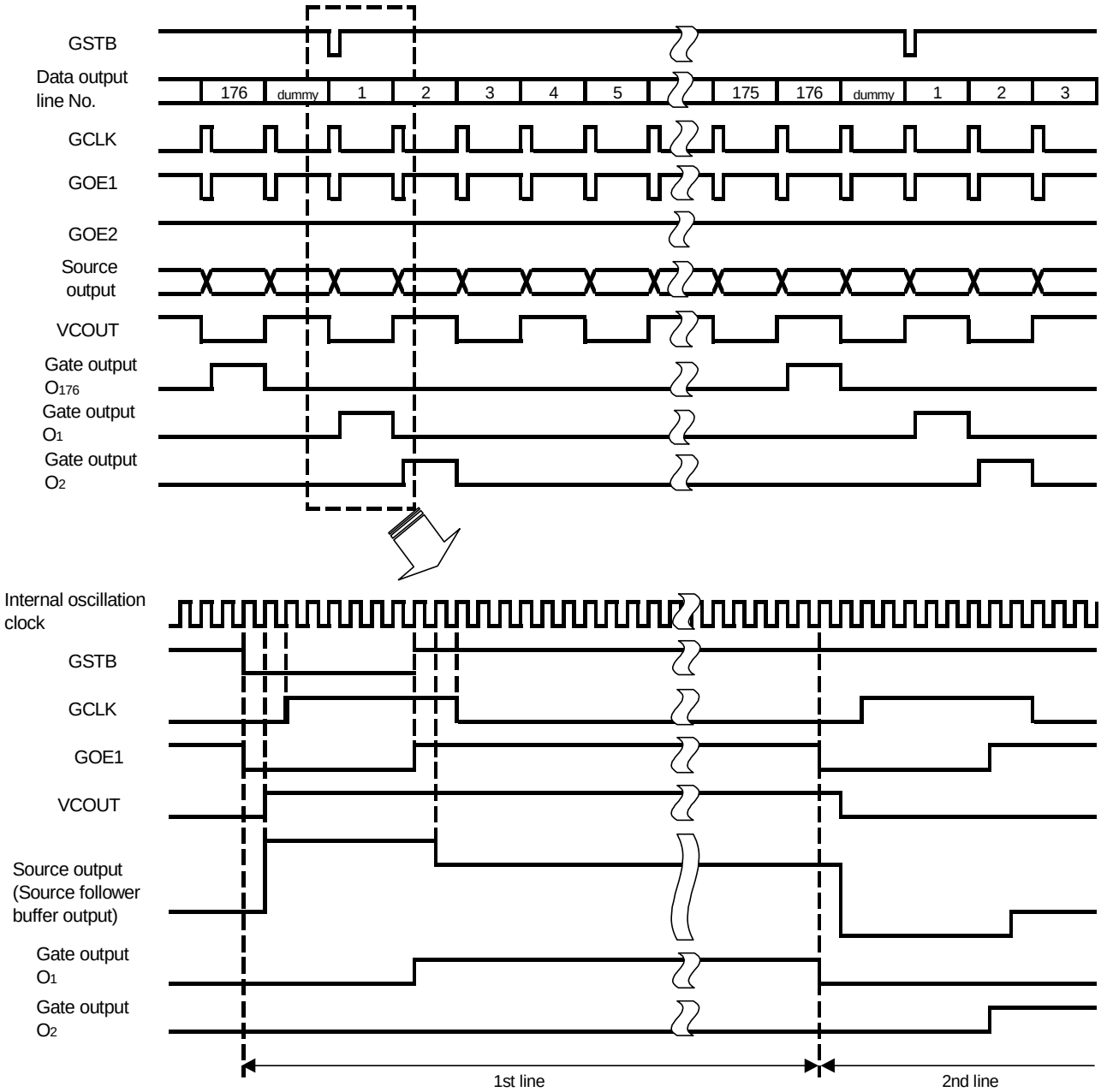
Figure 5–9. Calibration Function Timing



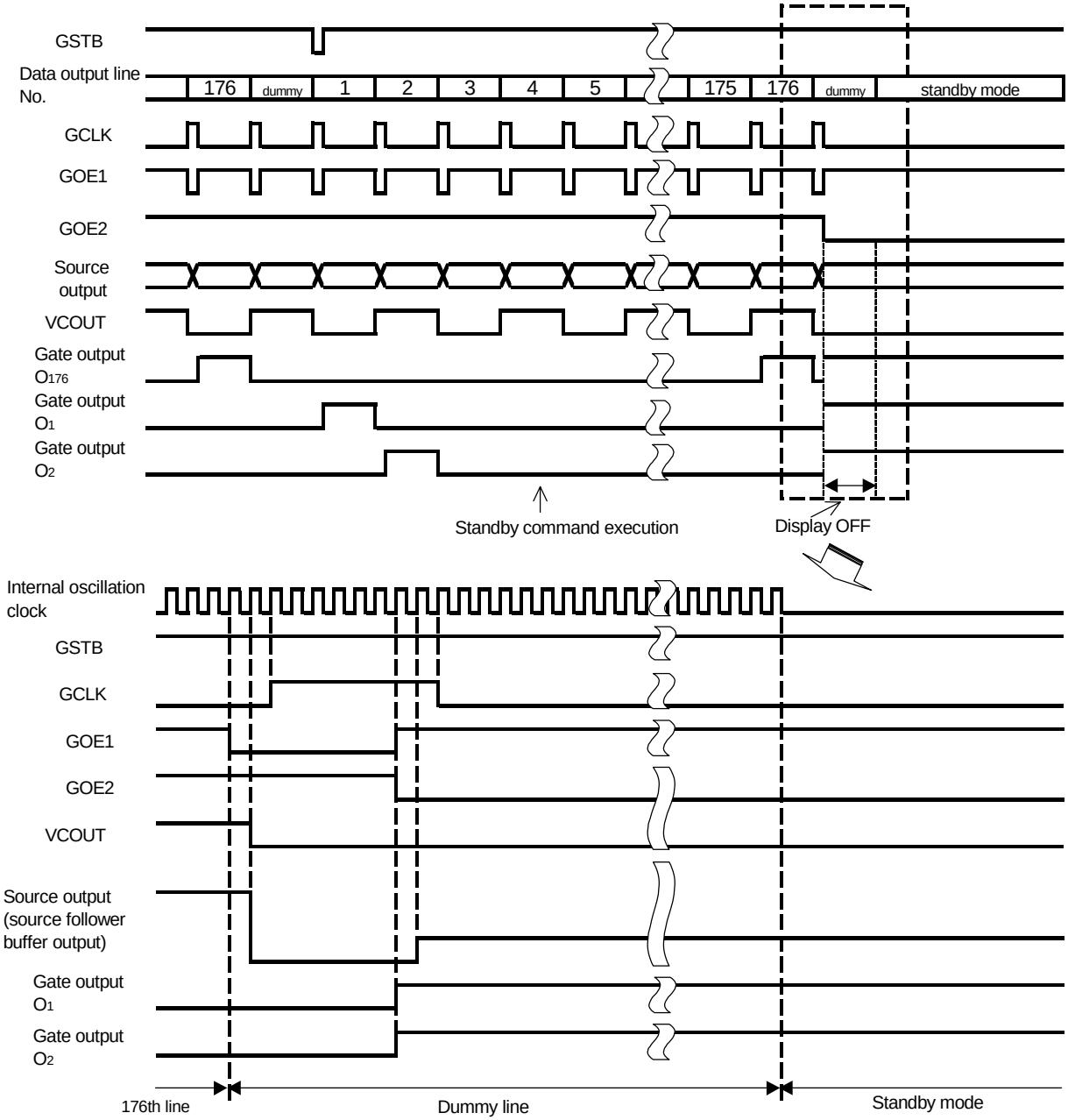
★ **5.4 Display Timing Generator**

The display timing generator generates the timing signals for the internal timing of the source driver and for the gate driver. The output timings for normal operation, for normal operation → standby mode, and for standby mode → normal operation, are shown below.

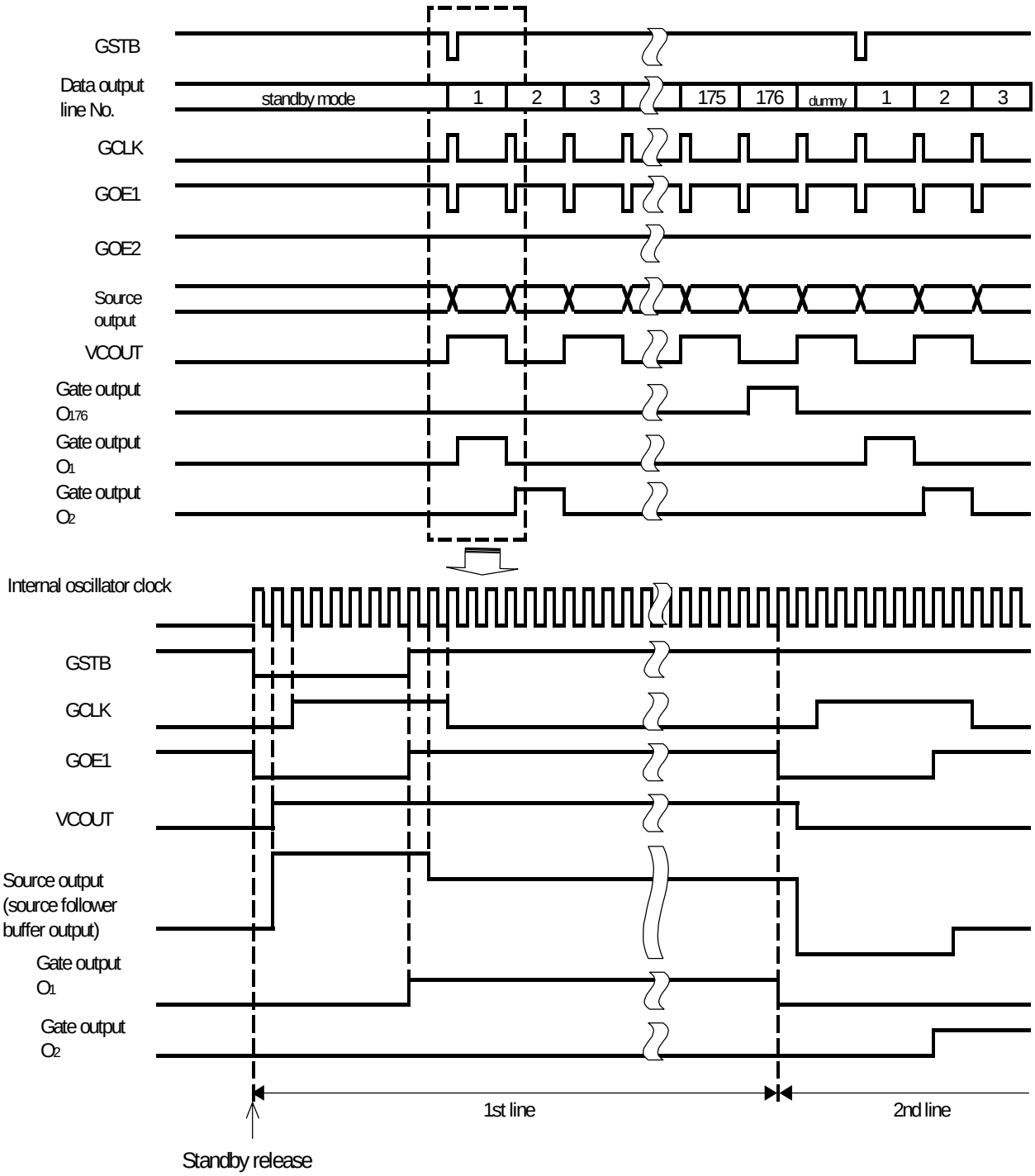
★ **Figure 5–10. During Normal Operation (during line inversion)**



★ **Figure 5–11. Normal Operation → Standby Input (during line inversion)**



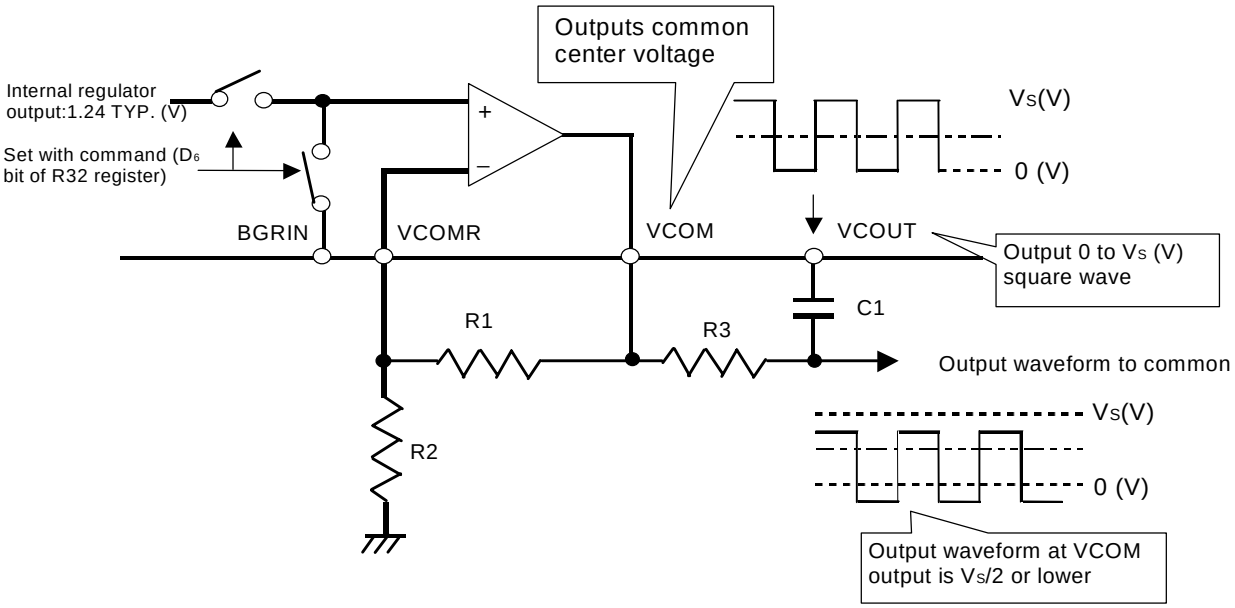
★ **Figure 5–12. Standby → Return to Normal Operation (during line inversion)**



★ **5.5 Common Adjustment Circuit**

To generate common output, the center voltage of the common waveform is output from the VCOM pin along with output of a 0 to V_S (V) square waveform from the VCOUT pin. The level of the VCOM output can be adjusted using as external resistor.

Figure 5–13. Common Adjustment Circuit



The BCOM voltage formulas are shown below.

<When internal power supply is used (D_6 of R32 = 0)>

COM voltage = (1+R1/R2) x (VBGR/3)

VBGR = 1.2 V TYP.

<When external power supply is used (D_6 of R32 = 1)>

COM voltage = (1+R1/R2) x (VBGRIN/9)

VBGRIN = External supply voltage (voltage input from BGRIN)

<Recommended values for R1, R2, R3, C1>

Use the values listed below as a guideline. The user is responsible for ultimately determining the resistance values and recommended values based on careful evaluation on actual panels.

R1: 200 kΩ

R2: 51 kΩ to 100 kΩ

R3: 51 kΩ to 100 kΩ

C1: 10 μF

5.6 Square Wave Signal Generation Circuit

★ This circuit generates a common square wave signal. A 0 to V_S (V) square wave is output from the BCOUT pin.

5.7 Reference Voltage Generator

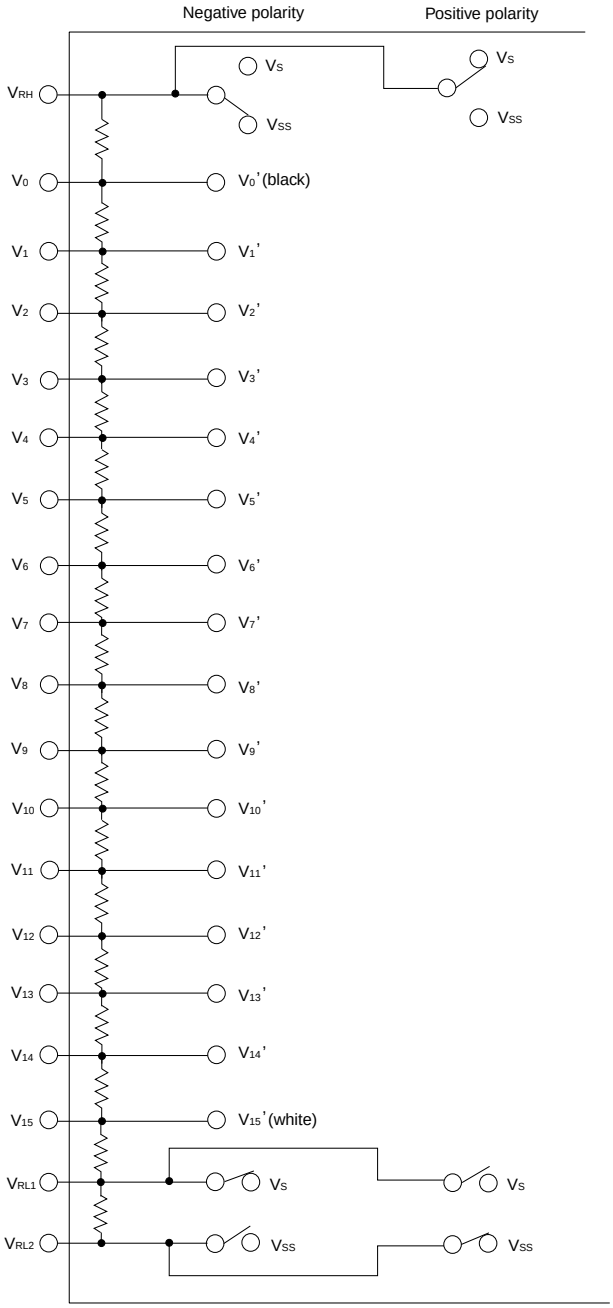
The μPD161620 has a reference voltage generator for the voltage regulator.

★ **5.8 γ-Curve Correction Power Supply Circuit for Cases of Unbalanced Driving**

The μPD161620 includes a γ-curve correction power supply circuit for cases of unbalanced driving. If the internal γ-curve correction matches the LCD characteristics, no external components are necessary.

Support for unbalanced driving is also provided in this circuit using the resistor between V_{RL1} to V_{RL2} shown in the Figure 5–14.

★ **Figure 5–14. γ-Curve Correction Circuit**

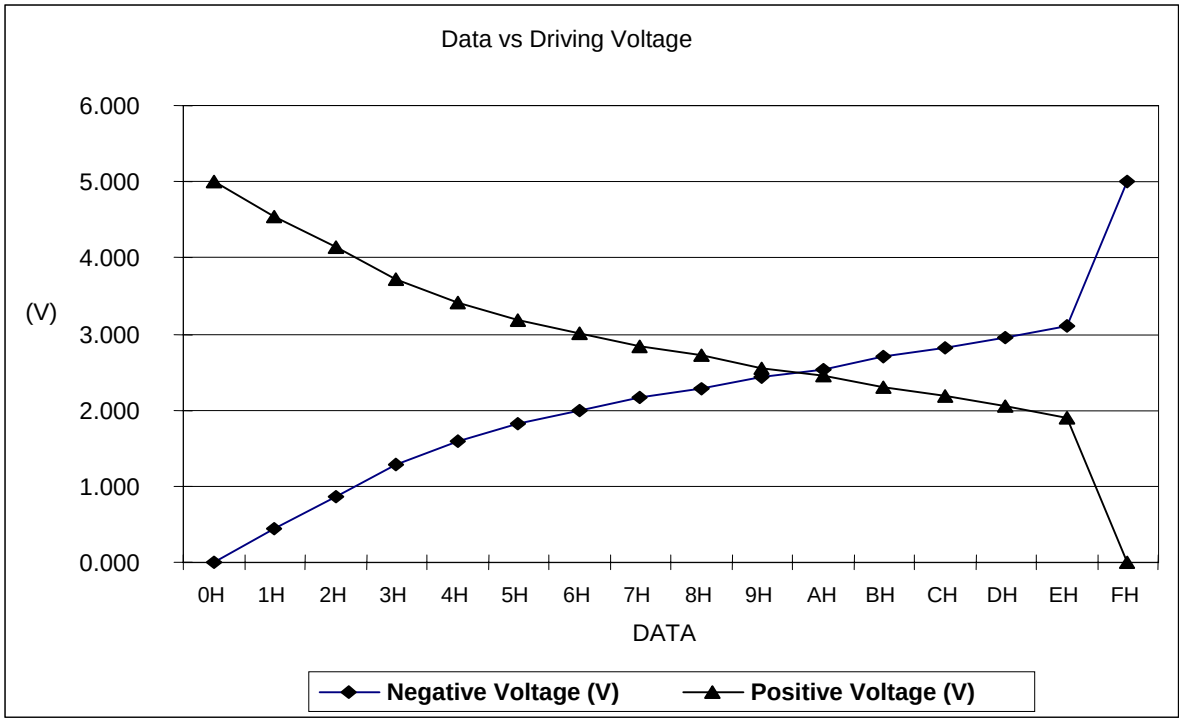


★ **Table 5–7. γ-Curve Correction Circuit**

When in V_S = 5 V

Data	Dn+3	Dn+2	Dn+1	Dn		Resistance(kΩ)		Negative Voltage (V)	Positive Voltage (V)
						r1	0.0		
0H	0	0	0	0	V_0'	r2	18.4	0.000	5.000
1H	0	0	0	1	V_1'	r3	16.8	0.449	4.551
2H	0	0	1	0	V_2'	r4	17.6	0.859	4.141
3H	0	0	1	1	V_3'	r5	12.0	1.289	3.711
4H	0	1	0	0	V_4'	r6	9.6	1.582	3.418
5H	0	1	0	1	V_5'	r7	7.2	1.816	3.184
6H	0	1	1	0	V_6'	r8	7.2	1.992	3.008
7H	0	1	1	1	V_7'	r9	4.8	2.168	2.832
8H	1	0	0	0	V_8'	r10	6.4	2.285	2.715
9H	1	0	0	1	V_9'	r11	4.0	2.441	2.559
AH	1	0	1	0	V_{10}'	r12	6.4	2.539	2.461
BH	1	0	1	1	V_{11}'	r13	4.8	2.695	2.305
CH	1	1	0	0	V_{12}'	r14	5.6	2.813	2.188
DH	1	1	0	1	V_{13}'	r15	6.4	2.949	2.051
EH	1	1	1	0	V_{14}'	r16	77.6	3.105	1.895
FH	1	1	1	1	V_{15}'	r17	0.0	5.000	0.000
						r18	0.0		

rTOTAL = 204.8



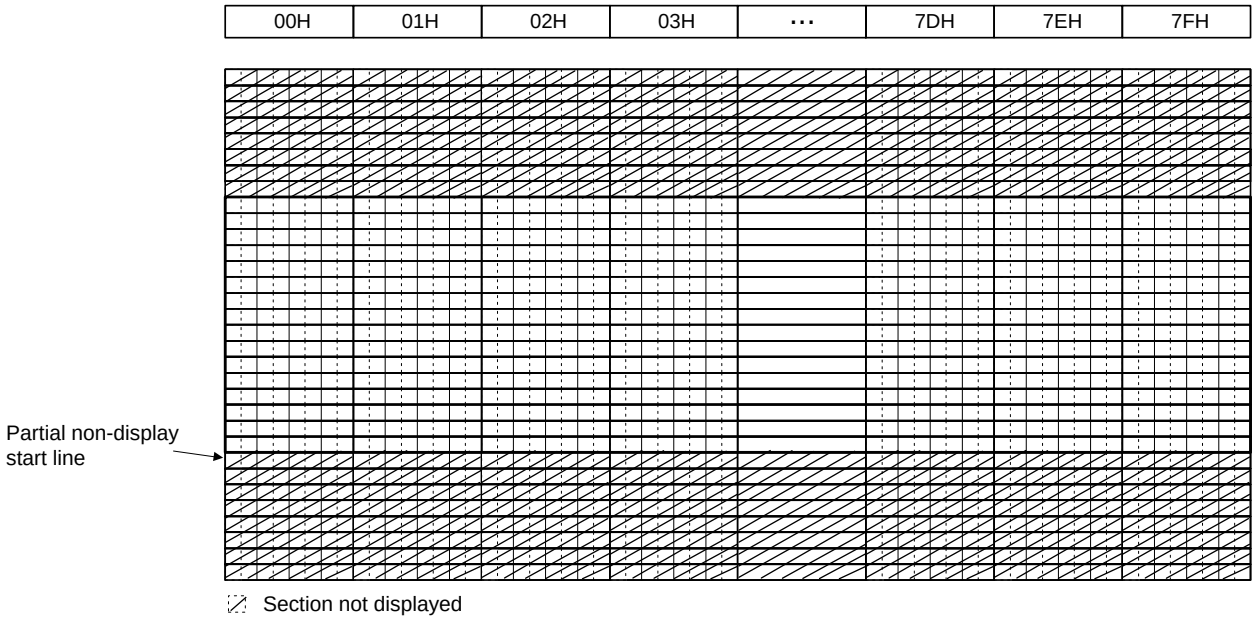
5.9 Partial Display Mode

The μPD161620 is provided with a function that allows sections within the screen to be displayed separately (partial display mode). The start line of the area to be displayed in partial display mode is set using the partial display area start line register (R28, R29), the number of lines in the area to be displayed is set using the partial display area line number register (R30, 31), and the color of the area not to be displayed is set using the partial off area color register
★ (R27). If "1" is set in the partial display area line count registers (R30, R31), the partial display areas each become 1 line. If "0" is set, there are no partial display areas but only normal display areas.

The non-display area indicated by R28 and R30 is called Partial 1, and the non-display area indicates by R29 and R31 is called Partial 2. The Partial 2 setting is enabled only when the Partial 1 setting has been performed (when R30 ≠ 0). Therefore, to set only one area as a non-display area, perform only the setting for Partial 1.

Low power consumption cannot be achieved if only the partial mode is set. If low power consumption is required, the mode must be switched to the 8-clor mode.

Figure 5–15. Partial Display Mode



Cautions 1. The "scroll step count register (R26)" command is ignored in the partial display mode.

★ **2. The specified partial areas must not directly overlap, and the Partial 1 area and Partial 2 area must be separated by at least one line. If the areas overlap, only the Partial 1 settings are valid, and partial display is not performed for the Partial 2 area.**

★ **3. In the case of the 4096 mode, only "00H" can be set to the partial OFF area color register (R27). In the case of the 8-color mode, any value from 00H to 07h can be set.**

The following sequence is recommended to avoid display malfunction when switching from normal display mode to partial display mode and vice versa.

(1) Recommended sequence for switching from normal display mode to partial display mode

DISP = 0	R0	D_6	<1> Display off
↓			
PGDn setting	R27	D_2 | D_0	<2> Partial off area color register setting [Note 1]
↓			
Display data overwrite (for partial display)			<3> Display data overwrite [Note 1]
↓			
P1SLn, P2SLn setting	R28, R29	D_7 | D_0	<4> Partial display area start line setting [Note 1]
↓			
P1AWn, P2AWn setting	R30, R31	D_7 | D_0	<5> Partial display area line number setting [Note 1]
↓			
DTY = 1, COLOR = 1	R1	D_1, D_2	<6> Partial display mode, 8-color mode [Note 2]
↓			
DISP = 1	R0	D_6	<7> Display on

Notes 1. <2> to <5> can be executed in any order.

2. <6> must be executed after <4> and <5> have been set.

(2) Recommended sequence for switching from partial display mode to normal display mode

DISP = 0	R0	D_6	<1> Display off
↓			
Display data overwrite (for normal display)			<2> Display data overwrite [Note]
↓			
DTY = 0, COLOR = 0	R1	D_1, D_2	<3> Partial display mode, 4096-color mode[Note]
↓			
DISP = 1	R0	D_6	<4> Display on

Note <2> to <3> can be executed in any order.

(3) Recommended sequence for switching from partial display mode to partial display mode (switching the partial display area)

DISP = 0	R0	D_6	<1> Display off
↓			
(Display data overwrite)			<2> Display data overwrite Notes [Note 1, 2]
↓			
P1SLn, P2SLn setting	R28, R29	D_7 | D_0	<3> Partial display area start line setting [Note 1]
↓			
P1AWn, P2AWn setting	R30, R31	D_7 | D_0	<4> Partial display area line number setting [Note 1]
↓			
DTY = 1	R1	D_1	<5> Partial display mode [Note 3]
↓			
DISP = 1	R0	D_6	<6> Display on

Notes 1. <2> to <4> can be executed in any order.

2. Execute <2> only when necessary.

3. <5> must be executed after <3> and <4> have been set.

(4) Partial display setting examples

Setting A-1

Register	Setting Value	Details of Setting Value
Partial display area start line register (R28, R29)	00H	Sets Y address 00H
Partial display area line number register (R30, R31)	57H	Sets an area of 88 lines

Setting A-2

Register	Setting Value	Details of Setting Value
Partial display area start line register (R28, R29)	58H	Sets Y address 58H
Partial display area line number register (R30, R31)	57H	Sets an area of 88 lines

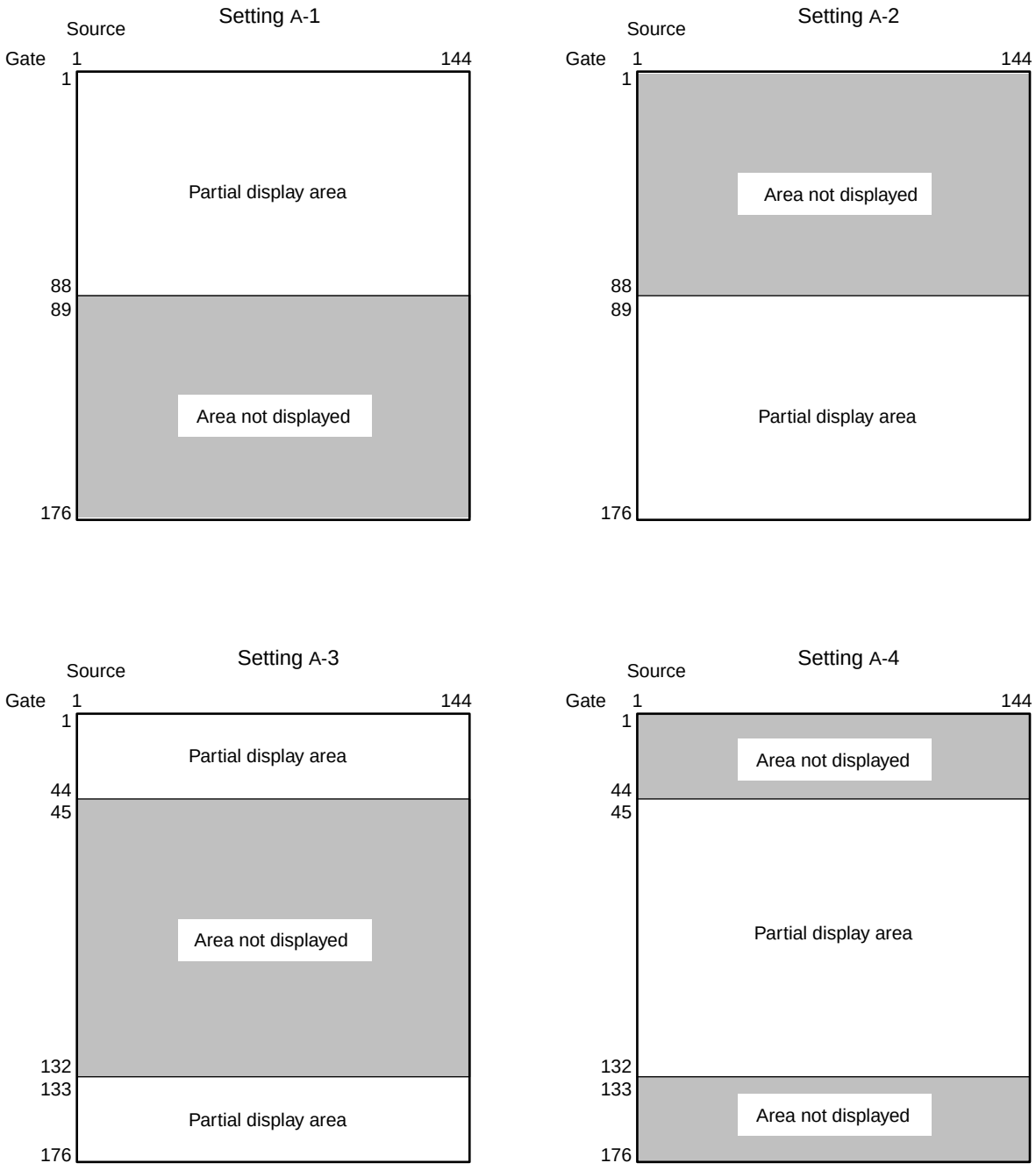
Setting A-3

Register	Setting Value	Details of Setting Value
Partial display area start line register (R28, R29)	84H	Sets Y address 84H
Partial display area line number register (R30, R31)	57H	Sets an area of 88 lines

Setting A-4

Register	Setting Value	Details of Setting Value
Partial display area start line register (R28, R29)	2CH	Sets Y address 2CH
Partial display area line number register (R30, R31)	57H	Sets an area of 88 lines

Figure 5–16. Partial Display Setting Examples



5.10 Screen Scroll

The μPD161620 has a screen scroll function. Any area of the screen can be scrolled by using the scroll area start line register (R22), scroll area line count register (R24), and scroll step count register (R26) to set the Y address of the top line of the area to be scrolled, the number of lines of the area to be scrolled, and the scroll step number, respectively.

Note that in partial mode, the screen scroll function is disabled.

Table 5–8. Scroll Area Start Line Register (R22)

SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0	Start Line Y Address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
0	0	0	0	0	0	1	0	02H
0	0	0	0	0	0	1	1	03H
				↓				↓
1	0	1	0	1	1	0	1	ADH
1	0	1	0	1	1	1	0	AEH
1	0	1	0	1	1	1	1	AFH

Table 5–9. Scroll Area Line Count Register (R24)

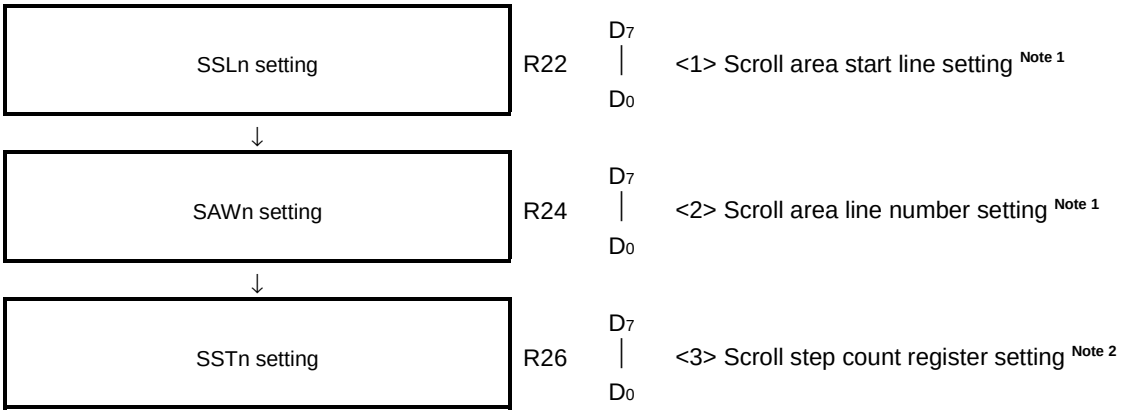
SAW7	SAW6	SAW5	SAW4	SAW3	SAW2	SAW1	SAW0	Scroll Area Line Number
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
				↓				↓
1	0	1	0	1	1	0	1	174
1	0	1	0	1	1	1	0	175
1	0	1	0	1	1	1	1	176

Table 5–10. Scroll Step count Register (R26)

SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0	Scroll Step Number
0	0	0	0	0	0	0	0	0 (No scroll)
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
				↓				↓
1	0	1	0	1	1	0	1	173
1	0	1	0	1	1	1	0	174
1	0	1	0	1	1	1	1	175

Scrolling must be set using the following sequence.

(1) Recommended sequence



Notes 1. <1> to <2> can be executed in any order.

2. <3> must be executed after <1> and <2> have been set.

Remark Set SSTn to 00H to disable the scroll operation. No particular sequence is required for this.

Cautions 1. If the sum of the values of SSLn and SAWn is 176 (AFH) or over, it is invalid (no scroll operation).

2. Set the step number SSTn so that it does not exceed the line number SAWn. If a value exceeding SAWn is set, it will be invalid (no scroll operation).

(2) Scroll setting examples

Setting A-1

Register	Setting Value	Details of Setting Value
Scroll area start line register (R22)	00H	Sets Y address 00H
Scroll area line count register (R24)	AFH	Sets an area of 176 lines

Setting A-2

Register	Setting Value	Details of Setting Value
Scroll area start line register (R22)	00H	Sets Y address 00H
Scroll area line count register (R24)	57H	Sets an area of 88 lines

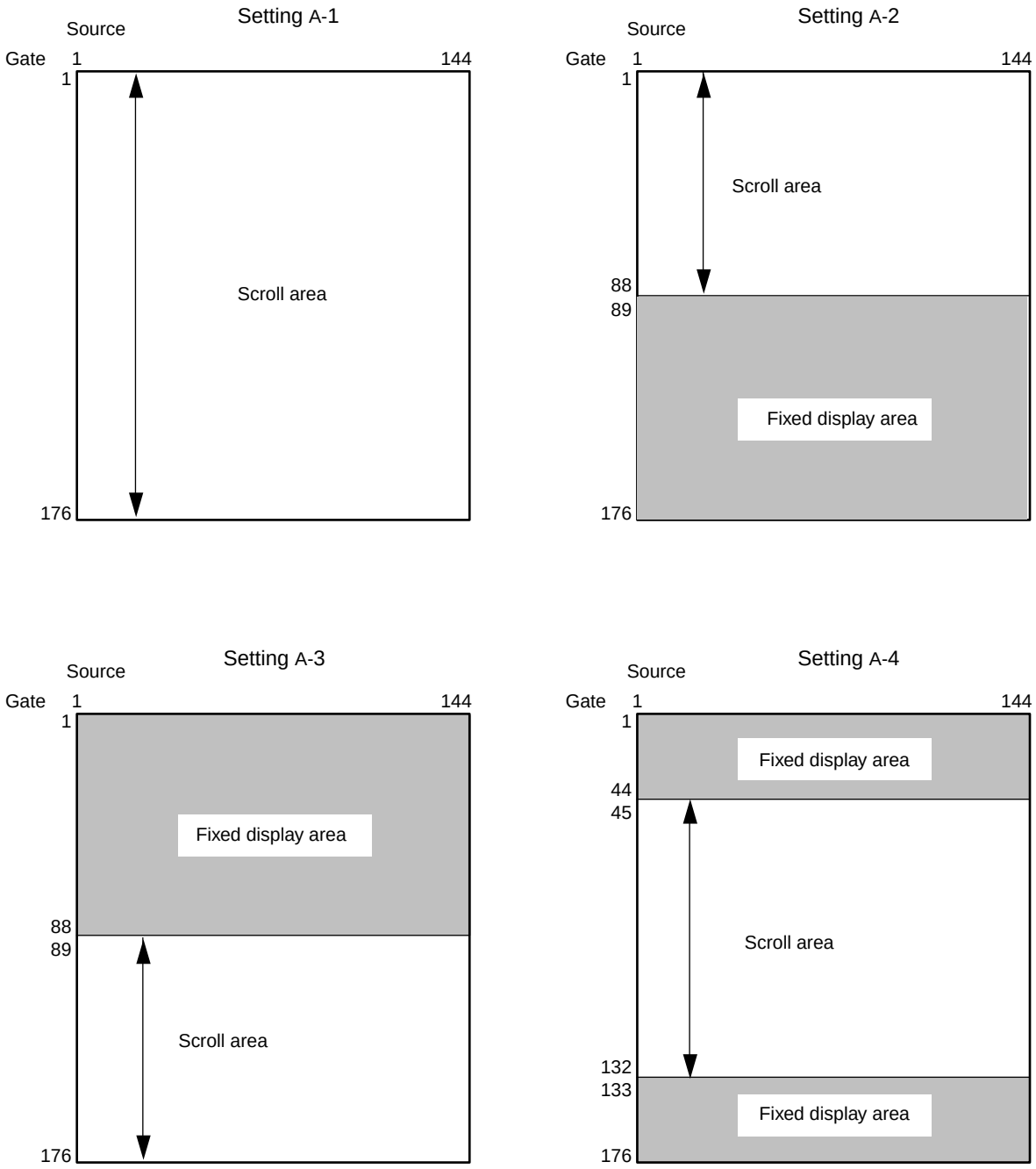
Setting A-3

Register	Setting Value	Details of Setting Value
Scroll area start line register (R22)	58H	Sets Y address 58H
Scroll area line count register (R24)	57H	Sets an area of 88 lines

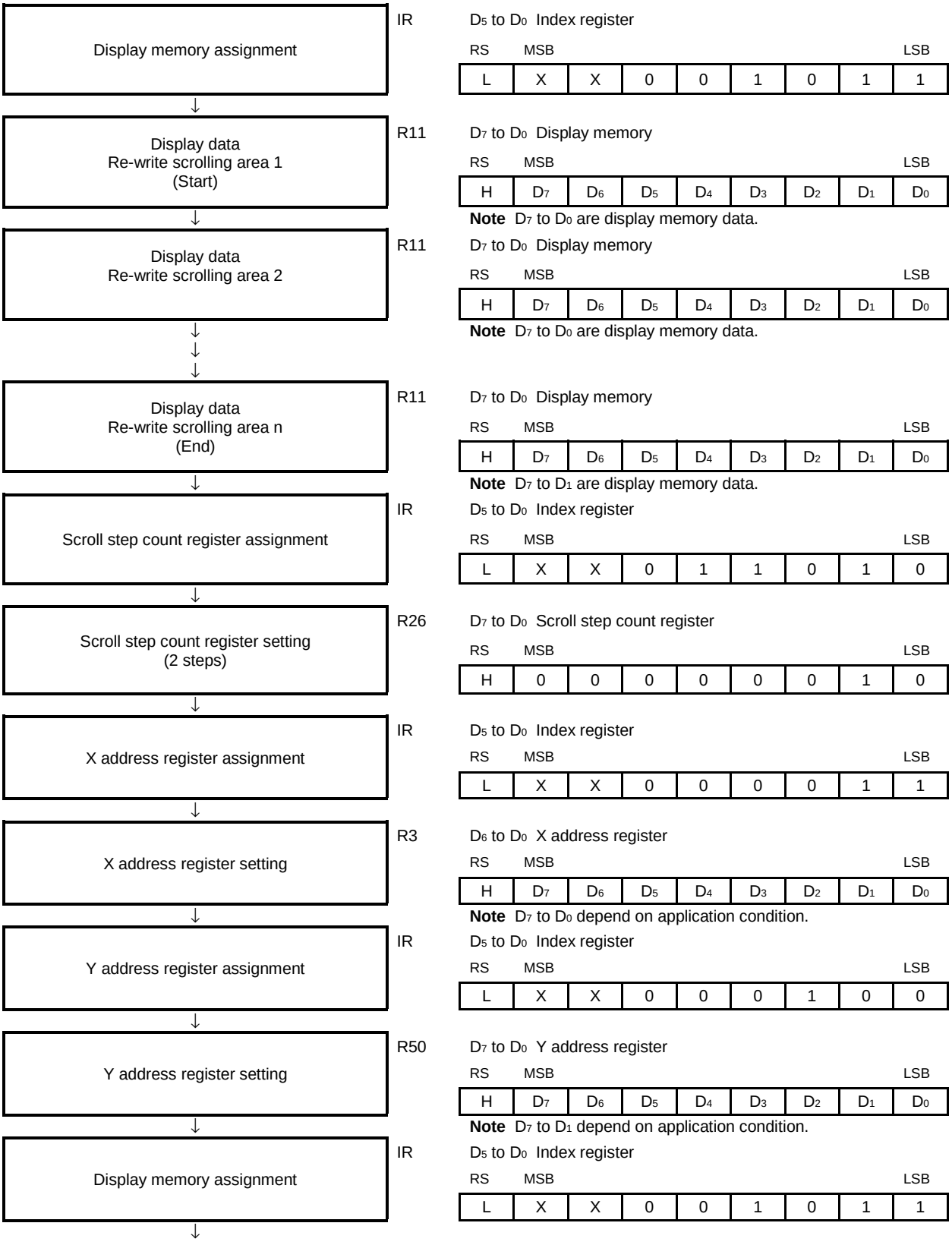
Setting A-4

Register	Setting Value	Details of Setting Value
Scroll area start line register (R22)	2CH	Sets Y address 2CH
Scroll area line count register (R24)	57H	Sets an area of 88 lines

Figure 5–17. Display Scroll Setting Examples



(3) Scroll setting flowchart example


Display memory assignment
IR
D5 to D0 Index register
RS MSB LSB
L X X 0 0 1 0 1 1
Display data
Re-write scrolling area 1
(Start)
R11
D7 to D0 Display memory
RS MSB LSB
H D7 D6 D5 D4 D3 D2 D1 D0
Note D7 to D0 are display memory data.
Display data
Re-write scrolling area 2
R11
D7 to D0 Display memory
RS MSB LSB
H D7 D6 D5 D4 D3 D2 D1 D0
Note D7 to D0 are display memory data.
Display data
Re-write scrolling area n
(End)
R11
D7 to D0 Display memory
RS MSB LSB
H D7 D6 D5 D4 D3 D2 D1 D0
Note D7 to D1 are display memory data.
Scroll step count register assignment
IR
D5 to D0 Index register
RS MSB LSB
L X X 0 1 1 0 1 0
Scroll step count register setting
(2 steps)
R26
D7 to D0 Scroll step count register
RS MSB LSB
H 0 0 0 0 0 0 1 0
X address register assignment
IR
D5 to D0 Index register
RS MSB LSB
L X X 0 0 0 0 1 1
X address register setting
R3
D6 to D0 X address register
RS MSB LSB
H D7 D6 D5 D4 D3 D2 D1 D0
Note D7 to D0 depend on application condition.
Y address register assignment
IR
D5 to D0 Index register
RS MSB LSB
L X X 0 0 0 1 0 0
Y address register setting
R50
D7 to D0 Y address register
RS MSB LSB
H D7 D6 D5 D4 D3 D2 D1 D0
Note D7 to D1 depend on application condition.
Display memory assignment
IR
D5 to D0 Index register
RS MSB LSB
L X X 0 0 1 0 1 1

Display data
Re-write scrolling area 1
(Start)

R11 D_7 to D_0 Display memory

RS	MSB							LSB
H	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Note D_7 to D_0 are display memory data.

↓

Display data
Re-write scrolling area 2

R11 D_7 to D_0 Display memory

RS	MSB							LSB
H	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Note D_7 to D_0 are display memory data.

↓
↓
↓

Display data
Re-write scrolling area n
(End)

R11 D_7 to D_0 Display memory

RS	MSB							LSB
H	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Note D_7 to D_0 are display memory data.
(Repeat)

↓
↓
↓
↓

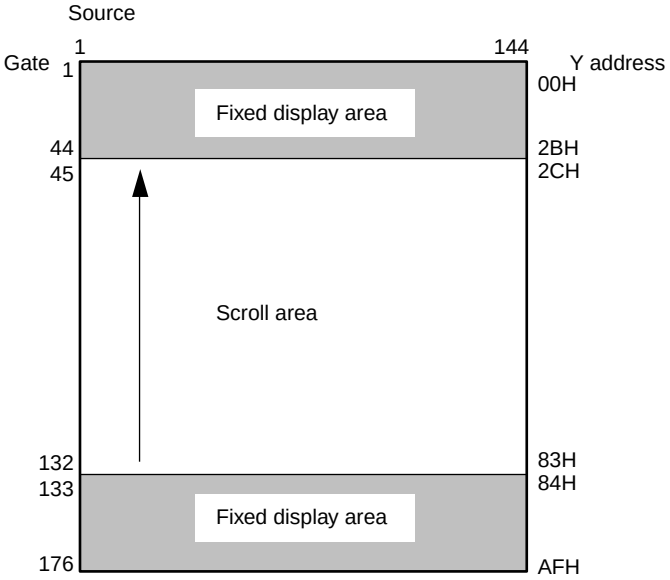
Next transaction

(4)Scroll function example

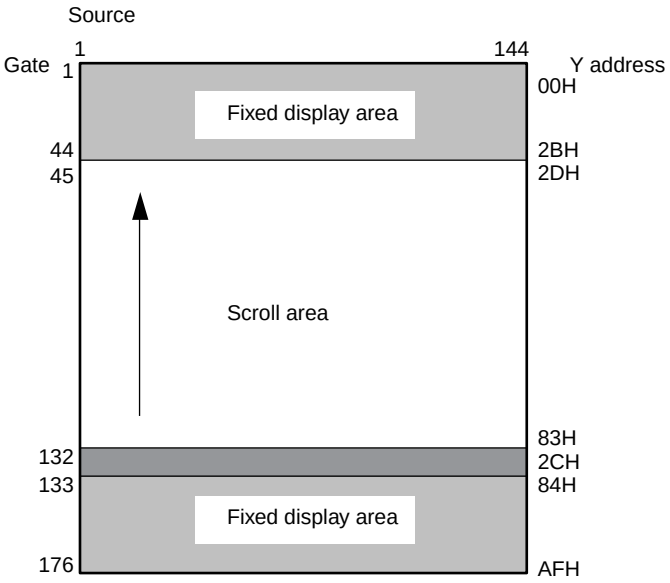
Scroll area start line register (R22): 2CH

Scroll area line count register (R24): 58H

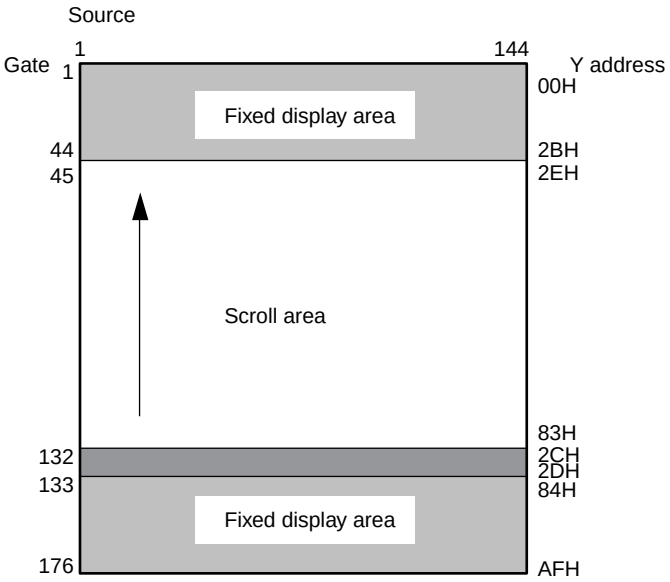
(a)Scroll step count register setting (R26): 00H



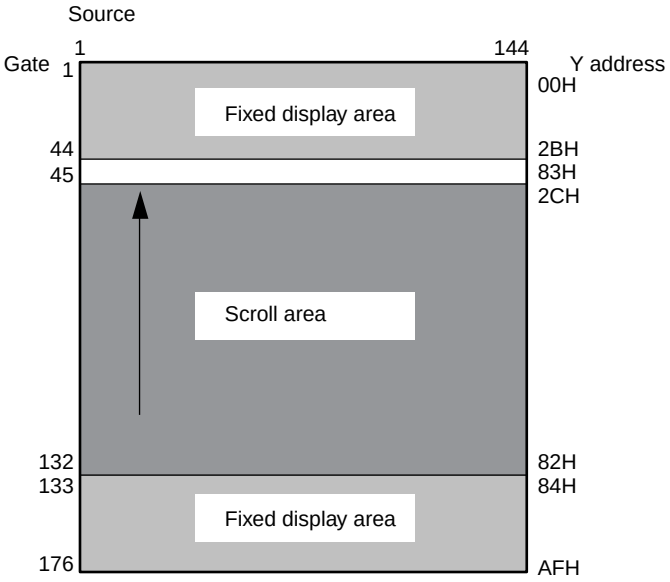
(b)Scroll step count register setting (R26): 01H



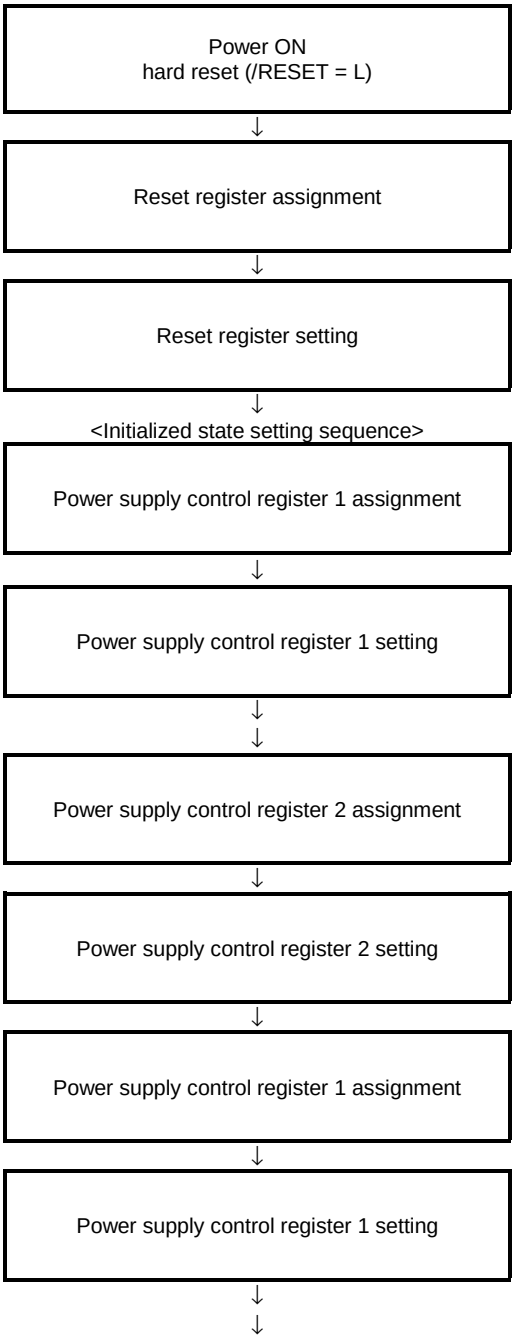
(c)Scroll step count register setting (R26): 02H



(d)Scroll step count register setting (R26): 57H



★ 5.11 Initialization Setting Sequence Example



IR D5 to D0 Index register

RS	MSB							LSB
L	X	X	0	0	0	0	1	0

R2 D7 to D0 Reset

RS	MSB							LSB
H	X	X	X	X	X	X	X	1

IR D5 to D0 Index register

RS	MSB							LSB
L	X	X	1	0	0	0	0	0

R32 D7 to D0 Power supply control register 1

RS	MSB							LSB
H	X	D6	D5	D4	D3	0	0	0

Note D6 to D4 depend on application condition., D3 to D0:gate driver, power supply IC regulator OFF, DC/DC converter OFF

IR D5 to D0 Index register

RS	MSB							LSB
L	X	X	1	0	0	0	1	0

R34 D7 to D0 Power supply control register2

RS	MSB							LSB
H	X	X	X	X	D3	D2	X	X

Note D3, D2 depend on application condition.

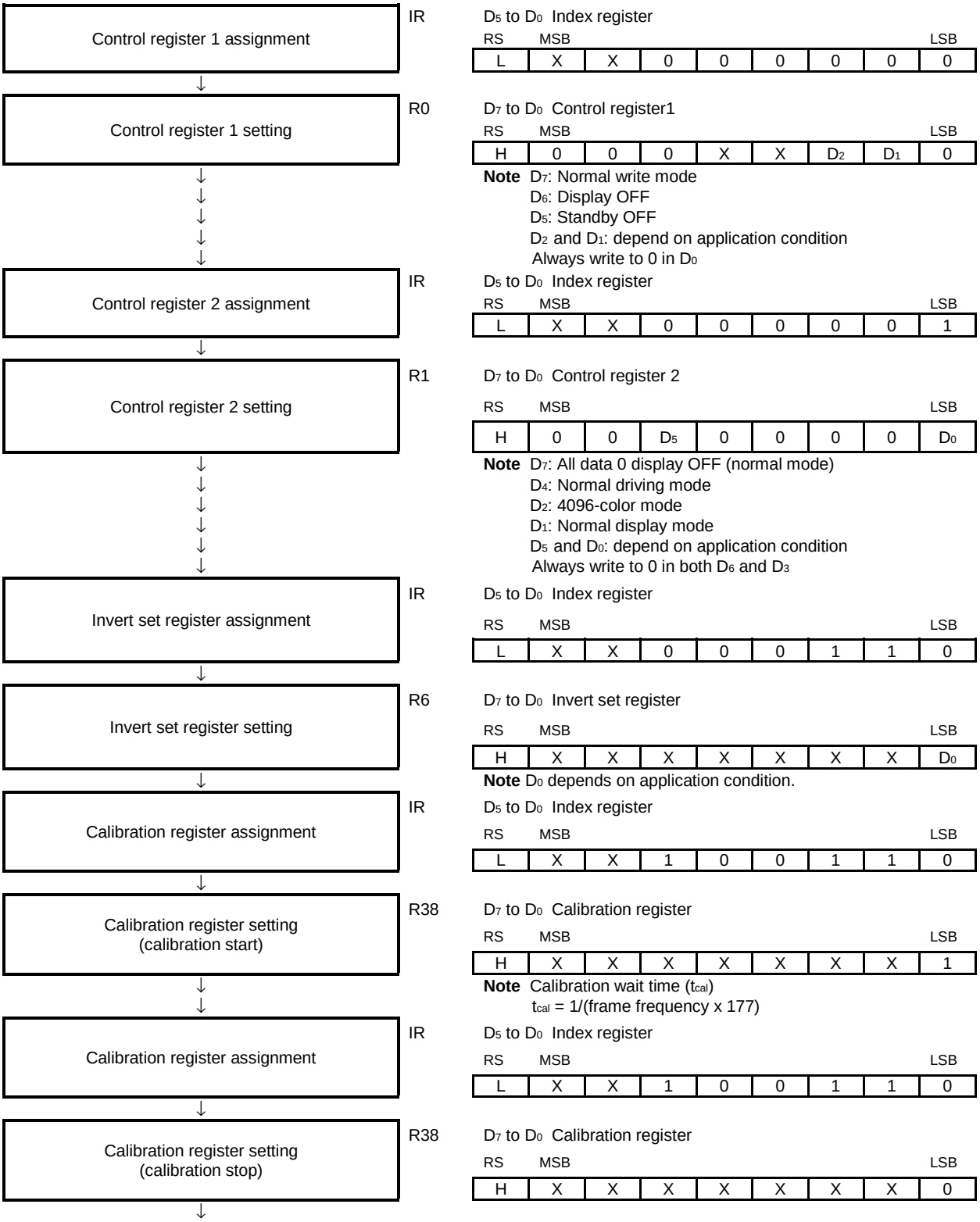
IR D5 to D0 Index register

RS	MSB							LSB
L	X	X	1	0	0	0	0	0

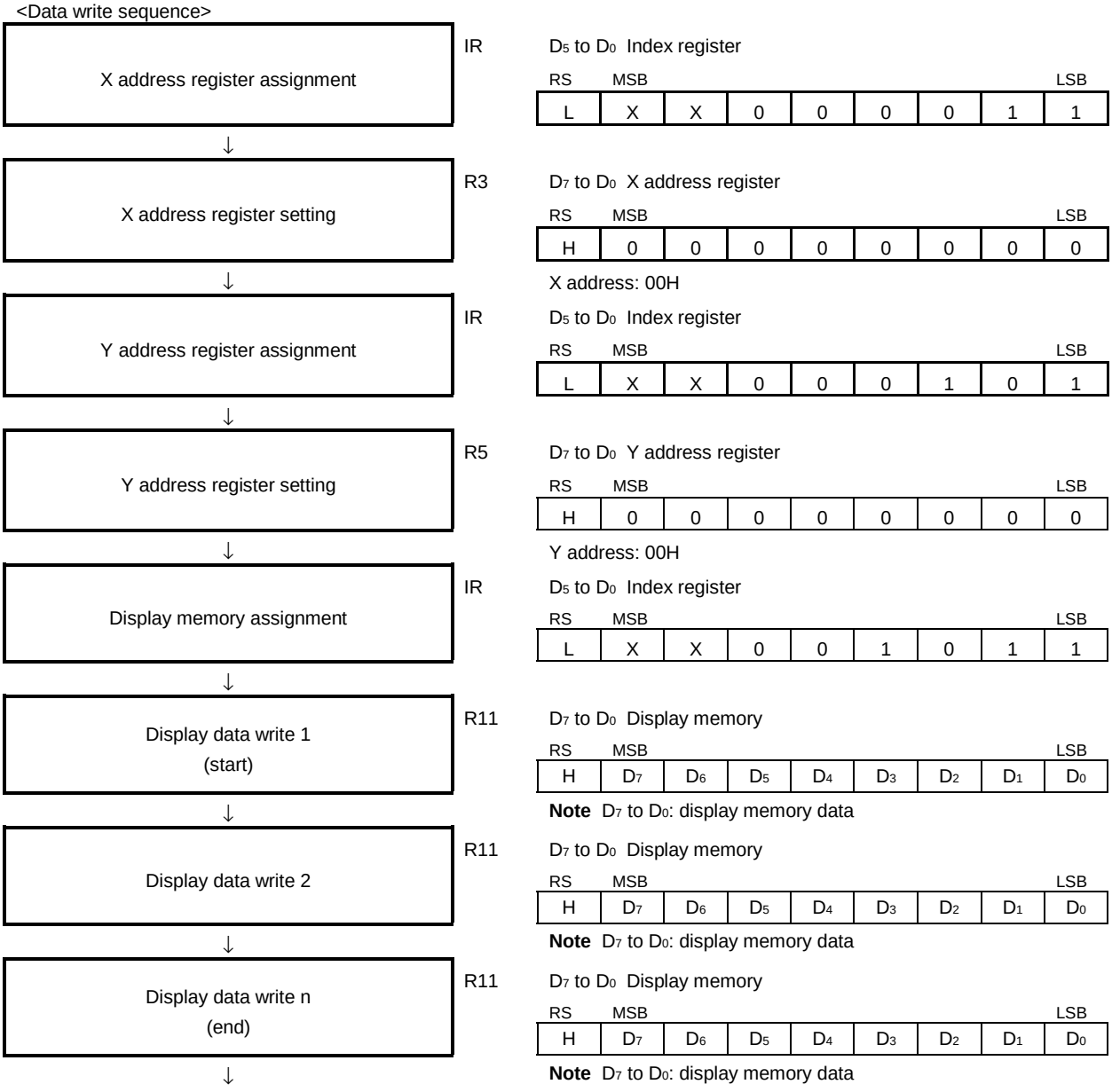
R32 D7 to D0 Power supply control register1

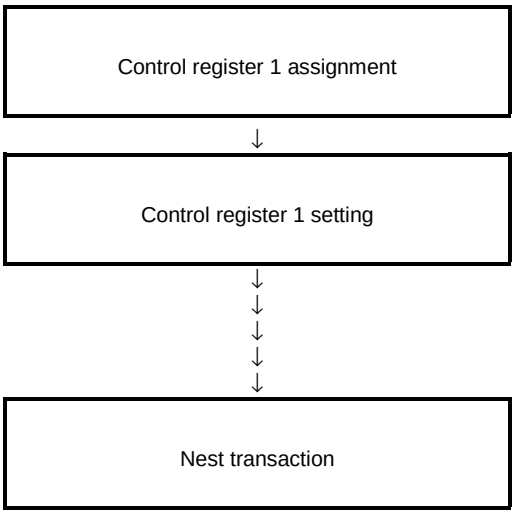
RS	MSB							LSB
H	X	D6	D5	D4	D3	1	1	1

Note D6 to D4 depend on application condition., D3 to D0:gate driver, power supply IC regulator OFF, DC/DC converter OFF


Control register 1 assignment
IR
D5 to D0 Index register
RS MSB LSB
L X X 0 0 0 0 0 0
Control register 1 setting
R0
D7 to D0 Control register1
RS MSB LSB
H 0 0 0 X X D2 D1 0
Note D7: Normal write mode
D6: Display OFF
D5: Standby OFF
D2 and D1: depend on application condition
Always write to 0 in D0
Control register 2 assignment
IR
D5 to D0 Index register
RS MSB LSB
L X X 0 0 0 0 0 1
Control register 2 setting
R1
D7 to D0 Control register 2
RS MSB LSB
H 0 0 D5 0 0 0 0 D0
Note D7: All data 0 display OFF (normal mode)
D4: Normal driving mode
D2: 4096-color mode
D1: Normal display mode
D5 and D0: depend on application condition
Always write to 0 in both D6 and D3
Invert set register assignment
IR
D5 to D0 Index register
RS MSB LSB
L X X 0 0 0 1 1 0
Invert set register setting
R6
D7 to D0 Invert set register
RS MSB LSB
H X X X X X X X D0
Note D0 depends on application condition.
Calibration register assignment
IR
D5 to D0 Index register
RS MSB LSB
L X X 1 0 0 1 1 0
Calibration register setting
(calibration start)
R38
D7 to D0 Calibration register
RS MSB LSB
H X X X X X X X 1
Note Calibration wait time (tcal)
tcal = 1/(frame frequency x 177)
Calibration register assignment
IR
D5 to D0 Index register
RS MSB LSB
L X X 1 0 0 1 1 0
Calibration register setting
(calibration stop)
R38
D7 to D0 Calibration register
RS MSB LSB
H X X X X X X X 0

<Data write sequence>





IR D_5 to D_0 Index register

RS	MSB							LSB
L	X	X	0	0	0	0	0	0

R0 D_7 to D_0 Control register 1

RS	MSB							LSB
H	0	1	0	X	X	D_2	D_1	0

Note D_7: Normal write mode
D_6: Display ON
D_5: Standby OFF
D_2 and D_1: depend on application condition
Always write to 0 in D_0

6. RESET

If the /RESET input becomes L or the reset command is input, the internal timing generator is initialized. The reset command will also initialize each register to its default value. These default values are listed in the table below.

	Register		/RESET Pin Note 1	Reset Command	Default Value
	Index register	IR	X	O	00H
	Control register 1	R0	X	O	00H
	Control register 2	R1	X	O	00H
★	X address register	R3	X	O	00H
	Y address register	R5	X	O	00H
	Reverse setting register	R6	X	O	00H
	Display memory Note 2	R11	X	X	-
	Scroll area start line register	R22	X	O	00H
	Scroll area line count register	R24	X	O	00H
	Scroll step count register	R26	X	O	00H
	Partial off area color register	R27	X	O	00H
	Partial 1 display area start line register	R28	X	O	00H
	Partial 2 display area start line register	R29	X	O	00H
	Partial 1 display area line count register	R30	X	O	00H
	Partial 2 display area line count register	R31	X	O	00H
	Power supply control register 1	R32	X	O	00H
	Power supply control register 2	R34	X	O	00H
	Calibration register Note 3	R38	X	O	01H
	Output port register	R42	X	O	00H
	Input port register	R43	X	O	00H
★	Test mode	R44 to R47	X	O	00H

O: Default value set, X: Default value not set

Notes 1. The internal counters are initialized only by a reset from the /RESET pin. Be sure to perform reset via the /RESET pin at power application.

2. The contents of RAM are saved in the case of both reset by /RESET pin and reset by reset command. Note that the RAM contents are T.B.D. immediately after the power is turned on.

3. The following value is set as the calibration setting time, t_{cal}, in a reset by reset command.

$t_{cal} = 1/f_{OSC} \times 32$

★ **Remark** T.B.D. (to be determined.)

7. COMMAND

★ 7.1 Command List

	Index Register						Register Name		R/W	Data Bits							
	5	4	3	2	1	0				7	6	5	4	3	2	1	0
1st byte							IR	Index register	W			IR5	IR4	IR3	IR2	IR1	IR0
2nd byte	0	0	0	0	0	0	R0	Control register 1	R/W	RMW	DISP	STBY			ADX	ADC	
	0	0	0	0	0	1	R1	Control register 2	R/W	FDM		DTX	LPM		COLOR	DTY	INC
	0	0	0	0	1	0	R2	Reset	W								CRES
	0	0	0	0	1	1	R3	X address register	R/W	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0
	0	0	0	1	0	0	R4										
	0	0	0	1	0	1	R5	Y address register	R/W	YA7	YA6	YA5	YA4	YA3	YA2	YA1	YA0
	0	0	0	1	1	0	R6	Reverse setting register	R/W								INV
	0	0	0	1	1	1	R7										
	0	0	1	0	0	0	R8										
	0	0	1	0	0	1	R9										
	0	0	1	0	1	0	R10										
	0	0	1	0	1	1	R11	Display memory	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	0	1	1	0	0	R12										
	0	0	1	1	0	1	R13										
	0	0	1	1	1	0	R14										
	0	0	1	1	1	1	R15										
	0	1	0	0	0	0	R16										
	0	1	0	0	0	1	R17										
	0	1	0	0	1	0	R18										
	0	1	0	0	1	1	R19										
	0	1	0	1	0	0	R20										
	0	1	0	1	0	1	R21										
	0	1	0	1	1	0	R22	Scroll area start line register	R/W	SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0
	0	1	0	1	1	1	R23										
	0	1	1	0	0	0	R24	Scroll area line count register	R/W	SAW7	SAW6	SAW5	SAW4	SAW3	SAW2	SAW1	SAW0
	0	1	1	0	0	1	R25										
	0	1	1	0	1	0	R26	Scroll step count register	R/W	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0
	0	1	1	0	1	1	R27	Partial off area color register	R/W						PGD2	PGD1	PGD0
	0	1	1	1	0	0	R28	Partial 1 display area start line register	R/W	P1SL7	P1SL6	P1SL5	P1SL4	P1SL3	P1SL2	P1SL1	P1SL0
	0	1	1	1	0	1	R29	Partial 2 display area start line register	R/W	P2SL7	P2SL6	P2SL5	P2SL4	P2SL3	P2SL2	P2SL1	P2SL0
	0	1	1	1	1	0	R30	Partial 1 display area line count register	R/W	P1AW7	P1AW6	P1AW5	P1AW4	P1AW3	P1AW2	P1AW1	P1AW0
	0	1	1	1	1	1	R31	Partial 2 display area line count register	R/W	P2AW7	P2AW6	P2AW5	P2AW4	P2AW3	P2AW2	P2AW1	P2AW0
	1	0	0	0	0	0	R32	Power supply control register 1	R/W		BGRS	VCE	VCD2	PVCOM	RGONG	RGONP	DCON
	1	0	0	0	0	1	R33										
	1	0	0	0	1	0	R34	Power supply control register 2	R/W					VCD12	VCD11		
	1	0	0	0	1	1	R35										
	1	0	0	1	0	0	R36										
	1	0	0	1	0	1	R37										
	1	0	0	1	1	0	R38	Calibration register	R/W								OC
	1	0	0	1	1	1	R39										
	1	0	1	0	0	0	R40										
	1	0	1	0	0	1	R41										
	1	0	1	0	1	0	R42	Output port register	W					OP3	OP2	OP1	OP0
	1	0	1	0	1	1	R43	Input port register	R					IP3	IP2	IP1	IP0
	1	0	1	1	0	0	R44	Test mode	R/W								
	1	0	1	1	0	1	R45	Test mode	R/W								
	1	0	1	1	1	0	R46	Test mode	R/W								
	1	0	1	1	1	1	R47	Test mode	R/W								
	1	1	0	0	0	0	R48										
	1	1	0	0	0	1	R49										
	1	1	0	0	1	0	R50										
	1	1	0	0	1	1	R51										
	1	1	0	1	0	0	R52										
	1	1	0	1	0	1	R53										
	1	1	0	1	1	0	R54										
	1	1	0	1	1	1	R55										
	1	1	1	0	0	0	R56										
	1	1	1	0	0	1	R57										
	1	1	1	0	1	0	R58										
	1	1	1	0	1	1	R59										
	1	1	1	1	0	0	R60										
	1	1	1	1	0	1	R61										
	1	1	1	1	1	0	R62										
	1	1	1	1	1	1	R63										

Remark ▭ These registers cannot be used.

Cautions 1. If a write-only register is read, invalid data will be output.

★ **Also, the RS signal during the write operation becomes invalid.**

2. A low level is output when an unused register is read.

7.2 Command Explanation

(1/4)

Resistor	Bit	Symbol	Function
★ R0	D_7	RMW	This bit enables/disables use of the read-modify-write mode function. Perform read/write switching in the read-modify-write mode at every 2-byte access in the 1-pixel/2-byte mode. Similarly, in the 2-ixel/3-byte mode, perform read/write switching at every 3-byte access 0: Address is incremented by one each time a display data read or write 1: Read modify write mode (address is incremented by one each time a display data write only)
	D_6	DISP	This bit switches display ON/OFF. When display OFF is selected, output is performed as when all the data is “1”, regardless of the internal RAM data. (In the case of normally white, white display is performed.) This command is executed from the time the next line data is output. 0: Display off (All output pins are V_{SS} level, OSC and DC/DC converter are working) 1: Display on
	D_5	STBY	This bit selects the standby function. When the standby function is selected, a display OFF operation is executed and the amplifiers at each output stage and the operation of internal oscillation circuit are stopped. However, standby control cannot be performed for the gate IC (μ PD161640) connected to μ PD161620 and the power supply IC (μ PD161660). Therefore, after executing the standby function using this bit, set both the regulator for the gate IC and power supply IC to off and set the DC/DC converter to OFF. For the sequence, refer to the preliminary product information machine of the μ PD161660. Note that when releasing standby, perform the opposite operation, i.e., after setting the DC/DC converter to ON and setting the regulators of the gate IC and power supply IC to ON, execute the normal operation command. 0: Normal operation 1: Stand-by function (Display read off from RAM, stop both OSC and VCOM, display off = entire data is output as 1)
	D_2	ADX	Switches X address addressing X address direction
	D_1	ADC	Column address direction
★ R1	D_7	FDM	This bit does not depend on the internal RAM data. This function performs output in the same way as when all the data is “0”. (In the case of normally white, black display is performed.) This command is executed from the time the next line data is output. 0: Normal operation 1: RAM data is ignored and the entire data is output as 0.
	D_5	DTX	This bit selects the method for transferring data to internal RAM. 0: 2-pixel / 3-byte 1: 1-pixel / 2-byte
	D_4	LPM	This bit is used when setting the gate IC (μ PD161640) and power supply IC (μ PD161660) to the low-power mode. When the low-power mode is selected, the LPMG pin and the LPMP pin signals change from low to high (output changes immediately following command execution.). The LPMG pin must be connected to the LPM pin of the gate IC, and the LPMP pin must be connected to the LPM pin of the power supply IC. 0: Normal 1: Low power mode

(2/4)

	Resistor	Bit	Symbol	Function
		D_2	COLOR	This pin switches the 4096-color mode and the 8-color mode. When the 8-color mode is selected, low power supply can be selected in order to stop the amplifier at each output stage. In the 8-color mode, the value of the MSB of the internal RAM data is used as the color data. This command is executed following transfer from the time the next line data is output. 0: 4096-color mode (12 bits/pixels) 1: 8-color mode (3 bits/pixels)
		D_1	DTY	This pin selects the partial function. When the partial function s selected in the 4096-color mode, set the partial-OFF area-color selection register (R27) to 00H. In the 8-color mode, the partial OFF area color can be set to any value from 00H to 07 H. The power consumption cannot be reduced with the partial function. To reduce the power consumption, select the 8-color mode. This command is executed following transfer from the time the next line data is output. 0: Normal display mode 1: Partial display mode
		D_0	INC	This pin selects the address increment direction. In the case of the 8-bit parallel interface mode and the serial interface mode, when Y address increment is selected, only the 1-pixel/2-byte mode can be selected as the data transfer mode. However, when X address increment is selected, both the 1-pixel/2-byte and 2-pixel/3-byte modes can be selected. 0: X address increment 1: Y address increment
★	R2	D_0	CRES	Command reset function. Be sure to execute this bit after power ON. Command reset automatically clears this bit following execution (CRES = 01H). Therefore, it is not necessary to set 0 (select normal operation) again by software. Moreover, since the time required for the value of this bit to change (1 → 0) following command reset execution is extremely short, it is not necessary to secure time until the next command is set following command reset setting. 0: Normal operation 1: Command reset
★	R3	D_7 to D_0	XA_7 to XA_0	This register sets the X address. Set a value between 00H and 8FH.
★	R5	D_7 to D_0	YA_n	This register sets the Y address. Set a value between 00H and 8FH.
★	R6	D_0	INV	This bit selects between the line inversion function and the frame inversion function. The mode selected by this command is executed from the start of the next scan after the gate scan in progress when this command was executed has completed 176 lines. When the reset command is input, the INV register is initialized. 0: Line inversion with same line. 0: Line inversion 1: Frame inversion
★	R11	D_7 to D_0	D_n	These bits are used for reading/writing data from /to display memory (internal RAM).
	R22	D_7 to D_0	SSL_n	Scroll area start line register (00H to AFH)
	R24	D_7 to D_0	SAW_n	Scroll area line count register (00H to AFH)
	R26	D_7 to D_0	SST_n	Scroll step count register (00H to AFH), invalid in partial display mode

(3/4)

Resistor	Bit	Symbol	Function
★ R27	D_2 to D_0	PGD_n	Partial off area color register (000H to 111H) The relationship between each color data and the bits of this register is as follows. This relationship does not depend on the ADX and ADC values D_{11} to D_8: PGD0 D_7 to D_4: PGD1 D_3 to D_0: PGD2
R28	D_7 to D_0	$P1SL_n$	Partial1 display area start line register (00H to AFH)
R29	D_7 to D_0	$P2SL_n$	Partial2 display area start line register (00H to AFH)
★ R30	D_7 to D_0	$P1AW_n$	Partial1 display area line count register (00H to AFH) When this register is 0, the values of the partial 2 display area start line register (R29) and the partial 2 display area line count register (R31) are not valid.
R31	D_7 to D_0	$P2AW_n$	Partial2 display area line count register (00H to AFH)
★ R32	D_6	BGRS	This pin selects whether to use the internal power supply or an external power supply (input from the BRGIN pin) for generation the common center voltage output from the VCOM pin. 0: The internal power-supply is selected as the VCOM power supply 1: Input from the external power-supply BGRIN is selected as the BCOM power supply
	D_5	VCE	Selects the V_O output level of the power supply IC (μPD161660). The V_{CE} pin of this IC and the V_{CE} pin of the power supply IC must be connected. 0: The Vo high-level booster voltage level is V_{DD1} minus 1 level 1: The Vo high-level booster voltage level is the same level as V_{DD1}
	D_4	VCD2	Selects the V_{DD2} output level of the power supply IC (μPD161660). The V_{CD2} pin of this IC and the V_{CD2} pin of the power supply IC must be connected. 0: $V_{DD2} = V_{DC} \times 2$ 1: $V_{DD2} = V_{DC} \times 3$
	D_2	RGONG	Switches the internal regulator of the gate IC (μPD161640) ON/OFF. When OFF is selected, a low level is output from the RGONG pin, and when ON is selected, a high level is output from the RGONG pin. The RGONG pin of this IC and the RGON pin of the gate IC must be connected. 0: Regulators of gate driver (V_B) are off 1: Regulators of gate driver (V_B) are on
	D_1	RGONP	Switches the internal DC/DC converter of the power supply IC (μPD161660) ON/OFF. When OFF is selected, a low level is output from the RGONP pin, and when ON is selected, a high level is output from the RGONP pin. The RGONP pin of this IC and the RGON pin of the power supply IC must be connected. 0: Regulators of power supply IC (V_T, V_S) are off 1: Regulators of power supply IC (V_T, V_S) are on
	D_0	DCON	Switches the internal DC/DC converter of the power supply IC (μPD161660) ON/OFF. When OFF is selected, a low level is output from the DCON pin, and when ON is selected, a high level is output from the DCON pin. The DCON pin of this IC and the DCON pin of the power supply IC must be connected. 0: DC/DC converter is off 1: DC/DC converter is on

(4/4)

	Resistor	Bit	Symbol	Function
★	R34	D_3, D_2	VCD12, VCD11	Performs booster control for the DC/DC converter in the power supply IC (μ PD161660) The data set with this bit is output from the VCD11 pin and the VCD12 pin. The VCD11 pin and VCD12 pin of μ PD161620 must be connected to the VCD11 pin and the VCD12 pin of the power supply IC. VCD12, VCD11 = 0, 0: $V_{DD1} = V_{DC} \times 4$ = 0, 1: $V_{DD1} = V_{DC} \times 5$ = 1, 0: $V_{DD1} = V_{DC} \times 6$ = 1, 1: $V_{DD1} = V_{DC} \times 7$
★	R38	D_0	OC	This bit is used for calibration. The time from calibration start command execution until calibration stop command execution becomes the time for 1 line. 0: Calibration start 1: Calibration stop
★	R42	D_3 to D_0	OP_n	Output port (OP_3 to OP_0) write When after the R42 register is specified in the index register, writing to the R42 register is performed, the values written to the OP_3 to OP_0 pins are output.
★	R43	D_3 to D_0	IP_n	Input port (IP_3 to IP_0) read To read the IP_3 to IP_0 inputs, use the following method. <Read sequence> <1> Specify the R43 register from the index register. <2> Execute dummy write to the R43 register. (Values input to IP_3 to IP_0 are loaded to internal latch.) <3>Execute R43 register read. (Reads the internal latch data.)
	R44	-	-	Test mode (for IC testing only)
	R45	-	-	
	R46	-	-	
	R47	-	-	

8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_S	–0.5 to +6.5	V
Power supply voltage	V_{CC1}	–0.5 to +6.5	V
Power supply voltage	V_{CC2}	–0.5 to V_{CC1} + 0.5	V
★ Power supply voltage for γ-curve correction	V_1 to V_{15}	–0.5 to V_S + 0.5	V
Input voltage	V_I	–0.5 to V_{CC1} + 0.5	V
Input current	I_I	±10	mA
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
★ Power supply voltage	V_S	3.6	4.0/5.0	5.5	V
	V_{CC1}	2.5	2.7	3.6	V
	V_{CC2}	1.8		V_{CC1}	V
★ Input voltage	V_I Note1	0		V_{CC1}	V
	V_I Note2	0		V_{CC2}	V

★ **Notes 1.** Pins of V_{CC1} power-supply system: PSX_0, PSX_1, O_{SEL}, C86, $TEST_{OUT}$, IP_0 to IP_3, OP_0 to OP_3, LPMG, LPMP, GOE_1, GOE_2, GSTB, GCLK, DCON, RGONP, RGONG, V_{CD11}, V_{CD12}, V_{CD2}, V_{CE}, OSC_{SEL}, $TEST_{IN}$

★ **2.** Pins of V_{CC2} power-supply system: /CS1, CS2, /RD(E), /WR(R,/W), RDY, D_0 to D_4, D_5(SO), D_6(SCL), D_7(SI), RS, /RESET, GSB, OSC_{IN}

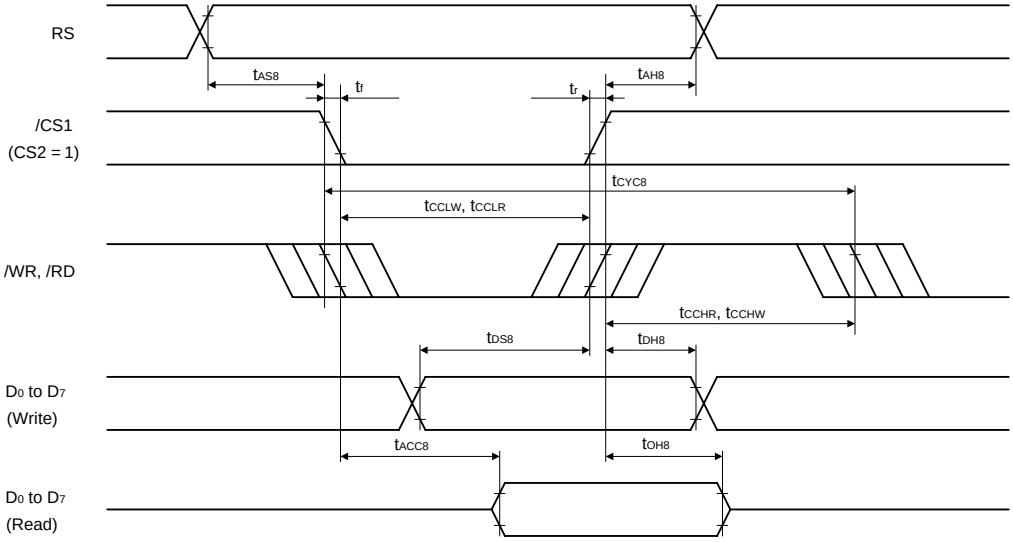
★ **Electrical Specifications (Unless Otherwise Specified, T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 1.8 V to V_{CC1}, V_S = 3.6 to 5.5 V)**

	Parameter	Symbol	Condition	Specification			Unit
				MIN.	TYP.[Note]	MAX.	
	High level input voltage	V_{IH1}	V_{CC1}	0.8 V_{CC1}			V
		V_{IH2}	V_{CC2}	0.8 V_{CC2}			V
	Low level input voltage	V_{IL1}	V_{CC1}			0.2 V_{CC1}	V
		V_{IL2}	V_{CC2}			0.2 V_{CC2}	V
	High level output voltage	V_{OH1}	V_{CC1}, I_{OUT} = –100 μA	0.9 V_{CC1}			V
		V_{OH2}	V_{CC2}, I_{OUT} = –1 mA	0.8 V_{CC2}			V
		V_{OH3}	VCOUT, I_{OUT} = –100 μA	0.9 V_S			V
	Low level output voltage	V_{OL1}	V_{CC1}, I_{OUT} = 100 μA			0.1 V_{CC1}	V
		V_{OL2}	V_{CC2}, I_{OUT} = 1 mA			0.2 V_{CC2}	V
		V_{OL3}	VCOUT, I_{OUT} = 100 μA			0.1 V_S	V
	VCOM output voltage	V_{COMH}	I_{SOURCE} = 40 μA	V_{COM} – 12.5			mV
		V_{COML}	I_{SINK} = –40 μA			V_{COM} + 12.5	mV
★	High level input current	I_{IH1}	D_0 to D_7, $TEST_{IN}$			1	μA
		I_{IH2}	$TEST_{IN}$	20	60	130	μA
	Low level input current	I_{IL1}	Except D_0 to D_7			–1	μA
	High level leakage current	I_{LIH}	D_0 to D_7			10	μA
	Low level leakage current	I_{LIL}	D_0 to D_7			–10	μA
★	High level driver output current	I_{VOH}	V_X = 3.0 V, V_{OUT} = 4.0 V, V_S = 5.0 V			–100	μA
★	Low level driver output current	I_{VOL}	V_X = 2.0 V, V_{OUT} = 1.0 V, V_S = 5.0 V	150			μA
★	Driver output deviation	ΔV_O				±30	mV
★	Internal reference voltage variation for VCOM output	ΔV_{COM}		–6	0	6	V
★	Current consumption	I_{CC1}	V_{CC1} (when non-access CPU)		90	135	μA
		I_{CC2}	V_{CC2} (when non-access CPU)			1	μA
		I_S	4096-color mode		800	1200	μA
			8-color mode		100	150	μA
			Stand-by mode			5	μA

Note TYP. values are reference values when T_A = 25°C

★ **AC Characteristics (Unless Otherwise Specified, T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 1.8 V to V_{CC1}, V_S = 3.6 to 5.5 V)**

(a) i80 series CPU interface



When V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 2.5 to 3.6 V, $V_{CC1} \geq V_{CC2}$

	Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
	Address hold time	t_{AH8}	RS	0			ns
	Address setup time	t_{AS8}	RS	0			ns
	System cycle time	t_{CYC8}		250			ns
★	Control low-level pulse width (/WR)	t_{CCLW}	/WR	120			ns
★	Control low-level pulse width (/RD)	t_{CCLR}	/RD	140			ns
	Control high-level pulse width (/WR)	t_{CCHW}	/WR	60			ns
★	Control high-level pulse width (/RD)	t_{CCHR}	/RD	80			ns
★	Data setup time	t_{DS8}	D_0 to D_7	80			ns
★	Data hold time	t_{DH8}	D_0 to D_7	5			ns
★	/RD access time	t_{ACC8}	D_0 to D_7, C_L = 100 pF			140	ns
★	Output disable time	t_{OH8}	D_0 to D_7, C_L = 100 pF	10		140	ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC2}.

When V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 1.8 to 2.5 V, $V_{CC1} \geq V_{CC2}$

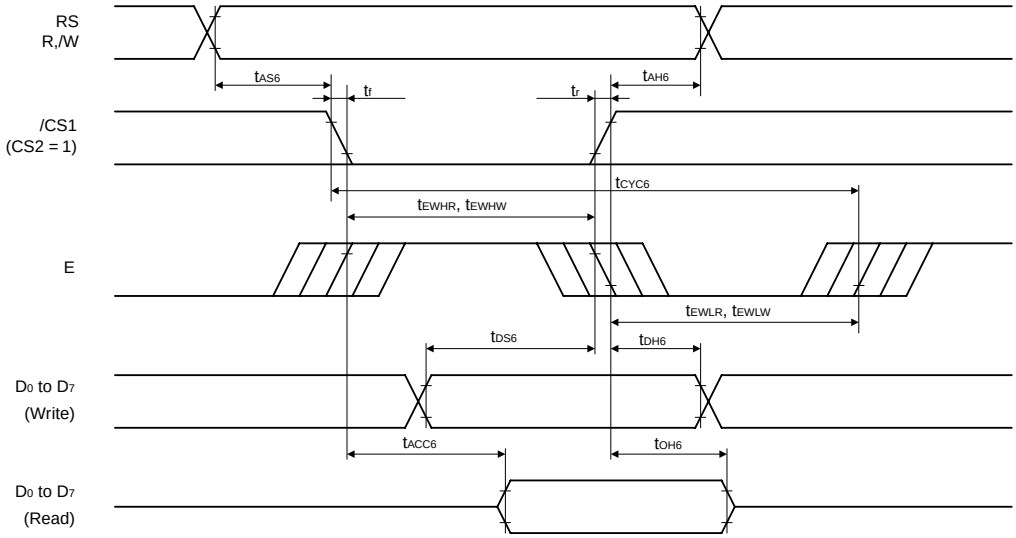
	Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
	Address hold time	t_{AH8}	RS	0			ns
	Address setup time	t_{AS8}	RS	0			ns
	System cycle time	t_{CYC8}		333			ns
★	Control low-level pulse width (/WR)	t_{CCLW}	/WR	120			ns
★	Control low-level pulse width (/RD)	t_{CCLR}	/RD	160			ns
	Control high-level pulse width (/WR)	t_{CCHW}	/WR	100			ns
★	Control high-level pulse width (/RD)	t_{CCHR}	/RD	140			ns
	Data setup time	t_{DS8}	D_0 to D_7	100			ns
★	Data hold time	t_{DH8}	D_0 to D_7	5			ns
★	/RD access time	t_{ACC8}	D_0 to D_7, C_L = 100 pF			180	ns
★	Output disable time	t_{OH8}	D_0 to D_7, C_L = 100 pF	10		180	ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC2}.

(b) M68 series CPU interface



When V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 2.5 to 3.6 V, $V_{CC1} \geq V_{CC2}$

	Parameter		Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
	Address hold time		t_{AH6}	RS	0			ns
	Address setup time		t_{AS6}	RS	0			ns
	System cycle time		t_{CYC6}		250			ns
★	Data setup time		t_{DS6}	D_0 to D_7	80			ns
	Data hold time		t_{DH6}	D_0 to D_7	0			ns
	Access time		t_{ACC6}	D_0 to D_7, C_L = 100 pF			110	ns
	Output disable time		t_{OH6}	D_0 to D_7, C_L = 100 pF	10		100	ns
★	Enable high pulse width	Read	t_{EWHR}	E	140			ns
		Write	t_{EWHW}	E	120			ns
★	Enable low pulse width	Read	t_{EWLR}	E	80			ns
		Write	t_{EWLW}	E	60			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either ($t_r + t_f$) < (t_{CYC6}–t_{EWLR}–t_{EWHR}) or ($t_r + t_f$) < (t_{CYC6}–t_{EWLW}–t_{EWHW}).

2. All timing is rated based on 20 to 80% of V_{CC2}.

When V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 1.8 to 2.5 V, $V_{CC1} \geq V_{CC2}$

	Parameter		Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
	Address hold time		t_{AH6}	RS	0			ns
	Address setup time		t_{AS6}	RS	0			ns
	System cycle time		t_{CYC6}		333			ns
	Data setup time		t_{DS6}	D_0 to D_7	100			ns
	Data hold time		t_{DH6}	D_0 to D_7	0			ns
	Access time		t_{ACC6}	D_0 to D_7, C_L = 100 pF			150	ns
	Output disable time		t_{OH6}	D_0 to D_7, C_L = 100 pF	10		150	ns
★	Enable high pulse width	Read	t_{EWHR}	E	160			ns
		Write	t_{EWHW}	E	120			ns
★	Enable low pulse width	Read	t_{EWLR}	E	140			ns
		Write	t_{EWLW}	E	100			ns

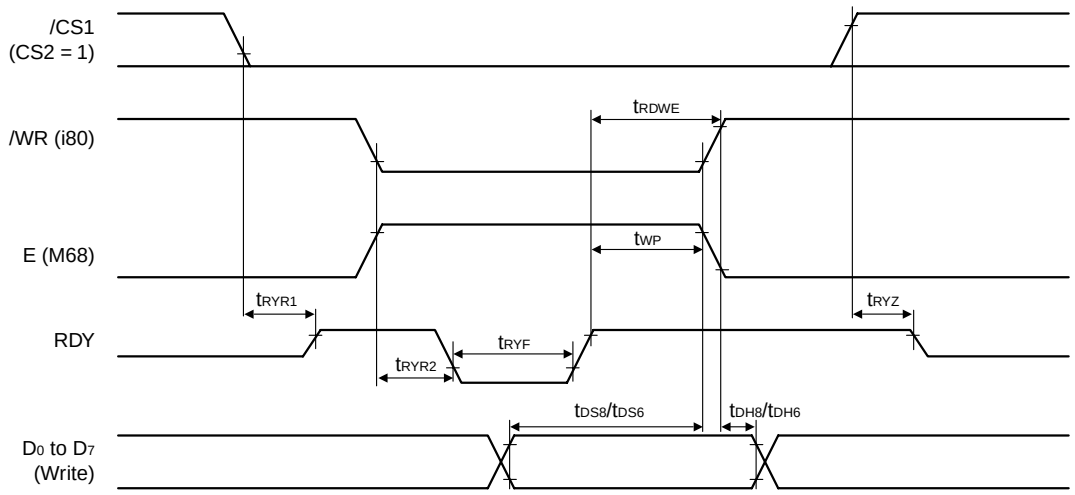
Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either ($t_r + t_f$) < (t_{CYC6}–t_{EWLR}–t_{EWHR}) or ($t_r + t_f$) < (t_{CYC6}–t_{EWLW}–t_{EWHW}).

2. All timing is rated based on 20 to 80% of V_{CC2}.

(c) RDY timing

Write cycle (Display data write)



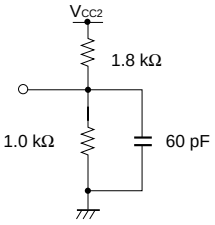
V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 1.8 to 1.9 V, $V_{CC1} \geq V_{CC2}$

	Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
	RDY output delay time (CS)	t_{RYR1}	C_L = 15 pF			110	ns
	RDY output delay time (/WR, E)	t_{RYR2}	C_L = 15 pF			160	ns
★	RDY low level time	t_{RYF}	**Note 1**			850	ns
	Write pulse width	t_{WP}	**Note 1**	0			ns
	RDY to /WR, E time	t_{RDWE}				1000	ns
	RDY output delay time	t_{RYZ}	**Note 2**			90	ns
★	Data setup time	$t_{DS8/6}$		100			ns
	Data hold time	$t_{DH8/6}$		0			ns

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC2}.

Notes 1.



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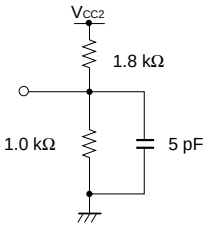
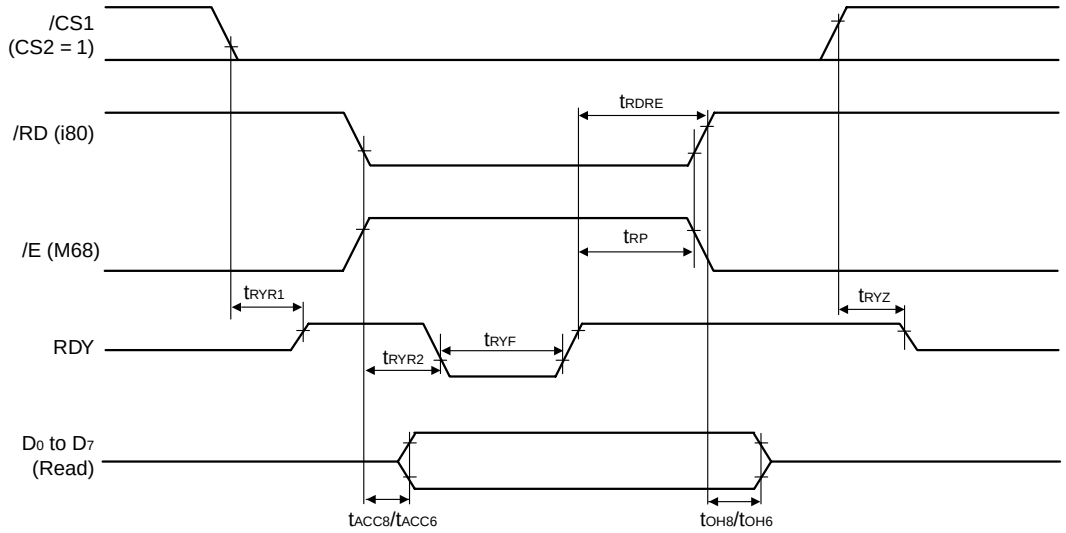


Write cycle (Display data read)



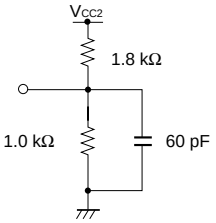
V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 1.8 to 1.9 V, $V_{CC1} \geq V_{CC2}$

	Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
	RDY output delay time (CS)	t_{RYR1}	C_L = 15 pF			110	ns
★	RDY output delay time (/RD, E)	t_{RYR2}	C_L = 15 pF			160	ns
★	RDY low level time	t_{RYF2}	**Note 1**			850	ns
	Read pulse width	t_{RP}	**Note 1**	0			ns
	RDY to /WR, E time	t_{RDRE}				1000	ns
	RDY output delay time	t_{RYZ}	**Note 2**			90	ns
★	Read data access time	$t_{ACC8/6}$	C_L = 100 pF			150	ns
★	Data hold time	$t_{OH8/6}$	C_L = 100 pF	10		150	ns

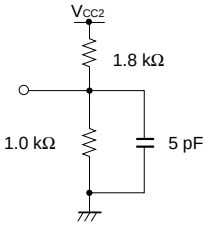
Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC2}.

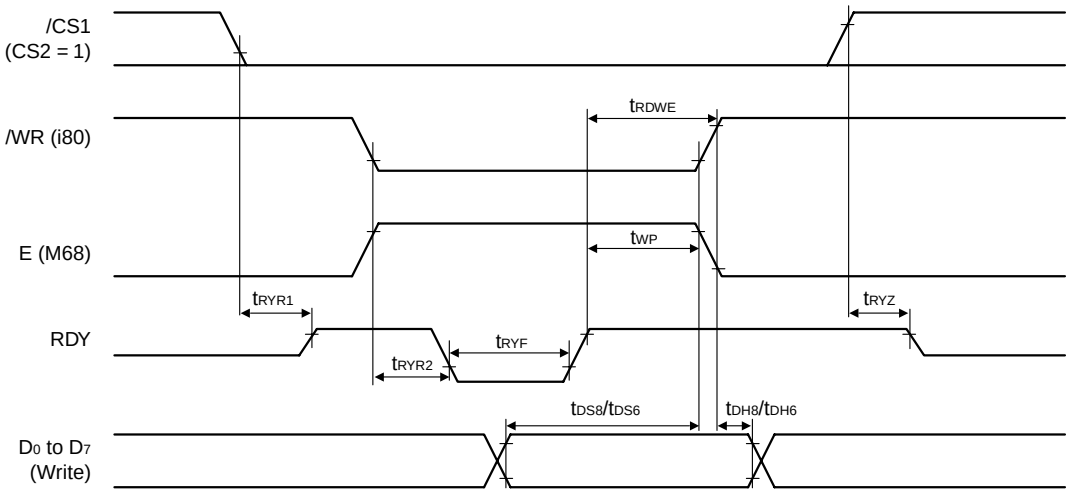
Notes 1.



2.



Write cycle (Display data write)



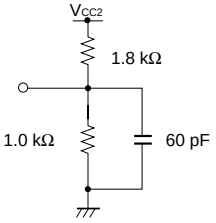
V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 2.5 to 3.6 V, $V_{CC1} \geq V_{CC2}$

	Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
	RDY output delay time (CS)	t_{RYR1}	C_L = 15 pF			80	ns
	RDY output delay time (/WR, E)	t_{RYR2}	C_L = 15 pF			140	ns
★	RDY low level time	t_{RYF2}	**Note 1**			850	ns
	Write pulse width	t_{WP}	**Note 1**	0			ns
	RDY to /WR, E time	t_{RDWE}				1000	ns
	RDY output delay time	t_{RYZ}	**Note 2**			70	ns
★	Data setup time	$t_{DS8/6}$		80			ns
	Data hold time	$t_{DH8/6}$		0			ns

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC2}.

Notes 1.



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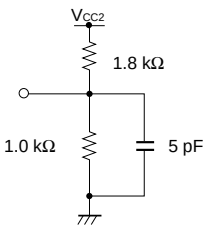
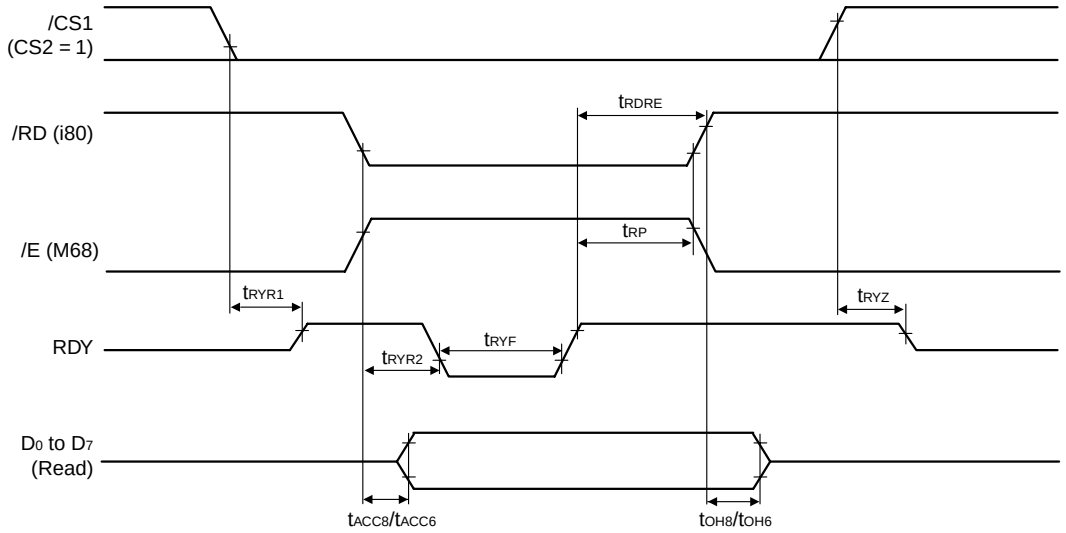


Read cycle (Display data read)



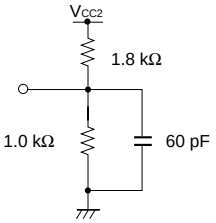
V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 2.5 to 3.6 V, $V_{CC1} \geq V_{CC2}$

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RDY output delay time (CS)	t_{RYR1}	C_L = 15 pF			80	ns
RDY output delay time (/RD, E)	t_{RYR2}	C_L = 15 pF			140	ns
★ RDY low level time	t_{RYF2}	**Note 1**			850	ns
Read pulse width	t_{RP}	**Note 1**	0			ns
RDY to /RD, E	t_{RDRE}				1000	ns
RDY output delay time	t_{RYZ}	**Note 2**			70	ns
Read data access time	$t_{ACC8/6}$	C_L = 100 pF			110	ns
Data hold time	$t_{OH8/6}$	C_L = 100 pF	10		100	ns

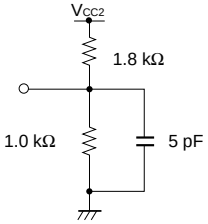
Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC2}.

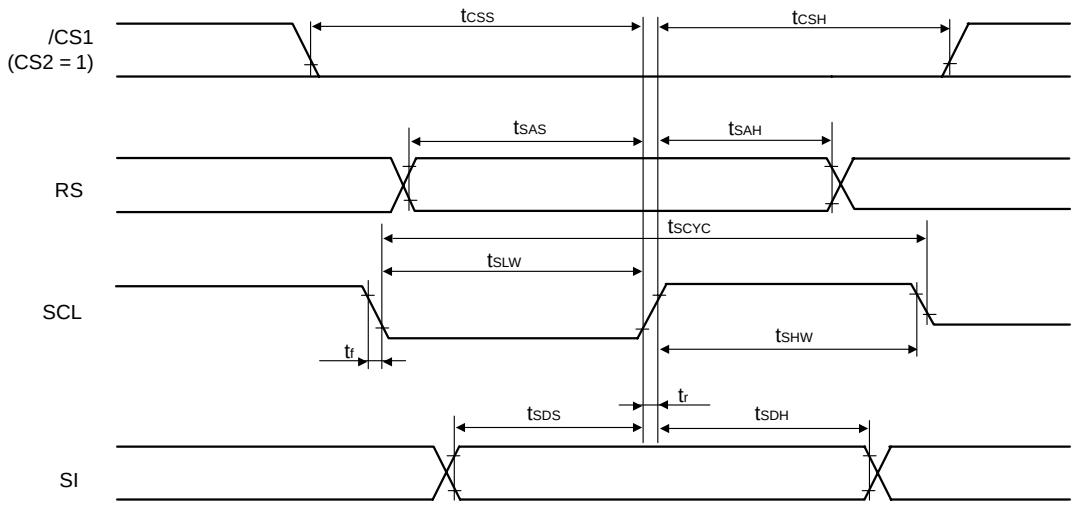
Notes 1.



2.



(d) Serial interface



V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 1.8 to 1.9 V, $V_{CC1} \geq V_{CC2}$

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Serial clock cycle	t_{SCYC}	SCL	250			ns
SCL high-level pulse width	t_{SHW}	SCL	100			ns
SCL low-level pulse width	t_{SLW}	SCL	100			ns
Address hold time	t_{SAH}	RS	150			ns
Address setup time	t_{SAS}	RS	150			ns
Data setup time	t_{SDS}	SI	100			ns
Data hold time	t_{SDH}	SI	100			ns
CS - SCL time	t_{CSS}	/CS1, CS2	150			ns
	t_{CSH}	/CS1, CS2	150			ns

Note TYP. values are reference values when T_A = 25°C.

V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 2.5 to 3.6 V, $V_{CC1} \geq V_{CC2}$

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Serial clock cycle	t_{SCYC}	SCL	150			ns
SCL high-level pulse width	t_{SHW}	SCL	60			ns
SCL low-level pulse width	t_{SLW}	SCL	60			ns
Address hold time	t_{SAH}	RS	90			ns
Address setup time	t_{SAS}	RS	90			ns
Data setup time	t_{SDS}	SI	60			ns
Data hold time	t_{SDH}	SI	60			ns
CS - SCL time	t_{CSS}	/CS1, CS2	90			ns
	t_{CSH}	/CS1, CS2	90			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times of input signal (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC2}.

(e) Common

	Parameter	Symbol	Condition	MIN.	TYP.[Note 1]	MAX.	Unit
	Oscillation frequency	f_{OSC}	Internal oscillator	260	412	680	kHz
★	Calibration setting time (frame frequency)	t_{cal} (f_{FRAME0})	**Note 2**	47 (120)	77.6 (72.8)	93 (60.7)	μs (Hz)
★	Frame frequency	f_{FRAME1}	Uncalibrated	46	73	120	Hz
		f_{FRAME2}	Calibrated [Note 3]	76	80	84	Hz
		f_{FRAME3}	Calibrated [Note 4]	79	80	81	Hz
	Input oscillation frequency	f_{OSCIN}	External oscillator	260		680	kHz
	Reset pulse width at power on	t_{VR}	V_{CC1} or V_{CC2} to /RESET↑	100			ns
	Reset pulse width	t_{RW}		100			ns
	Reset time	t_R	/RESET↑ to interface operation	100			ns

Notes 1. TYP. values are reference values when T_A = 25°C.

2. The relationship between the frame frequency and the calibration setting time is as follows (n: line count).

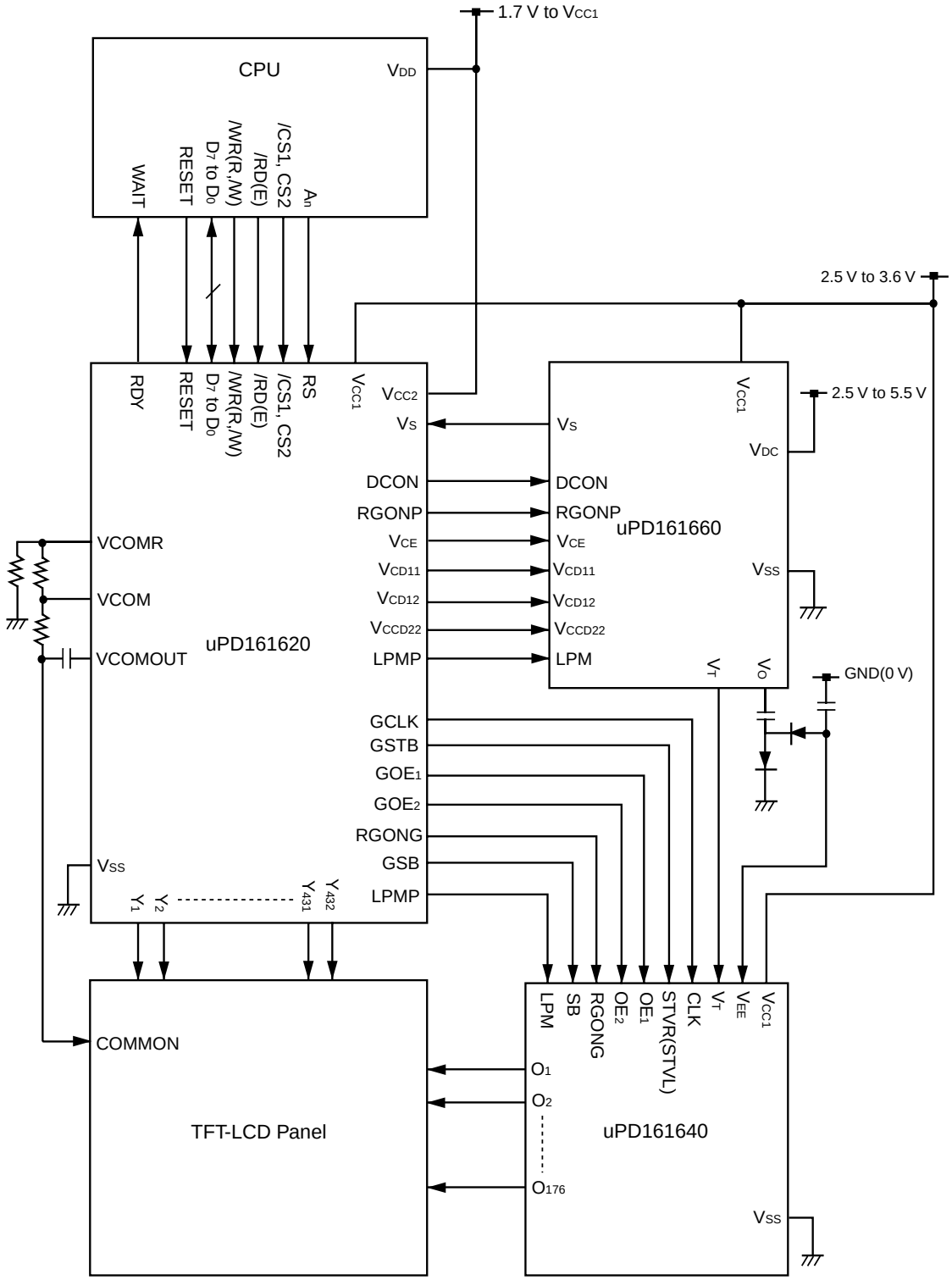
★
$$f_{FRAME0} = \frac{1}{t_{cal} \times 177}$$

3. Measured at T_A = –40 to +85°C, after calibration at frame frequency = 80 Hz, T_A = 25°C exactly.

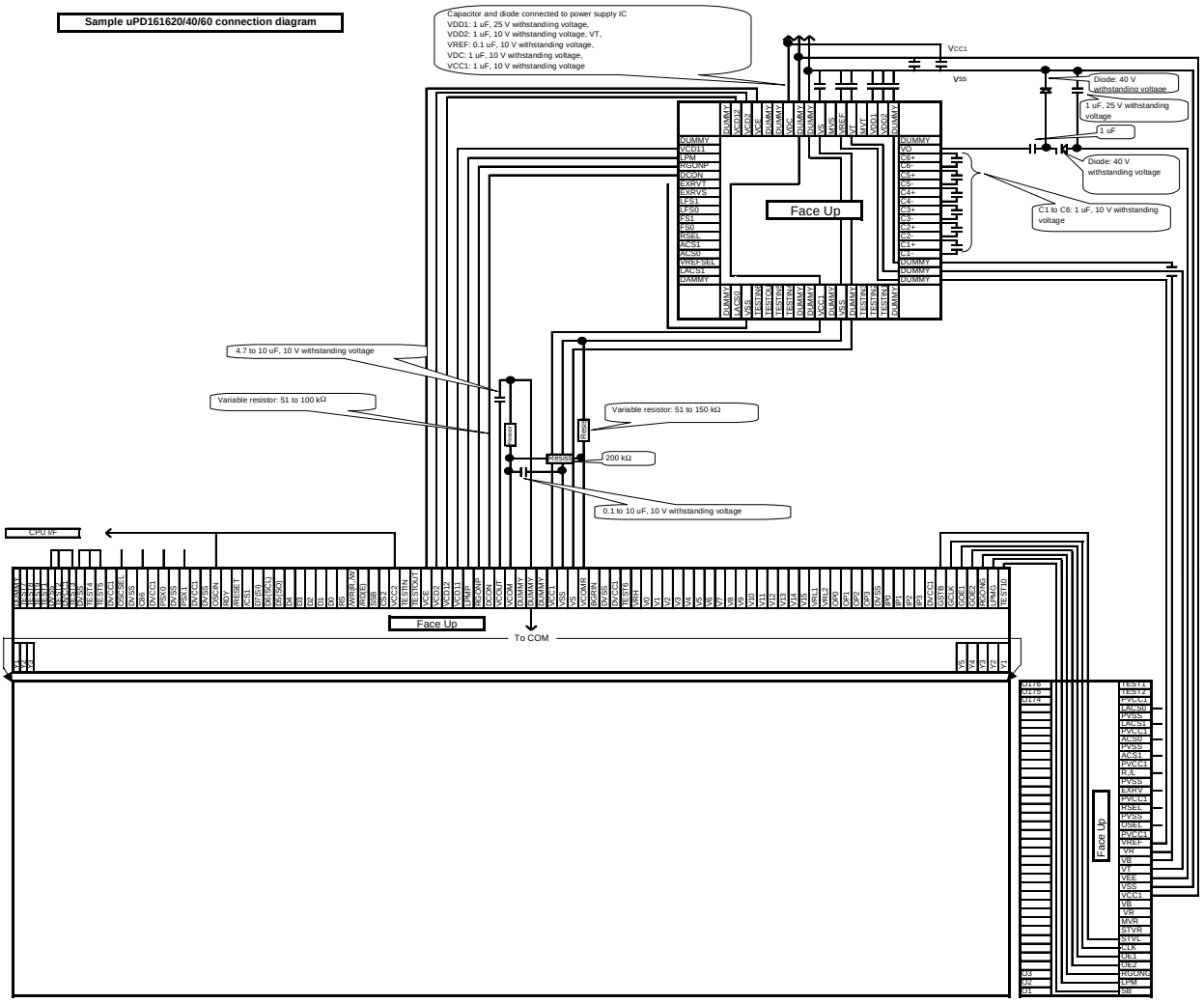
4. Measured at ±5°C, after calibration at frame frequency = 80 Hz exactly.

★ 9. CONNECTION of μPD161620, 161640, and 161660

The connection of the μPD161620, 161640, and 161660 is outlined below.



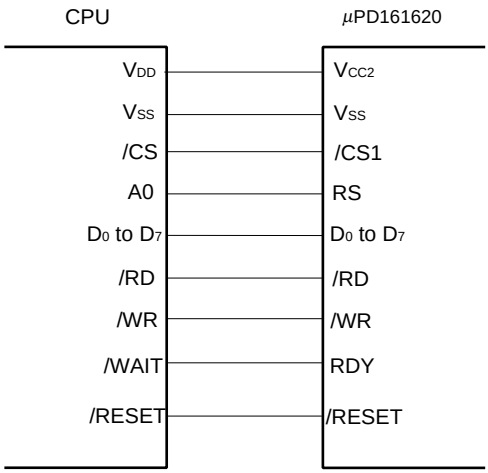
★ The appearance of the μPD161620, 161640, and 161660 when they are connected face-up is as follows.



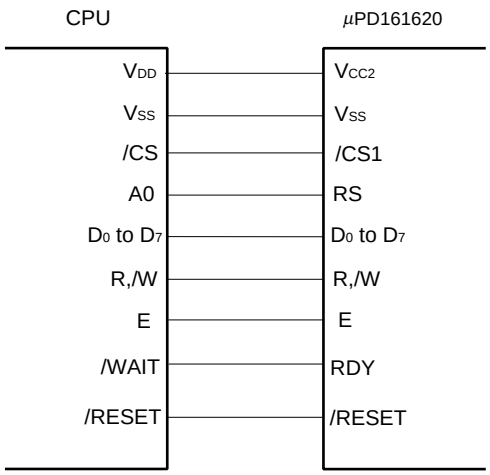
★ 10. EXAMPLE of μPD161620 and CPU CONNECTION

Examples of μPD161620 and CPU connection are shown below. In parallel interface mode, connect the RDY signal to the external WAIT pin of the CPU to execute wait control. In the example below, RS pin control in parallel interface mode is described for the case when the least significant bit of the address bus is being used.

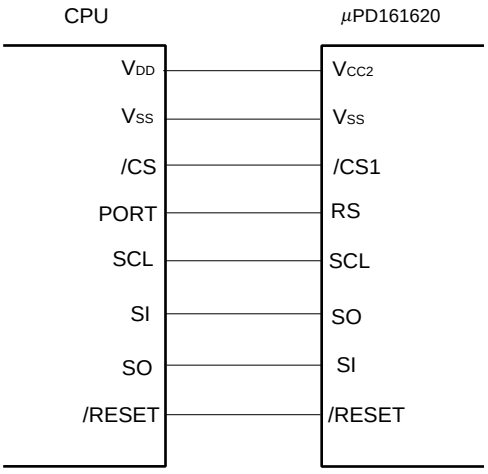
(1) i80 series format



(2) M68 series format



(3) Serial interface



11. REVISION HISTORY

(1/2)

Edition/ Date	Page		Description	
	This edition	Previous edition	Type of revision	Location
1st edition/ S14797EJ1V0PM00 Apr. 2000	–	–	–	–
2nd edition/ S14797EJ2V0PM00 Aug. 2000	Throughout	Throughout	Modification	Title
	Throughout	Throughout	Modification	R22 register name
	Throughout	Throughout	Modification	R24 register name
	p.2	p.2	Modification	1. BLOCK DIAGRAM
	p.7	p.7	Modification	3. PIN FUNCTIONS
	p.10	p.10	Modification	4. PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS
	p.12	p.11	Modification	5.1 title
	p.12	p.11	Modification	5.1.1 Selection of interface type
	p.12	p.11	Addition	5.1.2 Selection of data transfer mode
	p.14	p.13	Addition	Figure 5–3
	p.14	p.13	Modification	Figure 5–4 title
	p.15	–	Addition	5.1.4 Serial interface
	p.16	p.14	Addition	5.2.1 X address circuit
	p.17	p.15	Addition	5.2.3 Y address circuit
	p.18	–	Modification	Figure 5–7
	p.19	p.17	Modification	5.3 Oscillator
	p.19	–	Addition	Figure 5–9
	p.22	–	Addition	5.9 Partial Display Mode
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	p.36	p.19	Modification	6. RESET
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3rd edition/ S14797EJ3V7PM00 Jul. 2001	Throughout	Throughout	Deletion	384 output
	Throughout	Throughout	Addition	V_8 to V_{15}, V_{RH}, V_{RL1}, V_{RL2}
	p.1	p.1	Modification	Driver supply voltage, CPU interface (FEATURES)
	p.2	p.2	Modification	1. BLOCK DIAGRAM
	p.3,4,5,6,7	p.3,4,5,6	Modification	2. PIN CONFIGURATION, Table2–1 Pad Layout
	p.8	p.7	Modification	3. PIN FUNCTIONS
	p.12	p.10,11	Modification	4. PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS
	–	p.11	Deletion	Note 2, 3, 4
	p.13	p.12	Modification	5.1.1 Selection of interface type
	p.13	p.12	Modification	5.1.2 Selection of data transfer mode
	p.14	p.13	Modification	5.1.3 Parallel interface
	p.16	p.15	Modification	5.1.4 Serial interface
	p.16	p.15	Modification	5.1.5 Chip select
	p.17	p.15	Modification	5.1.6 Wait control in parallel interface mode
	p.18	p.17	Modification	5.2.3 Y address circuit
	p.18	p.18	Modification	Figure 5–7. μPD161620 RAM addressing
	p.20	p.20	Modification	5.4 Display Timing Generator
	p.23	p.20	Modification	5.5 Common Adjustment Circuit
	p.24	p.20	Modification	5.6 Square Wave Signal Generation Circuit
	p.25	p.21	Modification	5.8 γ-Curve Correction Power Supply Circuit for Cases of Unbalanced Driving, Figure5–14 γ-Curve correction circuit
	p.26	–	Addition	Table5–7 γ-Curve correction circuit
	p.27	p.22	Modification	5.9 Partial Display Mode, caution
	p.41	–	Addition	5.11 Initialization Setting Sequence Example
	p.45	p.36	Modification	6. RESET
	p.46	p.37	Modification	7.1 Command List, Caution1
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	p.51	p.40	Modification	Power supply voltage for γ-curve correction (Absolute Maximum Ratings)
	p.51	p.40	Modification	Power supply voltage, Input voltage (Recommended Operating Conditions)
	p.51	p.40	Addition	Notes1, 2 (Recommended Operating Conditions)
	p.52	p.41	Modification	Electrical Specifications
	p.53 to 61	p.42 to 50	Modification	Each table (AC Characteristics)
	p.62	p.51	Modification	(e) Common
	p.63, 64	–	Addition	9. CONNECTION of μPD161620, 161640, and 161660
	p.65	–	Addition	10. EXAMPLE of μPD161620 and CPU CONNECTION

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.