

TC74HC393AP, TC74HC393AF, TC74HC393AFN

(Note) The JEDEC SOP (FN) is not available in Japan.

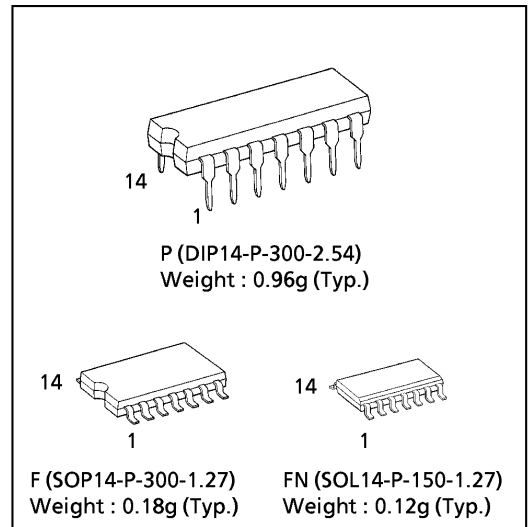
DUAL BINARY COUNTER

The TC74HC393A is a high speed CMOS 4 - BIT BINARY COUNTER fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It contains two independent counter circuits in one package, so that counting or frequency division of eight binary bits can be achieved with one IC.

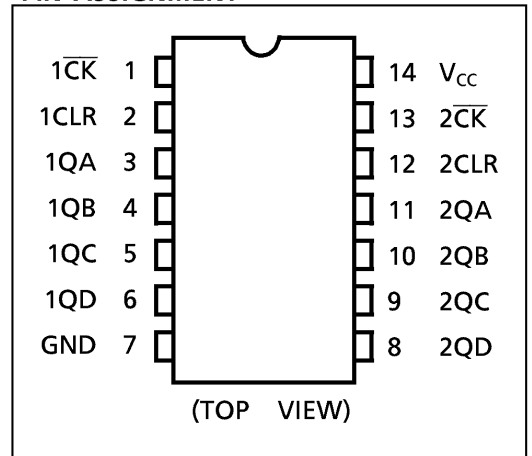
This device changes state on the negative going transition of the \overline{CK} pulse. The counter can be reset to "0" (QA~QD="L") by a high at the CLR input regardless of other inputs. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed..... $f_{MAX} = 72\text{MHz}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Output Drive Capability 10 LSTTL Loads
- Symmetrical Output Impedance · $|I_{OH}| = |I_{OL}| = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays · $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range · $V_{CC} (\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS393



PIN ASSIGNMENT

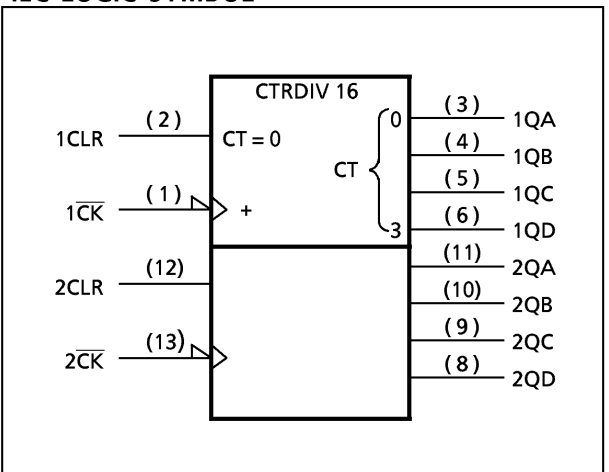


TRUTH TABLE

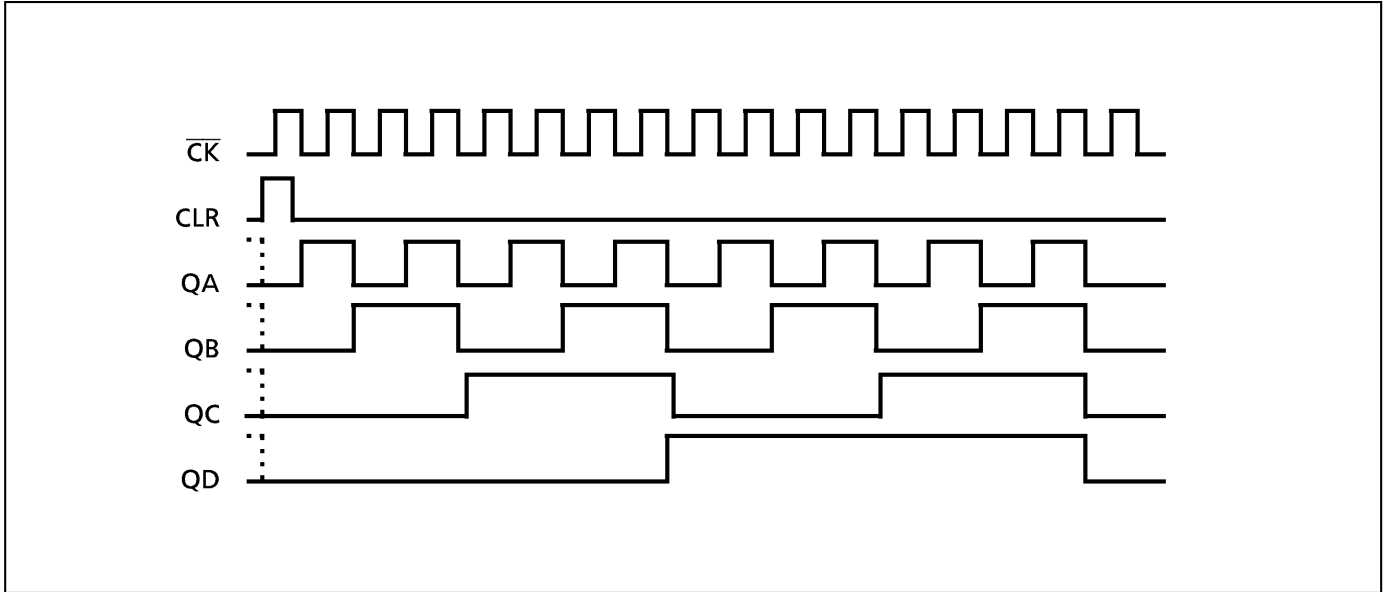
INPUTS		OUTPUTS			
\overline{CK}	CLR	QA	QB	QC	QD
X	H	L	L	L	L
	L	COUNT UP			
	L	NO CHANGE			

X : Don't Care

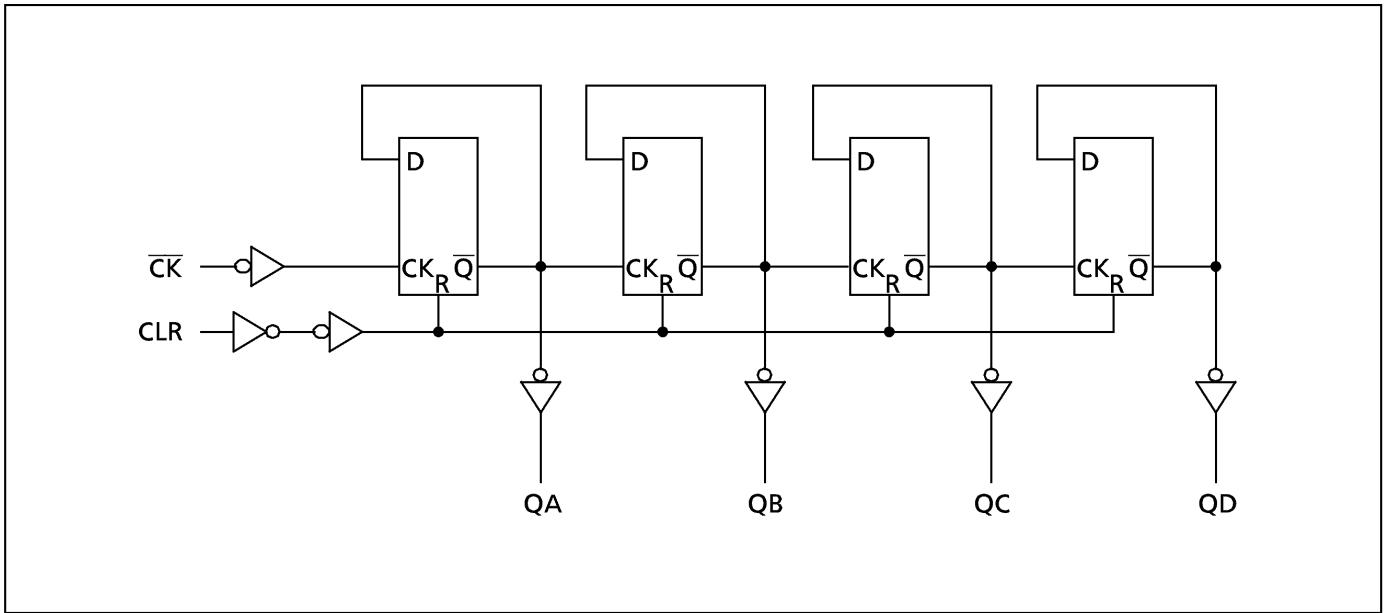
IEC LOGIC SYMBOL



TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000 (V_{CC} = 2.0\text{V})$ $0 \sim 500 (V_{CC} = 4.5\text{V})$ $0 \sim 400 (V_{CC} = 6.0\text{V})$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V_{IH}		2.0	1.50	—	—	1.50	—	V	
			4.5	3.15	—	—	3.15	—		
			6.0	4.20	—	—	4.20	—		
Low - Level Input Voltage	V_{IL}		2.0	—	—	0.50	—	0.50	V	
			4.5	—	—	1.35	—	1.35		
			6.0	—	—	1.80	—	1.80		
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	V	
				4.5	4.4	4.5	—	4.4		—
			6.0	5.9	6.0	—	5.9	—		
			$I_{OH} = -4 \text{ mA}$	4.5	4.18	4.31	—	4.13		—
				6.0	5.68	5.80	—	5.63		—
			$I_{OH} = -5.2 \text{ mA}$	4.5	—	—	—	—		—
6.0	—	—		—	—	—				
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
			6.0	—	0.0	0.1	—	0.1		
			$I_{OL} = 4 \text{ mA}$	4.5	—	0.17	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
			$I_{OL} = 5.2 \text{ mA}$	4.5	—	—	—	—	—	
6.0	—	—		—	—	—				
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	—	—	± 0.1	—	± 1.0	μA	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	—	—	4.0	—	40.0		

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C		Ta = -40-85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (\overline{CK})	$t_{W(H)}$ $t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width (CLR)	$t_{W(H)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Removal Time	t_{rem}		2.0	—	25	30	
			4.5	—	5	6	
			6.0	—	5	5	
Clock Frequency	f		2.0	—	6	5	MHz
			4.5	—	32	27	
			6.0	—	38	32	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, Ta = 25°C, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH}		—	4	8	ns
	t_{THL}					
Propagation Delay Time ($\overline{CK} - QA$)	t_{PLH}		—	12	20	
	t_{PHL}					
Propagation Delay Time ($\overline{CK} - QB$)	t_{PLH}		—	16	31	
	t_{PHL}					
Propagation Delay Time ($\overline{CK} - QC$)	t_{PLH}		—	21	38	
	t_{PHL}					
Propagation Delay Time ($\overline{CK} - QD$)	t_{PLH}		—	25	46	
	t_{PHL}					
Propagation Delay Time (CLR - Qn)	t_{PHL}		—	15	26	
Maximum Clock Frequency	f_{MAX}		35	72	—	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C			Ta = -40-85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	—	25	75	—	95	ns
			4.5	—	7	15	—	19	
			6.0	—	6	13	—	16	
Propagation Delay Time (\overline{CK} —QA)	t_{pLH} t_{pHL}		2.0	—	45	120	—	150	
			4.5	—	15	24	—	30	
			6.0	—	13	20	—	26	
Propagation Delay Time (\overline{CK} —QB)	t_{pLH} t_{pHL}		2.0	—	60	180	—	225	
			4.5	—	20	36	—	45	
			6.0	—	17	31	—	38	
Propagation Delay Time (\overline{CK} —QC)	t_{pLH} t_{pHL}		2.0	—	80	220	—	275	
			4.5	—	25	44	—	55	
			6.0	—	21	37	—	47	
Propagation Delay Time (\overline{CK} —QD)	t_{pLH} t_{pHL}		2.0	—	100	260	—	325	
			4.5	—	30	52	—	65	
			6.0	—	26	44	—	55	
Propagation Delay Time (CLR—Qn)	t_{pHL}		2.0	—	55	150	—	190	
			4.5	—	18	30	—	38	
			6.0	—	15	26	—	33	
Maximum Clock Frequency	f_{MAX}		2.0	6	22	—	5	—	MHZ
			4.5	32	67	—	27	—	
			6.0	38	77	—	32	—	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD} (1)			—	40	—	—	—	

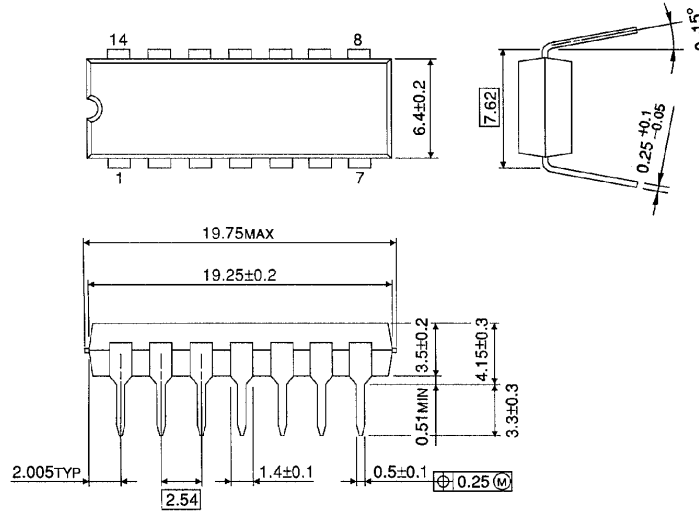
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per counter)}$$

DIP 14PIN PACKAGE DIMENSIONS (DIP14-P-300-2.54)

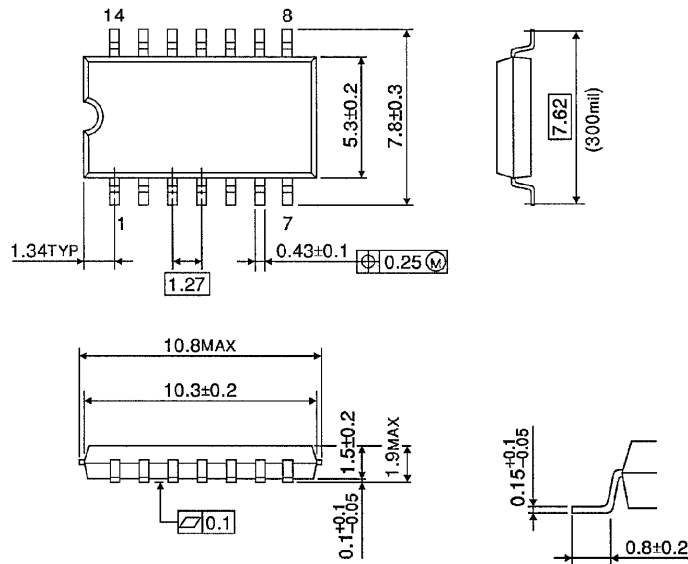
Unit in mm



Weight : 0.96g (Typ.)

SOP 14PIN (200mil BODY) PACKAGE DIMENSIONS (SOP14-P-300-1.27)

Unit in mm

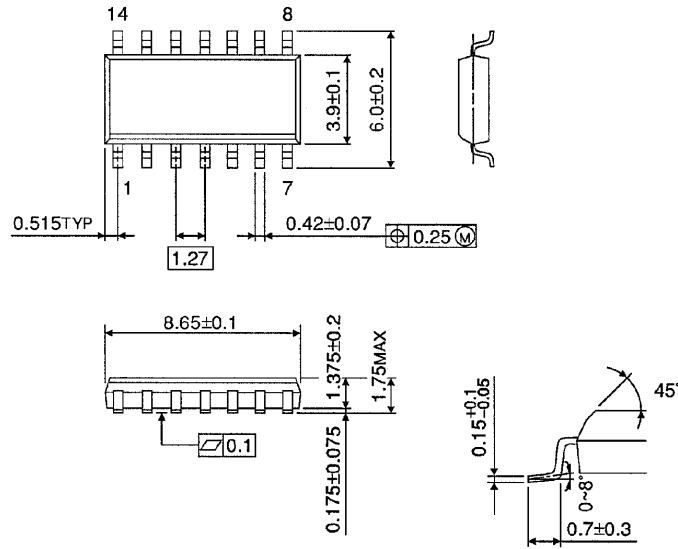


Weight : 0.18g (Typ.)

SOP 14PIN (150mil BODY) PACKAGE DIMENSIONS (SOL14-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

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000707EBA

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