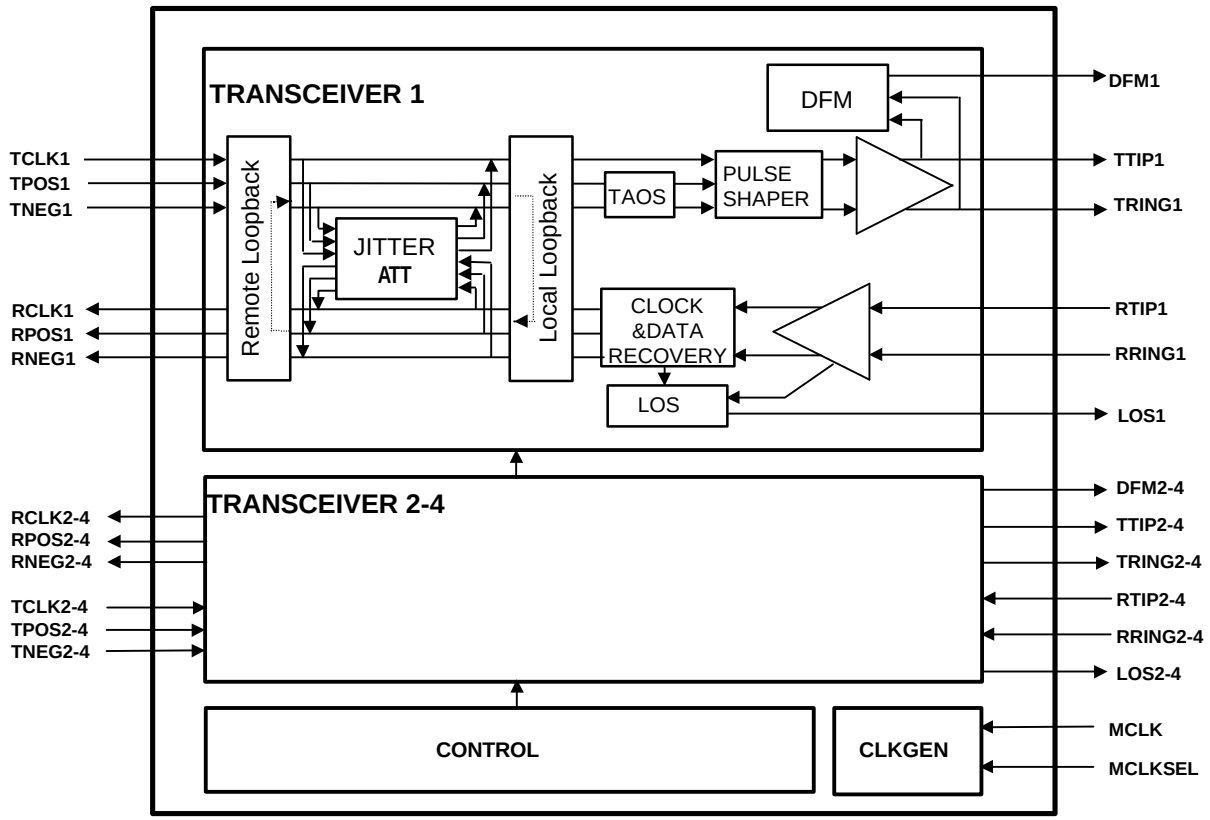
AK2540

Quad T1 Transceiver

FEATURE

- 4ch short haul T1 transceiver with jitter attenuator
- Jitter Tolerance: Compliant with GR-499 Category I,II and TR 62411
- Transmitter Pulse Shape: Compliant with GR-499 and ANSI T1.102 (1993)
- Loss of Signal Detection
- Local/Remote Loopback Mode
- Driver Failure Monitor
- Current limiter in transmit drivers for short circuits protection
- Hardware/Host Control Mode
- Single 3.3V±5% or 5.0V±5% Operation
- Low Power Consumption
- Package: 144LQFP

BLOCK DIAGRAM

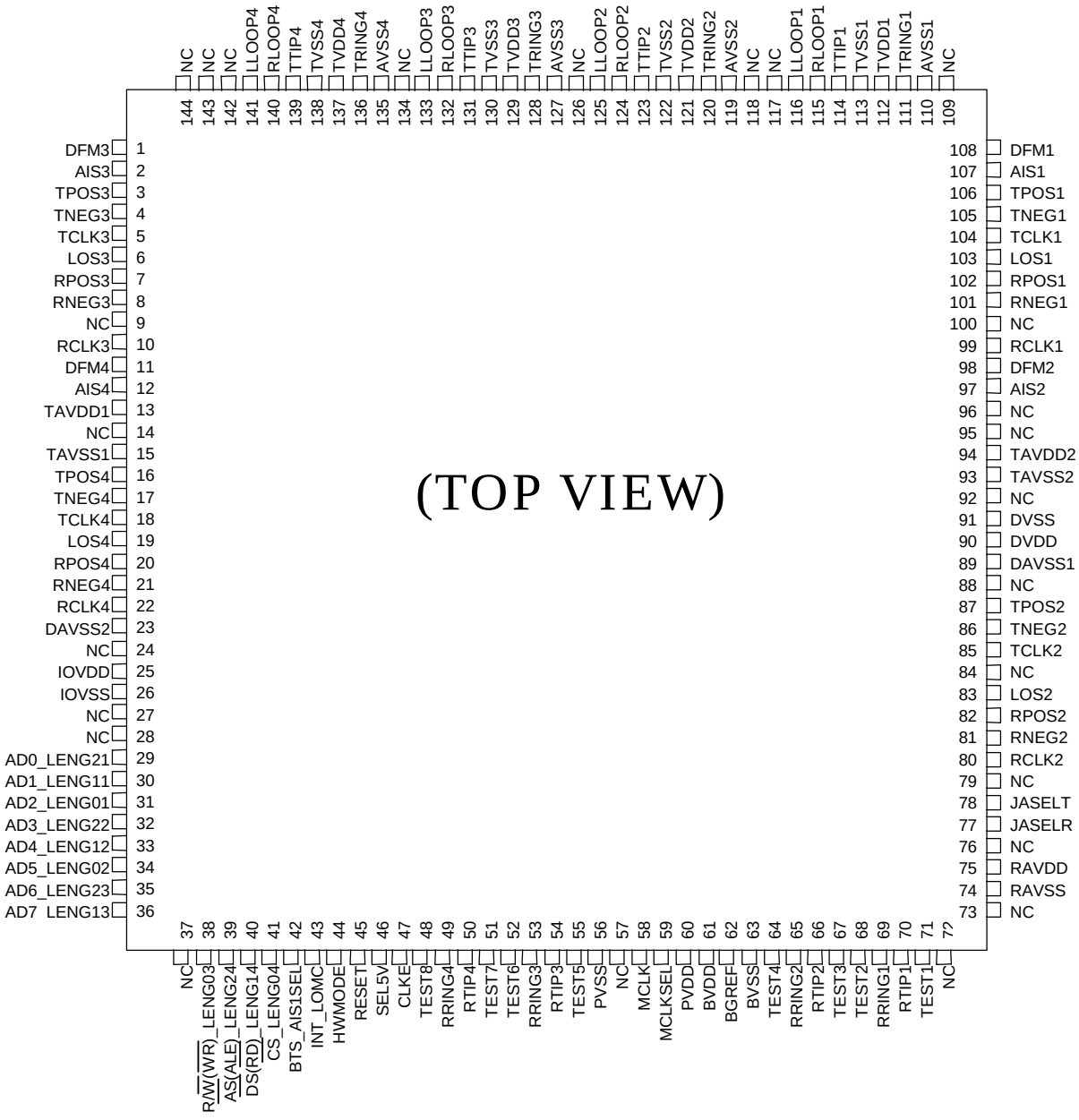


Quad T1 Transceiver Block Diagram

GENERAL DESCRIPTIONS

The AK2540 is the quad short haul T1 transceiver for asynchronous applications, such as M13 MUX, etc. It includes Transmitter, Clock and Data Recovery, Jitter Attenuator, LOS Detector, Driver Failure Monitor, Control Circuits, etc. in one LQFP-144 package. Internally generated transmit pulse provides the appropriate pulse shape for line length ranging from 0 to 655 feet from a DSX-1 cross connect.

PIN ASSIGNMENTS



PIN CONDITION

Pin #	Pin Name	I/O	Pin Type	AC Load	DC Load	Comments
1	DFM3	O	CMOS	≤15pF		
2	AIS3	I	CMOS			Note2)
3	TPOS3	I	CMOS			
4	TNEG3	I	CMOS			
5	TCLK3	I	CMOS			
6	LOS3	O	CMOS	≤15pF		
7	RPOS3	O	CMOS	≤15pF		
8	RNEG3	O	CMOS	≤15pF		
9	NC					
10	RCLK3	O	CMOS	≤15pF		
11	DFM4	O	CMOS	≤15pF		
12	AIS4	I	CMOS			Note2)
13	TAVDD1	I	Power			
14	NC					
15	TAVSS1	I	Power			
16	TPOS4	I	CMOS			
17	TNEG4	I	CMOS			
18	TCLK4	I	CMOS			
19	LOS4	O	CMOS	≤15pF		
20	RPOS4	O	CMOS	≤15pF		
21	RNEG4	O	CMOS	≤15pF		
22	RCLK4	O	CMOS	≤15pF		
23	DAVSS2	I	Power			
24	NC					
25	IOVDD	I	Power			
26	IOVSS	I	Power			
27	NC					
28	NC					
29	AD0_LENG21	I/O	CMOS	≤50pF		
30	AD1_LENG11	I/O	CMOS	≤50pF		
31	AD2_LENG01	I/O	CMOS	≤50pF		
32	AD3_LENG22	I/O	CMOS	≤50pF		
33	AD4_LENG12	I/O	CMOS	≤50pF		
34	AD5_LENG02	I/O	CMOS	≤50pF		
35	AD6_LENG23	I/O	CMOS	≤50pF		
36	AD7_LENG13	I/O	CMOS	≤50pF		

Pin #	Pin Name	I/O	Pin Type	AC Load	DC Load	Comments
37	NC					
38	R/$\overline{W}$($\overline{WR}$)_LENG03	I	CMOS			
39	$\overline{AS}$(ALE)_LENG24	I	CMOS			
40	$\overline{DS}$($\overline{RD}$)_LENG14	I	CMOS			
41	$\overline{CS}$_LENG04	I	CMOS			
42	BTS_AIS1SEL	I	CMOS			
43	INT_LOMC	O	Open drain			PMOS Open drain
44	HWMODE	I	CMOS			
45	RESET	I	CMOS			
46	SEL5V	I	CMOS			
47	CLKE	I	CMOS			
48	TEST8	I	CMOS			Note1)
49	RRING4	I	Analog			
50	RTIP4	I	Analog			
51	TESE7	I	CMOS			Note1)
52	TEST6	I	CMOS			Note1)
53	RRING3	I	Analog			
54	RTIP3	I	Analog			
55	TEST5	I	CMOS			Note1)
56	PVSS	I	Power			
57	NC					
58	MCLK	I	CMOS			
59	MCLKSEL	I	CMOS			
60	PVDD	I	Power			
61	BVDD	I	Power			
62	BGREF	O	Analog		12kΩ	±1% accuracy
63	BVSS	I	Power			
64	TEST4	I	CMOS			Note1)
65	RRING2	I	Analog			
66	RTIP2	I	Analog			
67	TEST3	I	CMOS			Note1)
68	TEST2	I	CMOS			Note1)
69	RRING1	I	Analog			
70	RTIP1	I	Analog			
71	TEST1	I	CMOS			Note1)
72	NC					

Pin #	Pin Name	I/O	Pin Type	AC Load	DC Load	Comments
73	NC					
74	RAVSS	I	Power			
75	RAVDD	I	Power			
76	NC					
77	JASELR	I	CMOS			Note2)
78	JASELT	I	CMOS			Note2)
79	NC					
80	RCLK2	O	CMOS	≤15pF		
81	RNEG2	O	CMOS	≤15pF		
82	RPOS2	O	CMOS	≤15pF		
83	LOS2	I	CMOS	≤15pF		
84	NC					
85	TCLK2	I	CMOS			
86	TNEG2	I	CMOS			
87	TPOS2	I	CMOS			
88	NC					
89	DAVSS1	I	Power			
90	DVDD	I	Power			
91	DVSS	I	Power			
92	NC					
93	TAVSS2	I	Power			
94	TAVDD2	I	Power			
95	NC					
96	NC					
97	AIS2	I	CMOS			Note2)
98	DFM2	O	CMOS	≤15pF		
99	RCLK1	O	CMOS	≤15pF		
100	NC					
101	RNEG1	O	CMOS	≤15pF		
102	RPOS1	O	CMOS	≤15pF		
103	LOS1	O	CMOS	≤15pF		
104	TCLK1	I	CMOS			
105	TNEG1	I	CMOS			
106	TPOS1	I	CMOS			
107	AIS1	I	CMOS			Note2)
108	DFM1	O	CMOS	≤15pF		

Pin #	Pin Name	I/O	Pin Type	AC Load	DC Load	Comments
109	NC					
110	AVSS1	I	Power			
111	TRING1	O	Analog			driver output
112	TVDD1	I	Power			
113	TVSS1	I	Power			
114	TTIP1	O	Analog			driver output
115	RLOOP1	I	CMOS			Note2)
116	LLOOP1	I	CMOS			Note2)
117	NC					
118	NC					
119	AVSS2	I	Power			
120	TRING2	O	Analog			driver output
121	TVDD2	I	Power			
122	TVSS2	I	Power			
123	TTIP2	O	Analog			driver output
124	RLOOP2	I	CMOS			Note2)
125	LLOOP2	I	CMOS			Note2)
126	NC					
127	AVSS3	I	Power			
128	TRING3	O	Analog			driver output
129	TVDD3	I	Power			
130	TVSS3	I	Power			
131	TTIP3	O	Analog			driver output
132	RLOOP3	I	CMOS			Note2)
133	LLOOP3	I	CMOS			Note2)
134	NC					
135	AVSS4	I	Power			
136	TRING4	O	Analog			driver output
137	TVDD4	I	Power			
138	TVSS4	I	Power			
139	TTIP4	O	Analog			driver output
140	RLOOP4	I	CMOS			Note2)
141	LLOOP4	I	CMOS			Note2)
142	NC					
143	NC					
144	NC					

Note1)Should be connected to VSS externally.

Note2)Should be connected to VSS externally in host mode.

Note3)All NC pins are recommended to connected to VSS externally.

PIN DESCRIPTIONS

Pin Name	I/O	Function	Comments
T1 Transceiver			
TTIP1-4 TRING1-4	O O	Transmit Tip/Ring Output pins Bipolar output over transmit transformer	
TPOS1-4 TNEG1-4	I I	Transmit Positive/Negative Data Input pins Input on the falling edge of TCLK	
TCLK1-4	I	Transmit Clock Input pins	
RTIP1-4 RRING1-4	I I	Receive Tip/Ring Input pins Bipolar Input over receive transformer	
RPOS1-4 RNEG1-4	O O	Receive Positive/Negative Data Output pins Output on the rising/falling edge of RCLK (determined by CLKE pin)	
RCLK1-4	O	Receive Clock Output recovered from receive data input pins	
RLOOP1-4	I	Remote Loopback Control input pins	Note1)
LLOOP1-4	I	Local Loopback Control input pins	Note1)
LENG01-04	I	Line Length Control 0 input pins	Note1)
LENG11-14	I	Line Length Control 1 input pins	Note1)
LENG21-24	I	Line Length Control 2 input pins	Note1)
AIS1-4	I	Transmit AIS Enable input pins	Note1)
AIS1SEL	I	Transmit All Ones/Zero Selection input pins when AIS is enabled	Note1)
JASELR	I	Jitter Attenuator Select input pin, placed at Receiver	Note1)
JASELT	I	Jitter Attenuator Select input pin, placed at Transmitter	Note1)
DFM1-4	O	Driver Failure Monitor output pins	
LOS1-4	O	Loss of signal output pins Output “high” when detect loss of signal LOSx output is not masked by MLOSx register.	
TVDD1-4		Positive Power Supply for the Transmit Driver	
TVSS1-4		Negative Power Supply for the Transmit Driver	
AVSS1-4		Analog ground.	
Common Block			
MCLK	I	1.544MHz or 24.704MHz External Reference Clock input pin	
LOMC	O	Loss of master clock output pin. Output “high” when detect loss of master clock LOMC output is not masked by MLOMC register.	Note1)
$\overline{\text{AS}}$(ALE)	I	Address Select(Address Latch Enable) input pin	Note2)
INT	O	Interrupt Output pin(PMOS open drain), Active High, INT output goes “high” when the alarm is reported to any one of LOSx, LOTCx or LOMC registers. This pin can be masked by MLOSx, MLOTCx or MLOMC registers.	Note2)
$\overline{\text{DS}}$($\overline{\text{RD}}$)	I	Data Strobe(Read Enable) input pin	Note2)
R/$\overline{\text{W}}$ ($\overline{\text{WR}}$)	I	Read/Write(Write Enable) input pin	Note2)

Pin Name	I/O	Function	Comments
Common block (Cont.)			
$\overline{CS}$	I	Chip Select input pin	Note2)
BTS	I	Bus Type Select input pin BTS="H" : Motorola Mode BTS="L" : Intel Mode	Note2)
AD0-AD7	I/O	Address/Data Input/Output pins Used for read/write internal registers.	Note2)
MCLKSEL	I	MCLK Select input pin CLKSEL="H":1.544MHz CLKSEL="L":24.704MHz	
HWMODE	I	Hardware/ Host Mode Select input pin HWMODE="H": Hardware Mode HWMODE="L": Host Mode	
SEL5V	I	5.0V /3.3V VDD Select input pin SEL5V="H": 5V operation SEL5V="L": 3.3V operation	
CLKE	I	RCLK clock edge select input pin	
RESET	I	Reset Input pin Active "High" input pulse over 200ns initializes the internal circuit and forces RPOSx/RNEGx output "low" and LOSx output "high".	
TEST1 - 8	I	Factory Use. Should be connected to "VSS" externally.	
TAVDD1,2		Positive Power Supply for the analog circuitry in the transmitters	
TAVSS1,2		Negative Power Supply for the analog circuitry in the transmitters	
RAVDD		Positive Power Supply for the digital circuitry in the transmitters	
RAVSS		Negative Power Supply for the digital circuitry in the transmitters	
DVDD		Positive Power Supply for Digital	
DVSS		Negative Power Supply for Digital	
DAVSS1,2		Ground for Digital	
IOVDD		Positive Power Supply for I/O	
IOVSS		Negative Power Supply for I/O	
BVDD		Positive Power Supply for Reference Circuit	
BVSS		Negative Power Supply for Reference Circuit	
PVDD		Positive Power Supply for PLL	
PVSS		Negative Power Supply for PLL	
BGREF		Bandgap Reference Output pin 12kΩ±1% external register should be connected across this pin and VSS.	

Note1) Hardware Mode

Note2) Host Mode

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Typ	Max	Units	Conditions
DC Supply	VDD	-0.3		6.5	V	
Input Voltage	VIN1	-0.3		VDD+0.3	V	Apply to except for RTIPx, RRINGx
	VIN2	-3.2		VDD+0.3	V	Apply to RTIPx,RRINGx
Input Current	IIN			10	mA	All Pins
Storage Temperature	Tstg	-55		130	°C	

RECOMMENDED OPERATING COMDITIONS

Parameter	Symbol	min	typ	max	Units	Conditions
DC Supply 1	V+1	3.135	3.3	3.465	V	3.3V± 5%
DC Supply 2	V+2	4.75	5.0	5.25	V	5.0V± 5%
Ambient Operating Temperature	Ta	-40	25	+85	°C	

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Parameter	Symbol	min	typ	max	Units	Conditions
Power Consumption(/ch)	PD		106	260	mW	Note1
Power Consumption(/ch)	PD		130	280	mW	Note2
Digital High-Level Output Voltage	VOH	0.9VDD			V	IOH=-500µA
Digital Low-Level Output Voltage	VOL			0.4	V	IOL=500µA
Digital High-Level Input Voltage	VIH	0.7VDD			V	
Digital Low-Level Input Voltage	VIL			0.3VDD	V	
Input Leak Current	Ii			10	µA	
Output Current (VOH=VDD-0.5)	IOH	2.0			mA	INT pin PMOS Open Drain

Note 1: typ: 50% mark, Room temp., VDD 3.3V, line length 399feet, Load 100ohm
max: 100% mark, Temp./VDD in all range, line length 655feet, Load 100ohm
Any other loads (ex. external pull up register, etc.) is not included except lines.

Note 2: typ: 50% mark, Room temp., VDD 5.0V, line length 399feet, Load 100ohm
max: 100% mark, Temp./VDD in all range, line length 655feet, Load 100ohm
Any other loads (ex. external pull up register, etc.) is not included except lines.

RECEIVER

Receiver characteristics are guaranteed under the conditions shown below.
VDD=3.3V±5% or 5.0V±5%, VSS=0V, GND=0V, Ta=-40 - 85°C,
MCLK frequency: 1.544MHz±100ppm, 24.704MHz±100ppm,
AMI input data rate:1.544bps±130ppm(reference input level: $3V_{0p}$±20%)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Sensitivity		-6			dB	Note 1
Loss of Signal Threshold		0.35	0.5	0.7	V_{0p}	Note 2
Jitter Tolerance	GR-499 CategoryI,II, ATT TR 62411					
Consecutive Zeros before Loss of Signal		170	175	180		Note 3
Input Impedance		20			kohm	Note 4

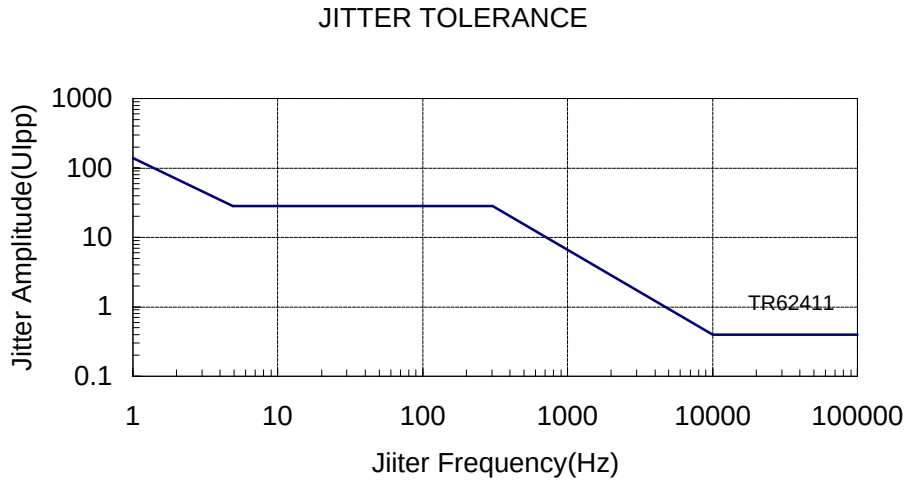
Note 1: Relative value to the reference level. Compare at 772kHz with all mark pattern.

Note 2: Level at the line side of transformer. Loss of signal is logical OR between an analog loss of signal, which monitors input level, and a digital loss of signal, which checks recovered data stream.

Note 3: The device will tolerate consecutive zeros until loss of signal is reported with QRSS (PN20 Modified) pattern.

Note 4: It is not subject to be tested for the production. Guaranteed by design.

JITTER TOLERANCE



TRANSMITTER

Transmitter characteristics are guaranteed under the conditions shown below.
VDD=3.3V±5% or 5.0V±5%, VSS=0V, GND=0V, Ta=-40 - 85°C,
MCLK frequency: 1.544MHz±100ppm, 24.704MHz±100ppm

Parameter		Symbol	Min	Typ	Max	Units	Conditions
Output Pulse Shape							GR-499,Note1
Output Pulse Amplitude			2.5	3.0	3.5	V_{0p}	Note1, Note2
Output Pulse Imbalance					0.4	dB	
Output Jitter	10Hz-8kHz				0.02	UIpp	
	10Hz-40kHz				0.025		
	8kHz-40kHz				0.025		
	Broad Band				0.05		
Power Levels @772kHz			12.6	15	17.9	dBm	Note3
Power Levels @1.544MHz					-29	dB	Note3, Note4
Consecutive Zeros before DPM Alarm				320			

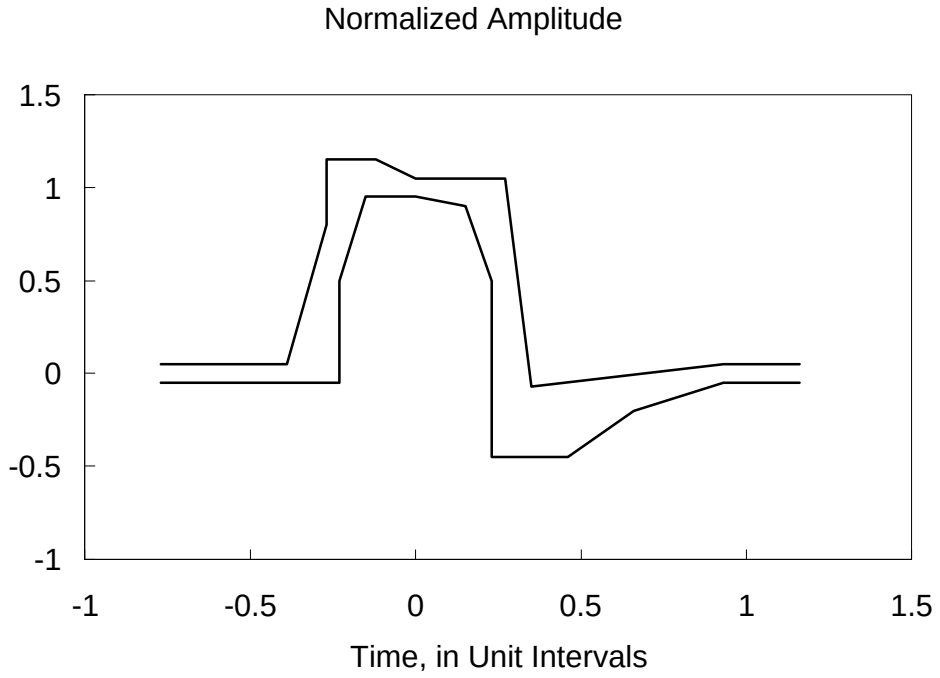
Note 1: Measured at the DSX terminated with 100ohm.

Note 2: Turns Ratio and DCR of transmission transformer are recommended value.

Note 3: Measured in a 2kHz bandwidth about the specified frequency. Transmit all mark pattern.

Note 4: Referenced to the power at 772kHz.

ISOLATED PULSE MASK (GR-499)



JITTER ATTENUATOR

Jitter Attenuator characteristics are guaranteed under the conditions shown below.
VDD=3.3V±5% or 5.0V±5%, VSS=0V, GND=0V, Ta=-40 - 85°C,
MCLK frequency: 1.544MHz±100ppm, 24.704MHz±100ppm

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Jitter attenuator curve corner frequency			6		Hz	
Jitter attenuation @ 10kHz			50		dB	Input Jitter: 1 UIpp
Attenuator input jitter tolerance before FIFO overflow/underflow protection			43		UIpp	
Intrinsic Jitter			0.03	0.06	UIpp	

AC CHARACTERISTICS(Clock/Data)

Parameter		Symbol	Min	Typ	Max	Units	Conditions
Clock Frequency	MCLK1 MCLK2	fci1 fci2	1.543846 24.70153	1.544000 24.70400	1.544154 24.70647	MHz	±100ppm Note 1
Clock Pulse Width	MCLK1	t_{pwhi} t_{pwli}		324		ns	Refer to Fig.4 1.544MHz
	MCLK2			20		ns	Refer to Fig.4 24.704MHz
Clock Pulse Width	TCLK	t_{pwhi} t_{pwli}		324		ns	Refer to Fig.2
Clock Pulse Width	RCLK	t_{pwho} t_{pwlo}		324		ns	Refer to Fig.1 Note 3
Duty Cycle	RCLK TCLK			50		%	Note 2 Note 3
Setup/Hold Time	RCLK RPOS RNEG	t_{su1} t_{h1}	150			ns	Refer to Fig.1
Setup/Hold Time	TCLK TPOS TNEG	t_{su2} t_{h2}	50			ns	Refer to Fig.2
Rise Time	RCLK, TCLK RPOS, TOPS RNEG, TNEG	t_r			50	ns	Refer to Fig.3 Note3
Fall Time	RCLK, TCLK RPOS, TPOS RNEG, TNEG	t_f			50	ns	Refer to Fig.3 Note3

Note 1: All AK2540 specifications are to be within the limit with ±100ppm MCLK.
However, MCLK needs to be within ±32ppm range in order to transmit AIS of ±32 ppm accuracy during the loss of TCLK.

Note 2: Duty Cycle:$(t_{pwho}/(t_{pwho} + t_{pwlo})) \times 100\%$

Note 3: Drive 15pF Load Capacitance

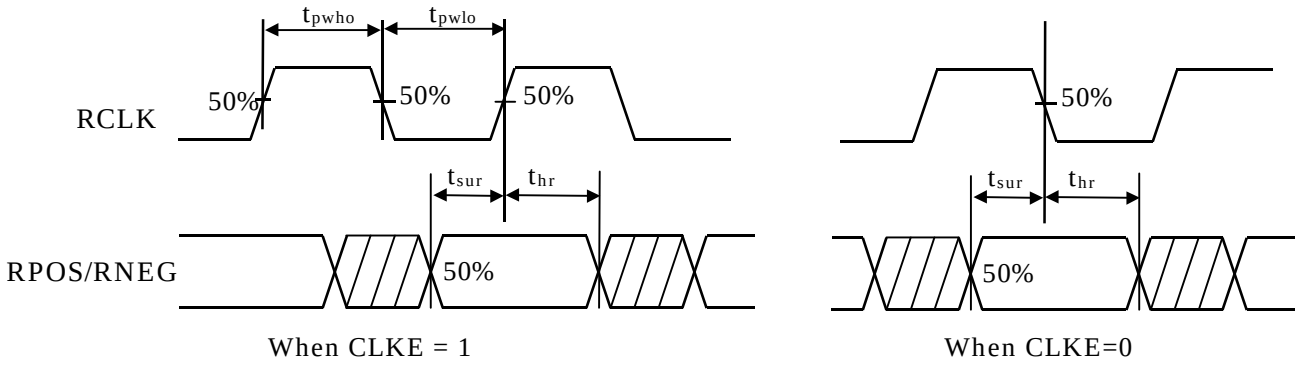


Fig. 1 Receiver Timing

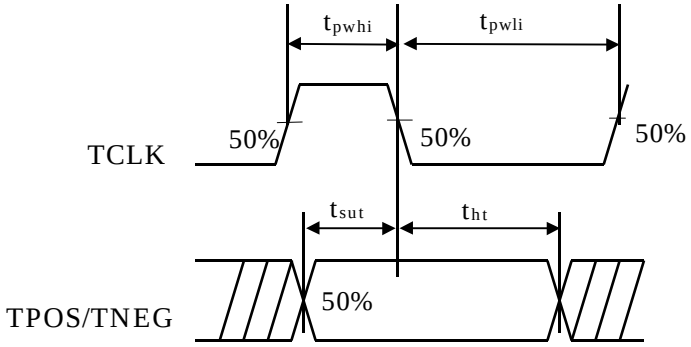


Fig. 2 Transmitter Timing

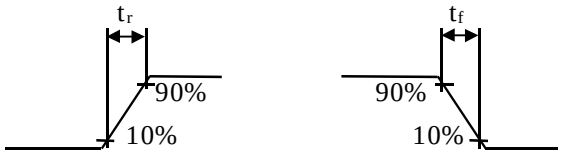


Fig. 3 Rise and Fall Times

(RCLK,RPOS,RNEG,TCLK,TPOS,TNEG,)

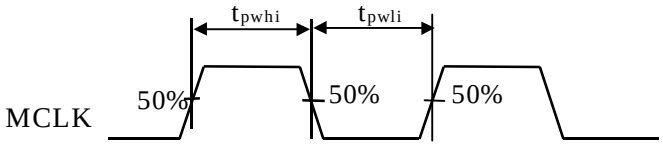


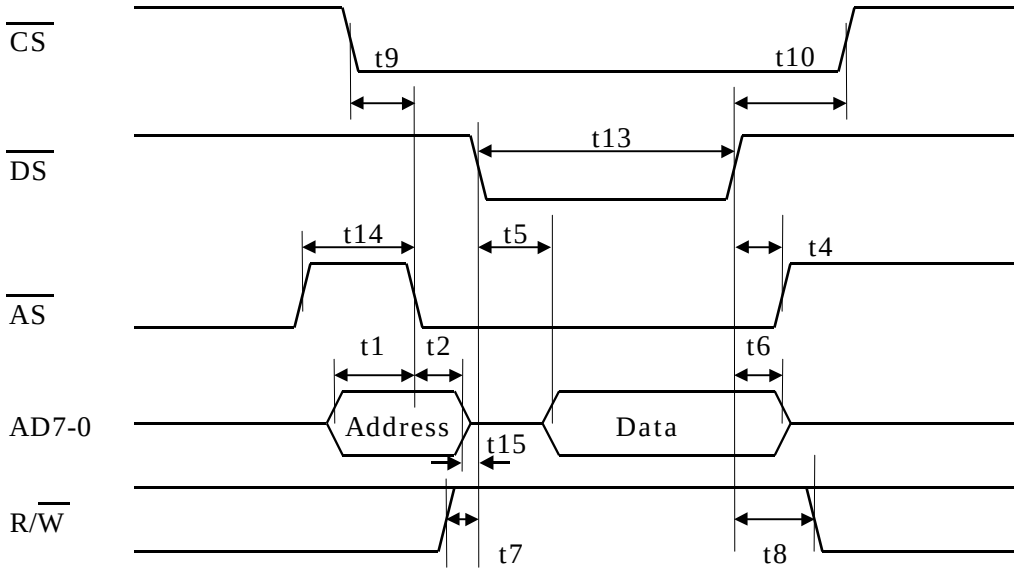
Fig.4 Master Clock Timing

AC CHARACTERISTICS(Parallel Port)

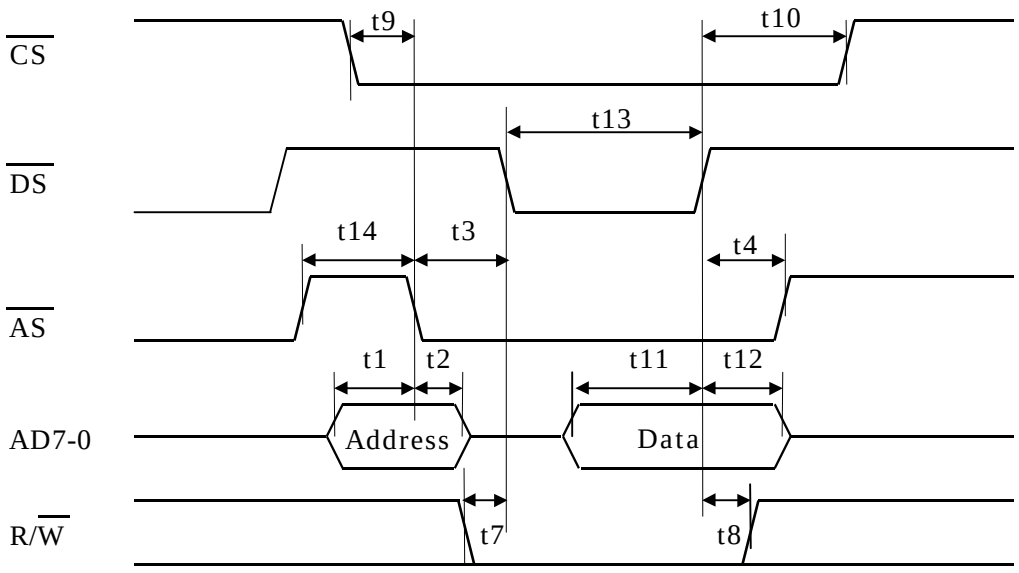
Parameter	Symbol	Min	Typ	Max	Units	Conditions
Motrola Mode						
Address Setup Time	t1	10	-	-	ns	
Address Hold Time	t2	10	-	-	ns	
$\overline{AS}\rightarrow\overline{DS}$ Delay Time	t3	20	-	-	ns	
$\overline{DS}\rightarrow\overline{AS}$ Delay Time	t4	20	-	-	ns	
Read Data Delay Time	t5	-	-	40	ns	
Read Data Hold Time	t6	-	-	20	ns	
R/$\overline{W}$ Setup Time	t7	10	-	-	ns	
R/$\overline{W}$ Hold Time	t8	10	-	-	ns	
$\overline{CS}$ Setup Time	t9	10	-	-	ns	
$\overline{CS}$ Hold Time	t10	15	-	-	ns	
Write Data Setup Time	t11	40	-	-	ns	
Write Data Hold Time	t12	20	-	-	ns	
$\overline{DS}$ Pulse Width	t13	100	-	-	ns	
$\overline{AS}$ Pulse Width	t14	20	-	-	ns	
Address Invalid$\rightarrow\overline{DS}$ Delay Time	t15	10	-	-	ns	
Intel Mode						
Address Setup Time	t21	10	-	-	ns	
Address Hold Time	t22	10	-	-	ns	
ALE$\rightarrow\overline{WR}$ Delay Time	t23	20	-	-	ns	
$\overline{WR}\rightarrow$ALE Delay Time	t24	20	-	-	ns	
$\overline{RD}\rightarrow$ALE Delay Time	t25	20	-	-	ns	
Read Data Delay Time	t26	-	-	40	ns	
Read Data Hold Time	t27	-	-	20	ns	
$\overline{CS}$ Setup Time	t28	10	-	-	ns	
$\overline{CS}$ Hold Time	t29	15	-	-	ns	
Write Data Setup Time	t30	40	-	-	ns	
Write Data Hold Time	t31	20	-	-	ns	
$\overline{RD}$ Pulse Width	t32	100	-	-	ns	
$\overline{WR}$ Pulse Width	t33	100	-	-	ns	
ALE Pulse Width	t34	20	-	-	ns	
Address Invalid$\rightarrow\overline{RD}$ Delay Time	t35	10	-	-	ns	

Notes: CL= 50pF on AD0-AD7. All of the timing is specified at 50%VDD.

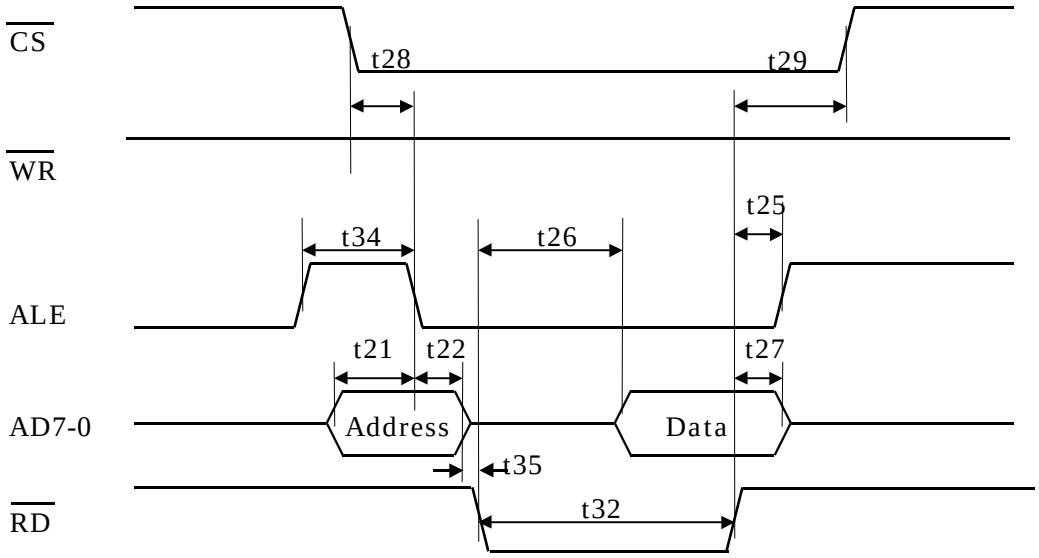
Motorola Mode(READ)



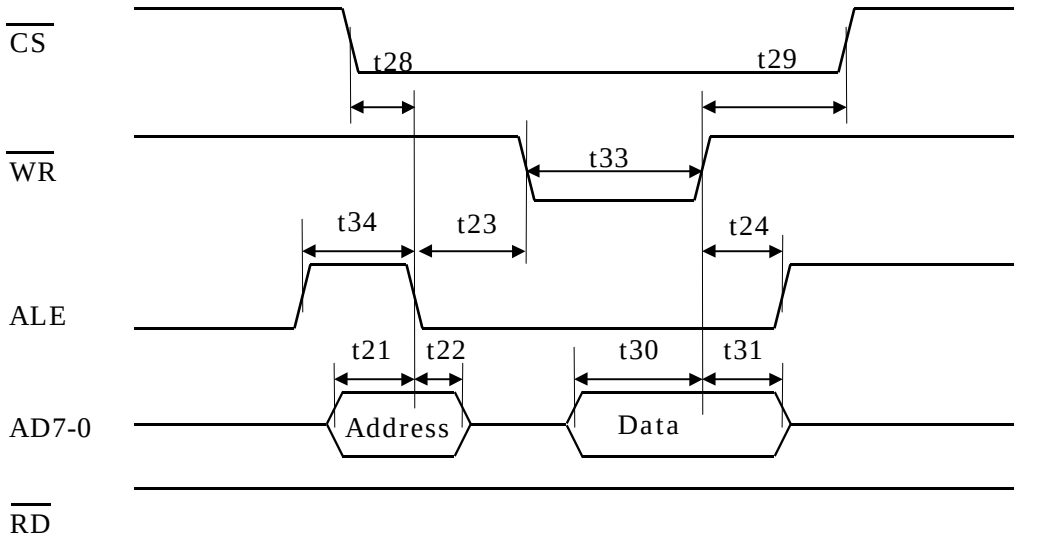
Motorola Mode(WRITE)



Intel Mode(READ)



Intel Mode(WRITE)



THEORY OF OPERATION

Mode of Operation

There are two mode of operation as selected by HWMODE pin. One is the hardware mode and the other is the host mode.

The device is in the hardware mode when HWMODE pin is pulled high and in the host mode when HWMODE pin is pulled low.

Minimum information is available in hardware mode. In Hardware Mode, the device is controlled by the appropriate pins. In Host Mode, the device is controlled by appropriate registers described after through parallel interface.

In Host Mode, all interrupt can be masked by appropriate mask register. However, the status registers and hard flag pins show the current status regardless of the mask register setting.

Pulse Shape Control (Hardware Mode and Host Mode)

In Hardware Mode, the transmit pulse shape in channel x (x = 1,2,3 and 4) is determined by Line Length control pins LENG0x through LENG2x as shown in Table 1.

Table 1. Line Length Control

LENG2x	LENG1x	LENG0x	Line Length
0	0	0	Reserved
0	0	1	0-133feet
0	1	0	133-266feet
0	1	1	266-399feet
1	0	0	399-533feet
1	0	1	533-655feet
1	1	0	Reserved
1	1	1	Reserved

X=1,2,3 and 4

In Host Mode, the transmission pulse shape is determined by appropriate register described in the Register Description section later

Jitter Attenuator (Hardware Mode and Host Mode)

Jitter Attenuator may be placed either transmitter path or receiver path, or bypassed according to JASELR and JASELT both in Hardware Mode and Host Mode as described in table 2. Jitter Attenuators are to be placed at the same place in channel 1 through channel 4.

Table 2. Jitter Attenuator Place Selection

JASELR	JASELT	Location of Jitter Attenuator
0	0	Bypassed
0	1	Transmitter
1	0	Receiver
1	1	Reserved (NA)

AIS (Hardware Mode and Host Mode)

AIS in channel x is selected when AISx is “high”. In AIS mode the TPOS and TNEG inputs are ignored, but the transmitter remains locked to the TCLK input. AIS can be enabled simultaneously with Local Loopback. AIS overdrives Remote Loopback. In this mode, either all ones or all zeros are transmitted according to the AIS1SEL selection. (see table 3)

Table 3. AIS Control

AISx	AIS1SEL	TTIP/TRING
0	0	Normal
0	1	Normal
1	0	All “0”
1	1	All “1”

X=1,2,3 and 4

Loopbacks (Hardware Mode and Host Mode)

Local Loopback (LLOOP) in channel x is selected when LLOOPx is “high” and RLOOPx is “low”. In LLOOP mode, the receiver circuits are inhibited. The transmit clock and data inputs (TCLK and TOPS/TNEG) are looped back and output at RCLK and RPOS/RNEG.
The transmitter circuits are unaffected by LLOOP.

Remote Loopback (RLOOP) in channel x is selected when RLOOPx is “high” and LLOOPx is “low”. However, RLOOP is ignored if AIS is selected. In RLOOP mode, the transmit clock and data inputs (TCLK and TPOS/TNEG) are ignored. The RPOS/RNEG outputs are looped back to the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP and continue to output the data and clock signals received from the line.

Table 4. Loopback mode Selection

RLOOPx	LLOOPx	Function
0	0	Normal
0	1	Local Loop back
1	0	Remote Loop back
1	1	Reserved (NA)

Driver Performance Monitor (Host Mode)

The device incorporates an internal Driver Performance Monitor (DPM) in parallel with TTIP and TRING. DPMx is set “high” when DPM detect 320 bits of consecutive space in channel x. INT pin becomes “high” when DPMx is set “high”, if MDPMx is “low”. DPMx registers represent the current status regardless of the MDPMx status. DPMx returns to “low”, when a mark is detected. However, DPMx is to be kept “high” for 320 TCLK cycle after the first detection of the event.

DPM output is ignored when all “0” AIS is being transmitted

Line Short Protection Circuit

The transmit driver includes a line short protection circuit. When the line short protection circuit detect a line short, transmit signal is fixed to “space”. The line short protection circuit monitor the line short every 160bits cycle. (This alarm is not outputted. Line short is shown for Driver Failure described below.)

Driver Failure Monitor (Hardware Mode and Host Mode)

Driver Failure Monitor asserts the detection of consecutive space or line short.
When DPMx is set “high” or line short circuit in channel x is detected, DFMx(Driver Failure Monitor) register is set “high” and DFMx pin becomes “high”. INT pin becomes “high” when DFMx is set “high” if MDFMx is “low”. DFMx registers and DFMx pins represent the current status regardless of the MDFMx status.

Loss of signal (Hardware Mode and Host Mode)

The receiver will indicate loss of signal upon receiving 175 consecutive zeros (DLOS) or detecting input level being below the threshold (ALOS).
LOSx returns to “low” when the received signal returns to 12.5% ones density and not including 100 consecutive zeros. (GR-820)

When Loss of Signal is detected in channel x, LOSx register is set “high” and LOSx pin becomes “high”. When LOSx is set “high”, interrupt will be issued on INT pin if MLOSx is “low”. LOSx pin becomes high regardless of MLOSx status. MLOSx is active-high and masks LOSx interrupt. LOSx registers and LOSx pins represent the current status of received signal regardless of the MLOSx status.

There are also ALOSx registers and the current status of each channel is available.

Loss of TCLK (Host Mode Only)

Loss of TCLKx is reported by setting LOTCx “high”. When LOTCx is set “high”, INT output becomes “high” if MLOTCx is “low”. MLOTCx is active-high and masks LOTCx interrupt. LOTCx represents the current status of TCLKx and can be read regardless of MLOTCx status.

When Loss of TCLKx is detected, TTIPx/TRINGx will be forced to “0”(except Remote loopback and AIS), and AIS in channel x is sent synchronized with MCLK if AISx is selected.

INT_LOMC output (Hardware Mode and Host Mode)

In Host Mode, INT_LOMC(Interrupt Output) output becomes “high” when the alarm is reported at any one of ALOSx, LOSx, LOTCx, DFMx or DPMx registers. INT_LOMC pin can be masked by MALOSx, MLOSx, MLOTCx, MDFM or MDPM registers.
In Hardware Mode, INT_LOMC pin assert LOMC(Loss of MCLK alarm).

REGISTER DESCRIPTIONS

REGISTER MAP

*A7-A4=”0”

Address				Function							
A3	A2	A1	A0	Bit7 <AD7>	Bit6 <AD6>	Bit5 <AD5>	Bit4 <AD4>	Bit3 <AD3>	Bit2 <AD2>	Bit1 <AD1>	Bit0 <AD0>
Status Register (READ ONLY)											
0	0	0	0	DPM4 (0)	DPM3 (0)	DPM2 (0)	DPM1 (0)	DFM4 (0)	DFM3 (0)	DFM2 (0)	DFM1 (0)
0	0	0	1	LOTC4 (1)	LOTC3 (1)	LOTC2 (1)	LOTC1 (1)	-	-	-	LOMC (1)
0	0	1	0	ALOS4 (1)	ALOS3 (1)	ALOS2 (1)	ALOS1 (1)	LOS4 (1)	LOS3 (1)	LOS2 (1)	LOS1 (1)
Mask Control Register (WRITE/READ)											
0	0	1	1	MDPM4 (1)	MDPM3 (1)	MDPM2 (1)	MDPM1 (1)	MDFM4 (1)	MDFM3 (1)	MDFM2 (1)	MDFM1 (1)
0	1	0	0	MLOTC4 (1)	MLOTC3 (1)	MLOTC2 (1)	MLOTC1 (1)	-	-	-	-
0	1	0	1	MALOS4 (1)	MALOS3 (1)	MALOS2 (1)	MALOS1 (1)	MLOS4 (1)	MLOS3 (1)	MLOS2 (1)	MLOS1 (1)
0	1	1	0	MSK4 (1)	MSK3 (1)	MSK2 (1)	MSK1 (1)	-	-	-	MLOMC (1)
Channel Control Register (WRITE/READ)											
0	1	1	1	LENG21 (0)	LENG11 (0)	LENG01 (1)	RLOOP1 (0)	LLOOP1 (0)	AIS1 (0)	-	PD1 (1)
1	0	0	0	LENG22 (0)	LENG12 (0)	LENG02 (1)	RLOOP2 (0)	LLOOP2 (0)	AIS2 (0)	-	PD2 (1)
1	0	0	1	LENG23 (0)	LENG13 (0)	LENG03 (1)	RLOOP3 (0)	LLOOP3 (0)	AIS3 (0)	-	PD3 (1)
1	0	1	0	LENG24 (0)	LENG14 (0)	LENG04 (1)	RLOOP4 (0)	LLOOP4 (0)	AIS4 (0)	-	PD4 (1)
Global Control Register (WRITE/READ)											
1	0	1	1	JASELR (0)	JASELT (0)	POL (1)	RDEN (0)	AIS1SEL (1)	-	-	-

* The other addresses are reserved.

* Initial value is in ( ).

* “<>” shows I/O pin name. Address A0-A3 should be input via AD0-AD3 pins.

STATUS REGISTER

Symbol	Description
LOSx (x=1 to 4)	Loss of signal alarm for channel x. Read only register. When the loss of signal is detected, LOSx is set High.
LOTCx (x=1 to 4)	Loss of TCLK alarm for channel x. Read only register. When the loss of TCLKx is detected, LOTCx is set High.
DPMx (x=1 to 4)	Driver Performance Monitor alarm for channel x. Read only register. When 320 bits of consecutive space is detected in channel x, DPMx is set high.
DFMx (x=1 to 4)	Driver Failure Monitor alarm for channel x. Read only register. When DPM or short circuit is detected in channel x , DFMx is set high.
ALOSx (x=1 to 4)	Analog loss of signal alarm for channel x. Read only register. When the analog loss of signal is detected, ALOSx is set High.
LOMC	Loss of MCLK alarm. Read only register. When the loss of MCLK is detected, LOMC is set High.

MASK CONTROL REGISTER

Symbol	Description
MLOSx (x=1 to 4)	Mask loss of signal alarm for channel x (LOSx). MLOSx is active-high and prevents LOSx from setting INT output “high”. LOSx register can be read regardless of the MLOSx status. Initial value is “high”.
MLOTCx (x=1 to 4)	Mask loss of TCLK alarm for channel x (LOTCx). MLOTCx is active high and prevents LOTCx from setting INT output “high”. LOTCx register can be read regardless of the MLOTCx status. Initial value is “high”.
MDPMx (x=1 to 4)	Mask DPM alarm for channel x (DPMx). MDPMx is active high Initial value is “high”.
MDFMx (x=1 to 4)	Mask DFM alarm for channel x (DFMx). MDFMx is active high Initial value is “high”.
MSKx (x=1 to 4)	MSKx is active-high and prevents LOSx, LOTCx, DFMx and DPMx in channel x from setting INT output “high”. Initial value is “high”.
MALOSx (x=1 to 4)	Mask analog loss of signal alarm for channel x (ALOSx). MALOSx is active-high and prevents ALOSx from setting INT output “high”. ALOSx register can be read regardless of the MALOSx status. Initial value is “high”.
MLOMC	Mask loss of MCLK alarm (LOMC). MLOMC is active high and prevents LOMC from setting INT output “high”. LOMC register can be read regardless of the MLOMC status. Initial value is “high”.

CHANNEL CONTROL REGISTER

Symbol	Description
LENGyx	The generated transmit pulse in channel x provides the appropriate pulse shape for line length from a DSX-1 cross connect through the setting of this register as shown below in Table 5.
RLOOPx/ LLOOPx	Loopback mode of channel x is activated through the setting of these registers as shown below in Table 6.
AISx	AISx is active-high to transmit AIS in the corresponding channel.
PDx	PDx is active-high to set the corresponding transceiver in power down mode. TTIPx and TRINGx goes “low”. LOSx goes “high” in power down mode. Initial value is “high”.

GLOBAL CONTROL REGISTER

Symbol	Description
JASELR/JA SELT	Jitter Attenuator is placed by these resisters as shown is Table 7. Initial values are “low”
POL	This register as shown in Table 8 controls TIP/RING output polarity. Initial value is “high”.
RDEN	RDEN is active-high and enabling RCLK, RPOS, and RNEG output upon Loss of signal. RCLK, RPOS and RNEG are forced to “high” or “low” upon Loss of Signal when RDEN is “low”. (Please refer to output control) Initial value is “low”.
AIS1SEL	All mark is transmitted as AIS when AIS1SEL is “high”. All space is transmitted as AIS when AIS1SEL is “low”.

Table 5. Line Length Control

LENG2x	LENG1x	LENG0x	Line Length
0	0	0	Reserved
0	0	1	0-133feet
0	1	0	133-266feet
0	1	1	266-399feet
1	0	0	399-533feet
1	0	1	533-655feet
1	1	0	Reserved
1	1	1	Reserved

Table 6. Loopback mode Selection

RLOOPx	LLOOPx	Function
0	0	Normal (Initial value)
0	1	Local Loop back
1	0	Remote Loop back
1	1	Reserved (NA)

Table 7. Jitter Attenuator Place Selection

JASELR	JASELT	Location of Jitter Attenuator
0	0	Bypassed (Initial value)
0	1	Transmitter
1	0	Receiver
1	1	Reserved (NA)

Table 8. TIPx/RINGx Polarity Control

POL	POSx/NEGx	TIPx/RINGx
1	0	space
	1	mark
0	0	mark
	1	space

OUTPUT CONTROL

* : don't care

LOS: LOSx output and LOSx register

Reset, Loss of MCLK, Power down (Host Mode)

RESET	MCLK	PD	Loopback		POL	RDEN	CLKE	TTIP TRING	RCLK	RPOS RNEG	LOS	DFM
			Local	Remote								
1	*	*	*	*	*	*	*	High-Z(Note1)	0	0	1	0
0	loss	*	*	*	1	*	*	0	0	0	1	0
0	loss	*	*	*	0	*	*	0	0	1	1	0
0	clocked	1	*	*	1	0	*	High-Z(Note1)	0	0	1	0
0	clocked	1	*	*	1	1	0	High-Z(Note1)	0	0	1	0
0	clocked	1	*	*	1	1	1	High-Z(Note1)	1	0	1	0
0	clocked	1	*	*	0	0	*	High-Z(Note1)	0	1	1	0
0	clocked	1	*	*	0	1	0	High-Z(Note1)	0	1	1	0
0	clocked	1	*	*	0	1	1	High-Z(Note1)	1	1	1	0

Reset, Loss of MCLK (Hardware Mode)

RESET	MCLK	Loopback		CLKE	TTIP TRING	RCLK	RPOS RNEG	LOS	DFM
		Local	Remote						
1	*	*	*	*	0	0	0	1	0
0	loss	*	*	*	0	0	0	1	0

In Hardware Mode, POL is fixed to "1" and RDEN is fixed to "0".

Normal Operation(RESET=0, AIS=0, MCLK:clocked, PD=0, LLOOP=RLOOP=0)

POL	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS RNEG	LOS	DFM
1	*	clocked	clocked	TPOS TNEG	RCLK	RTIP RRING	0	active
1	0	clocked	loss	TPOS TNEG	0	0	1	active
1	*	loss	clocked	0	RCLK	RTIP RRING	0	0
1	0	loss	loss	0	0	0	1	0
1	1	clocked	loss	TPOS TNEG	RCLK	RTIP RRING	1	active
1	1	loss	loss	0	RCLK	RTIP RRING	1	0
0	*	clocked	clocked	$\overline{\text{TPOS}}$ $\overline{\text{TNEG}}$	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	0	active
0	0	clocked	loss	$\overline{\text{TPOS}}$ $\overline{\text{TNEG}}$	0	1	1	active
0	*	loss	clocked	0	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	0	0
0	0	loss	loss	0	0	1	1	0
0	1	clocked	loss	$\overline{\text{TPOS}}$ $\overline{\text{TNEG}}$	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	1	active
0	1	loss	loss	0	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	1	0

Normal Operation: Transmit all space
(RESET=0, AIS=1,AIS1SEL=0, MCLK:clocked, PD=0, LLOOP=RLOOP=0)

POL	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS RNEG	LOS	DFM
1	*	clocked	clocked	0	RCLK	RTIP RRING	0	0
1	0	clocked	loss	0	0	0	1	0
1	*	loss	clocked	0	RCLK	RTIP RRING	0	0
1	0	loss	loss	0	0	0	1	0
1	1	clocked	loss	0	RCLK	RTIP RRING	1	0
1	1	loss	loss	0	RCLK	RTIP RRING	1	0
0	*	clocked	clocked	0	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	0	0
0	0	clocked	loss	0	0	1	1	0
0	*	loss	clocked	0	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	0	0
0	0	loss	loss	0	0	1	1	0
0	1	clocked	loss	0	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	1	0
0	1	loss	loss	0	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	1	0

Normal Operation: Transmit all mark
(RESET=0, AIS=1,AIS1SEL=1, MCLK:clocked, PD=0, LLOOP=RLOOP=0)

POL	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS RNEG	LOS	DFM
1	*	clocked	clocked	All Mark	RCLK	RTIP RRING	0	active
1	0	clocked	loss	All Mark	0	0	1	active
1	*	loss	clocked	All Mark (Note2)	RCLK	RTIP RRING	0	active
1	0	loss	loss	All Mark (Note2)	0	0	1	active
1	1	clocked	loss	All Mark	RCLK	RTIP RRING	1	active
1	1	loss	loss	All Mark (Note2)	RCLK	RTIP RRING	1	active
0	*	clocked	clocked	All Mark	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	0	active
0	0	clocked	loss	All Mark	0	1	1	active
0	*	loss	clocked	All Mark (Note2)	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	0	active
0	0	loss	loss	All Mark (Note2)	0	1	1	active
0	1	clocked	loss	All Mark	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	1	active
0	1	loss	loss	All Mark (Note2)	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	1	active

Remote Loopback
(RESET=0, AIS=0, MCLK:clocked, PD=0, LLOOP=0, RLOOP=1)

POL	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS RNEG	LOS	DFM
1	*	*	clocked	RTIP RRING	RCLK	RTIP RRING	0	active
1	0	*	loss	RTIP RRING	0	0	1	active
1	1	*	loss	RTIP RRING	RCLK	RTIP RRING	1	active
0	*	*	clocked	RTIP RRING	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	0	active
0	0	*	loss	RTIP RRING	0	1	1	active
0	1	*	loss	RTIP RRING	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	1	active

Remote Loopback: Transmit all space
(RESET=0, AIS=1, AIS1SEL=0, MCLK:clocked, PD=0, LLOOP=0, RLOOP=1)

POL	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS RNEG	LOS	DFM
1	*	*	clocked	0	RCLK	RTIP RRING	0	0
1	0	*	loss	0	0	0	1	0
1	1	*	loss	0	RCLK	RTIP RRING	1	0
0	*	*	clocked	0	RCLK	$\overline{\text{RTIP}}$ RRING	0	0
0	0	*	loss	0	0	1	1	0
0	1	*	loss	0	RCLK	$\overline{\text{RTIP}}$ RRING	1	0

Remote Loopback: Transmit all mark
(RESET=0, AIS=1, AIS1SEL=1, MCLK:clocked, PD=0, LLOOP=0, RLOOP=1)

POL	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS RNEG	LOS	DFM
1	*	*	clocked	All Mark	RCLK	RTIP RRING	0	active
1	0	*	loss	All Mark	0	0	1	active
1	1	*	loss	All Mark	RCLK	RTIP RRING	1	active
0	*	*	clocked	All Mark	RCLK	$\overline{\text{RTIP}}$ RRING	0	active
0	0	*	loss	All Mark	0	1	1	active
0	1	*	loss	All Mark	RCLK	$\overline{\text{RTIP}}$ RRING	1	active

Local Loopback(RESET=0, AIS=0, MCLK:clocked, PD=0, LLOOP=1, RLOOP=0)

POL	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS RNEG	LOS	DFM
1	*	clocked	clocked	TPOS TNEG	TCLK (Note4)	TPOS TNEG	0	active
1	*	clocked	loss	TPOS TNEG	TCLK (Note4)	TPOS TNEG	1	active
1	*	loss	clocked	0	0/1 (Note3)	0	0	0
1	*	loss	loss	0	0/1 (Note3)	0	1	0
0	*	clocked	clocked	$\overline{\text{TPOS}}$ TNEG	TCLK (Note4)	$\overline{\text{TPOS}}$ TNEG	0	active
0	*	clocked	loss	$\overline{\text{TPOS}}$ TNEG	TCLK (Note4)	$\overline{\text{TPOS}}$ TNEG	1	active
0	*	loss	clocked	0	0/1 (Note3)	0	0	0
0	*	loss	loss	0	0/1 (Note3)	0	1	0

Local Loopback: Transmit all space
(RESET=0, AIS=1, AIS1SEL=0, MCLK:clocked, PD=0, LLOOP=1, RLOOP=0)

POL	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS RNEG	LOS	DFM
1	*	clocked	clocked	0	TCLK (Note4)	TPOS TNEG	0	0
1	*	clocked	loss	0	TCLK (Note4)	TPOS TNEG	1	0
1	*	loss	clocked	0	0/1 (Note3)	0	0	0
1	*	loss	loss	0	0/1 (Note3)	0	1	0
0	*	clocked	clocked	0	TCLK (Note4)	$\overline{\text{TPOS}}$ TNEG	0	0
0	*	clocked	loss	0	TCLK (Note4)	$\overline{\text{TPOS}}$ TNEG	1	0
0	*	loss	clocked	0	0/1 (Note3)	1	0	0
0	*	loss	loss	0	0/1 (Note3)	1	1	0

Local Loopback: Transmit all mark
(RESET=0, AIS=1, AIS1SEL=1, MCLK:clocked, PD=0, LLOOP=1, RLOOP=0)

POL	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS RNEG	LOS	DFM
1	*	clocked	clocked	All Mark	TCLK (Note4)	TPOS TNEG	0	active
1	*	clocked	loss	All Mark	TCLK (Note4)	TPOS TNEG	1	active
1	*	loss	clocked	All Mark (Note2)	0/1 (Note3)	0	0	active
1	*	loss	loss	All Mark (Note2)	0/1 (Note3)	0	1	active
0	*	clocked	clocked	All Mark	TCLK (Note4)	$\overline{\text{TPOS}}$ TNEG	0	active
0	*	clocked	loss	All Mark	TCLK (Note4)	$\overline{\text{TPOS}}$ TNEG	1	active
0	*	loss	clocked	All Mark (Note2)	0/1 (Note3)	1	0	active
0	*	loss	loss	All Mark (Note2)	0/1 (Note3)	1	1	active

Note1) The impedance between TTIP and TRING is 30kohm(typ)

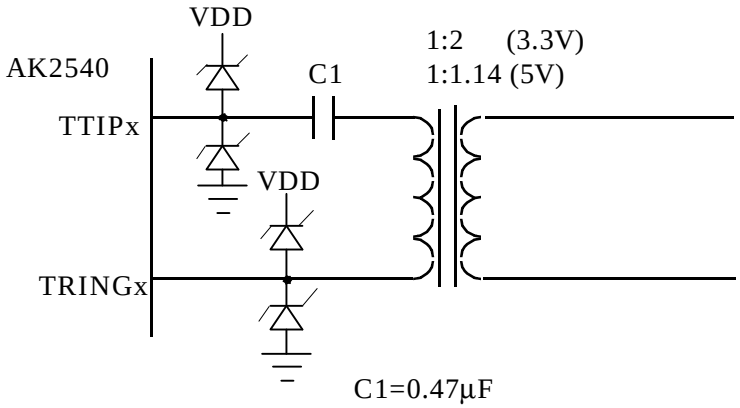
Note2) Transmit signal synchronize with MCLK

Note3) When CLKE is “1”, RCLK is fixed to “1”.

Note4) The phase of the TCLK satisfy receive output timing.

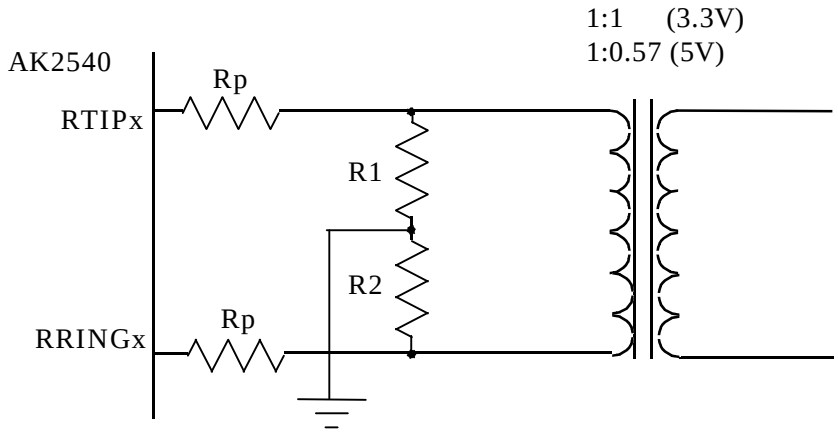
RECOMMENDED EXTERNAL CIRCUITS

Transmit Circuit



C1=0.47μF

Received Circuit



R1=R2= 50ohms (3.3V)
154ohms (5V)
Rp=100ohms(Protection resistance, Example value)

Recommended Transformer Specification

VDD = 3.3V

	Turns Ratio (Typ)	Primary Inductance (Min)	Leakage Inductance (Max)	Interwinding Capacitance (Max)	DCR (Max)	
					pri	sec
Tx	1:2	1.5mH	0.3uF	30pF	0.6ohms	0.6ohms
Rx	1:2(CT)	1.5mH	0.3uF	30pF	0.6ohms	0.6ohms

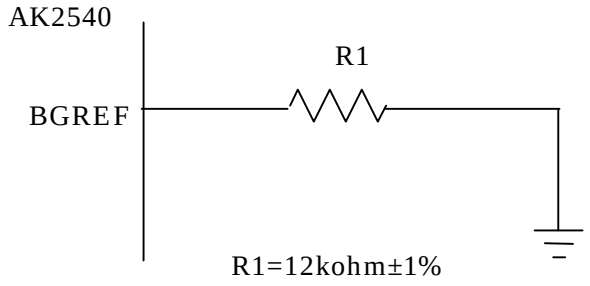
VDD = 5V

	Turns Ratio (Typ)	Primary Inductance (Min)	Leakage Inductance (Max)	Interwinding Capacitance (Max)	DCR (Max)	
					pri	sec
Tx	1:1.14	1.5mH	0.3uF	30pF	0.6ohms	0.6ohms
Rx	1:1.14(CT)	1.5mH	0.3uF	30pF	0.6ohms	0.6ohms

Reference current circuit

To determine input reference current, connect 12kohm±1% resistor.

R1 is recommended to connect to AK2540 as short as possible to avoid noise.



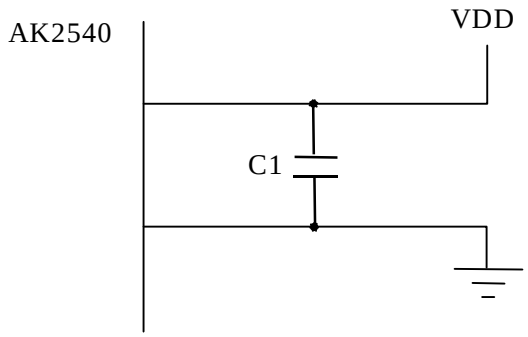
Power Supply

To attenuate the power supply noise, connect capacitors between VDD and VSS respectively.

The value of the capacitance AK2540 need depend on the condition of the power supply line.

Please decide the value of the capacitance after your evaluation.

C1 is recommended to connect to AK2540 as short as possible to avoid noise.



Pin name	C1
RAVDD-RAVSS, BVDD-BVSS, TAVDD1-TAVSS1, TAVDD2-TAVSS2	1uF
TVDD1-TVSS1, TVDD2-TVSS2, TVDD3-TVSS3, TVDD4-TVSS4, IOVDD-IOVSS, DVDD-DVSS, PVDD-PVSS	0.01uF

Recommended Transformers Selection

Power Supply	Turns Ratio	Manufacturer	Part Number	Description
3.3V Operation	1:1.14	TDK	WBTT-0425B	Single, SMT,1.5kV
		Pulse Engineering	T1104	Octal, SMT,1.5kV
5V Operation	1:2	TDK	WBTT-0425	Single, SMT,1.5kV
		Pulse Engineering	T1105	Octal, SMT,1.5kV
		JPC	4101	Single, SMT,1.5kV

PACKAGE

144pin LQFP

Outline Dimensions