DDR110-xxT7RL

DOUBLE DATA RATE TERMINATION NETWORK WITH DISABLE SWITCH

ASD™
IPAD™ Computer

MAIN APPLICATION

DDR (double data rate) Termination Network used on.

- Motherboard
- Workstation
- Server
- Notebooks

DESCRIPTION

The DDR110 provides 10 bits resistor Network to be used for SDR/DDR (double data rate) SDRAM bus Termination.

This device has a series resistors (Rs) to reduce signal reflection noise. This eliminates the need for external terminating resistors.

The DDR Termination Nerwork is enabled with the output Enable pin (OE). When OE is HIGH Inputs are connected to Outputs (A connected to B). When OE is LOW every inputs are in High impedance state (Hi - Z).

The DDR Termination Network is a bidirectional device when the internal switch is ON. When the switch is OFF, the device will block current in both directions.

This device is made using ST IPAD™ (Integrated Passive & Active devices) technology.

FEATURES AND BENEFITS

- 10 bits Termination Network.
- Integrated Termination resistor (Rs)
- Enable input TTL level compatible
- Impedance matching ± 2% (A0-B0 / An-Bn)
- Optimized Low Crosstalk for parallel Termination to Vtt.
- Optimized Low propagation delay

TSSOP24
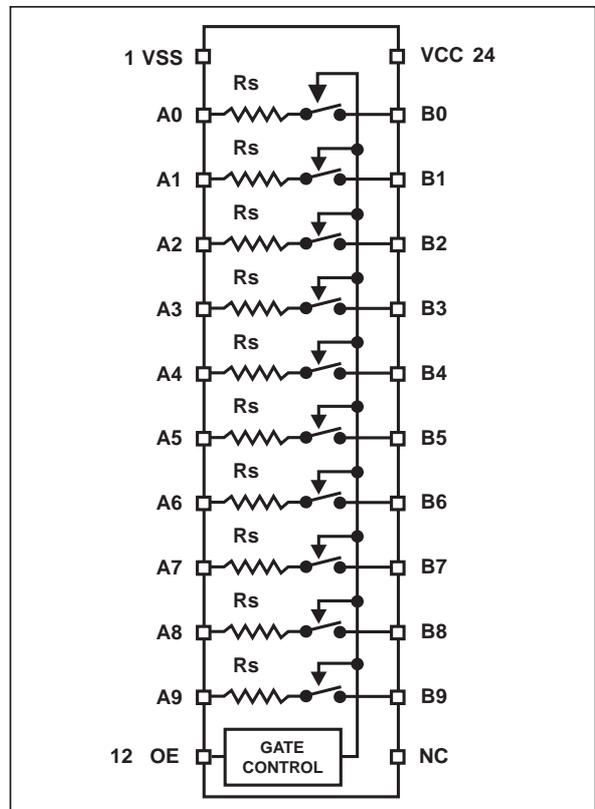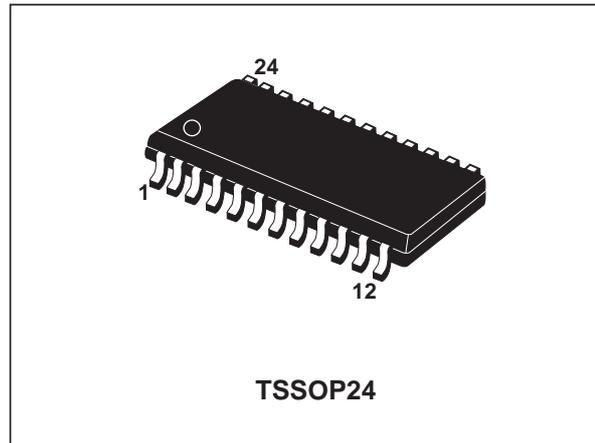
FUNCTION TABLE

OE	B0 - B9	Function
High	A0 - A9	Connect Termination
Low	Hi - Z	Disconnect Termination

ABSOLUTE MAXIMUM RATINGS (Tamb = 25°C)

Symbol	Parameter	Test Conditions	Value Tambient = 25°C			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage range		- 0.5	5	7	V
V_{IN}	Input voltage range DQ0/7, DM0, DQS0		- 0.5		7	V
V_{TT}	Termination voltage		- 0.5		7	V
V_{OE}	Termination Enable Voltage range		- 0.5		7	V
I_{IN}	Continuous input current				30	mA
V_{ESD}	ESD ratings (input / output YOE)	HBM MIL STD 883C			2	kV
T_{STG}	Storage temperature		- 65		150	°C

RECOMMENDED OPERATING CONDITIONS (Tamb = 25°C)

| Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IN}	Input voltage DQ0/7, DM0, DQS0	OE LOW OE HIGH	0 0		+ 3.3 + 2.5	V
V_{IH}	Output Enable (OE) HIGH voltage	Guaranteed logic HIGH level	2	5 [1]		V
V_{IL}	Output Enable (OE) LOW voltage	Guaranteed logic LOW level			0.8	V
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{TT}	Termination voltage			1.25		V

(1) Open collector output with 10k pull-up resistor to 5V is recommended for typical OE signal.

ELECTRICAL CHARACTERISTICS (Tamb = 25°C - Vcc = 5V)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
R_{ON}	Switch ON Resistance	V_{TT} = 1.25V, V_{IN} = 0V, OE = + 5V DDR110-27 DDR110-56	22 45	27 56	32 67	Ω Ω
I_{OFF}	INPUT Leakage current Switch OFF	INPUT = + 3.3V, OE = 0V			1	µA
C_{OFF}	OFF-state capacitance	V_{IN} = 0V, 1MHz, 30mV$_{RMS}$, OE = 0V		6		pF

APPLICATION SCHEMATICS
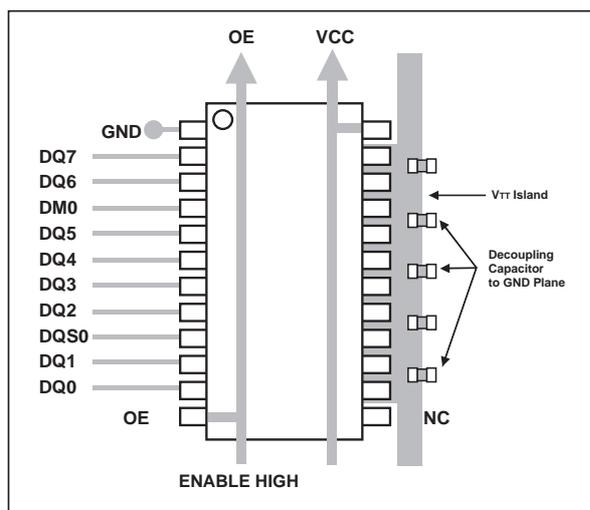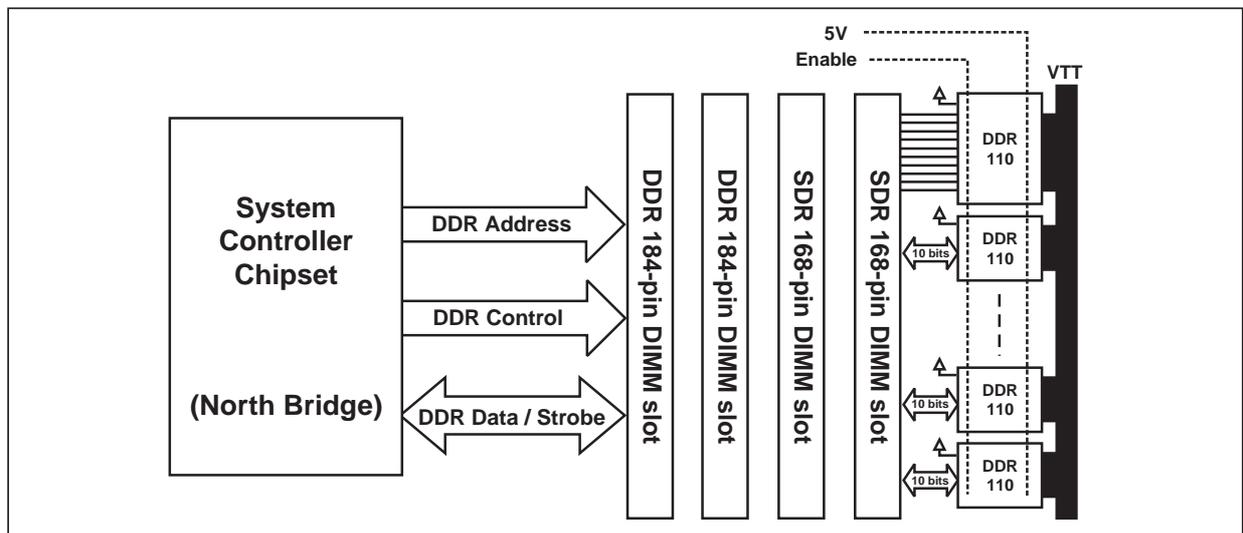
PIN ASSIGNEMENT

Pin #	Assignement for DDR Termination	Pin #	Assignement for DDR Termination
1	V_{ss} = GND	24	V_{cc}
2	A0	23	B0
3	A1	22	B1
4	A2	21	B2
5	A3	20	B3
6	A4	19	B4
7	A5	18	B5
8	A6	17	B6
9	A7	16	B7
10	A8	15	B8
11	A9	14	B9
12	Termination enable HIGH	13	Not Connected

OTHER INFORMATION

DDR1 10 - 27 T7 RL

Double Data Rate Single switch ←

10-BIT Wide ←

Rs value in Ω
27Ω, 56Ω

→ Tape & Reel

→ Package code T7: TSSOP24
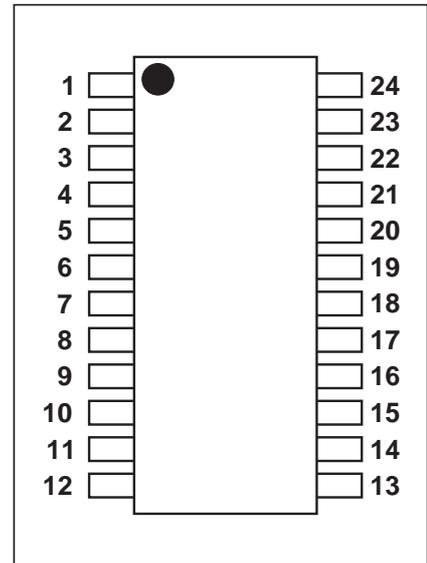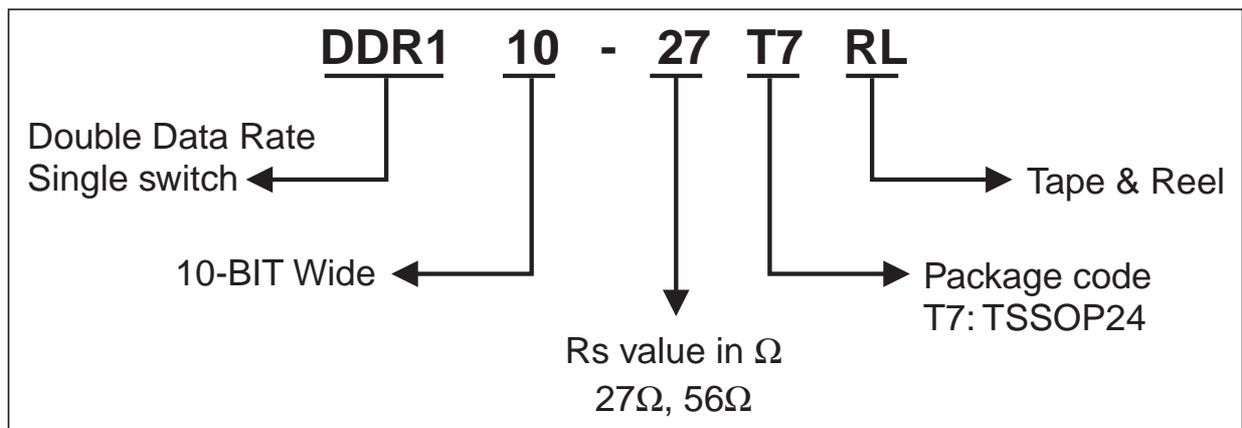
PACKAGE MECHANICAL DATA
TSSOP-24

REF.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.200			0.047
A1	0.050		0.150	0.002		0.006
A2	0.800	1.000	1.050	0.031	0.039	0.041
b	0.190		0.300	0.007		0.012
c	0.090		0.200	0.004		0.008
D	7.700	7.800	7.900	0.303	0.307	0.311
E		6.400			0.252	
E1	4.300	4.400	4.500	0.169	0.173	0.177
e		0.65			0.026	
k	0°		8°	0°		8°
L	0.450	0.600	0.750	0.017	0.024	0.029
L1		1.000			0.039	

FOOTPRINT

0.65mm   0.30mm   6.8mm   4.4mm   8.00mm
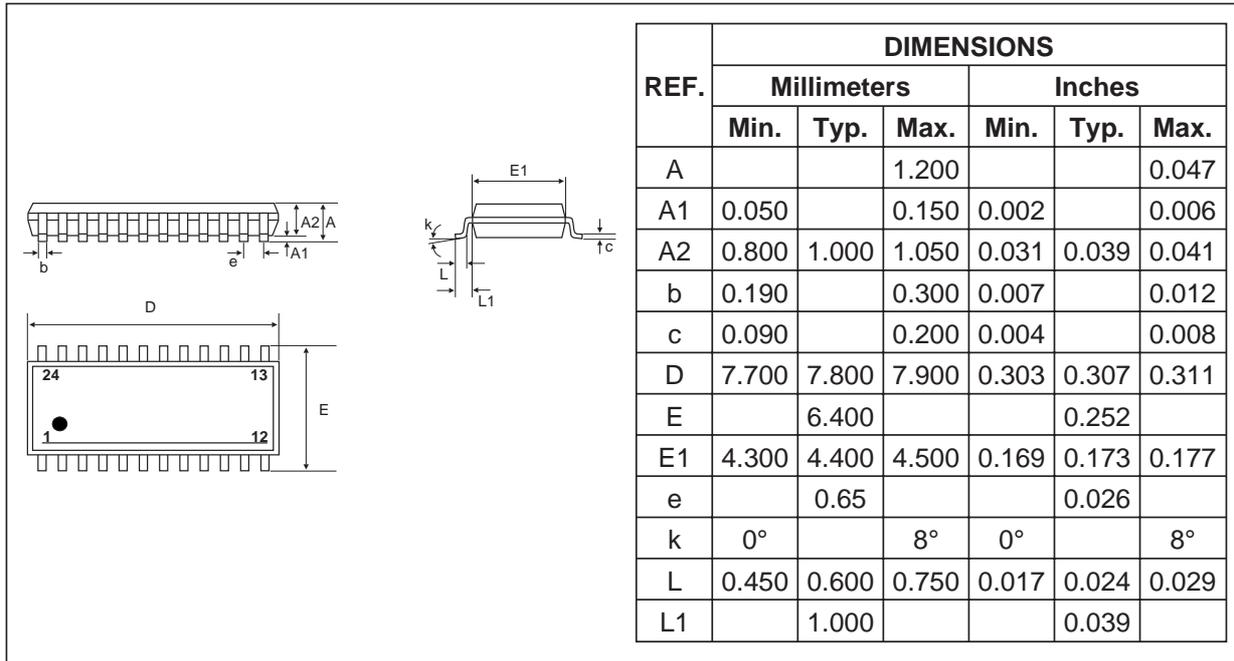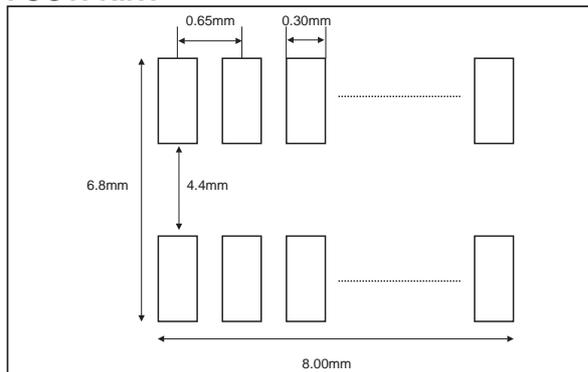
Type	Marking	Package	Weight	Base qty	Delivery mode
DDR110-27T7RL	DDR110-27	TSSOP-24	0.088 g	2500	Tape & Reel
DDR110-56T7RL	DDR110-56	TSSOP-24	0.088 g	2500	Tape & Reel

■ Epoxy meets UL94 - V0 standard