- **Organization**
  - **TM497BBK32H/I: 4194304 x 32**
  - **TM893CBK32H/I: 8388608 x 32**
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Single-In-Line Memory Module (SIMM) for Use With Sockets**
- **TM497BBK32H/I – Uses Eight 16M-Bit Dynamic Random-Access Memory (DRAM) Devices in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM893CBK32H/I – Uses Sixteen 16M-Bit DRAMs in Plastic SOJ Packages**
- **Long Refresh Period 32 ms (2 048 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL-Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines in Four Blocks**
- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR), $\overline{RAS}$-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'497BBK32H/I-50	50 ns	25 ns	13 ns	90 ns
'497BBK32H/I-60	60 ns	30 ns	15 ns	110 ns
'497BBK32H/I-70	70 ns	35 ns	18 ns	130 ns
'893CBK32H/I-50	50 ns	25 ns	13 ns	90 ns
'893CBK32H/I-60	60 ns	30 ns	15 ns	110 ns
'893CBK32H/I-70	70 ns	35 ns	18 ns	130 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Gold-Tabbed Version Available:† TM497BBK32H, TM893CBK32H**
- **Tin-Lead (Solder-) Tabbed Version Available: TM497BBK32I, TM893CBK32I**

description

The TM497BBK32H/I is a 16M-byte dynamic random-access memory (DRAM) device organized as 4 × 4194304 × 8 bits in a 72-pin leadless single-in-line memory module (SIMM). The SIMM is composed of eight TMS417400ADJ, 4194304 × 4-bit DRAMs, each in 24/26-lead plastic small-outline J-lead (SOJ) packages mounted on a substrate with decoupling capacitors. The TMS417400ADJ is described in the TMS417400A data sheet (literature number SMKS889).

The TM497BBK32H/I SIMM is available in the single-sided BK leadless module for use with sockets. The TM497BBK32H/I features $\overline{RAS}$ access times of 50, 60, and 70 ns. This device is characterized for operation from 0°C to 70°C.

The TM893CBK32H/I is a 32M-byte DRAM organized as 4 × 8388608 × 8 bits in a 72-pin leadless SIMM. The SIMM is composed of sixteen TMS417400ADJ, 4194304 × 4-bit DRAMs.

The TM893CBK32H/I SIMM is available in the double-sided BK leadless module for use with sockets. The TM893CBK32H/I features $\overline{RAS}$ access times of 50, 60, and 70 ns. This device is characterized for operation from 0°C to 70°C.

operation

The TM497BBK32H/I operates as eight TMS417400ADJs connected as shown in the functional block diagram and in Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

operation (continued)

The TM893CBK32H/I operates as sixteen TMS417400ADJs connected as shown in the functional block diagram and in Table 2. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

Table 1 and Table 2 show TM497BBK32H/I and TM389CBK32H/I data block configurations in reference to $\overline{RAS}$ and $\overline{CAS}$ interfacing.

Table 1. TM497BBK32H/I Connection Table

DATA BLOCK	$\overline{RASx}$	$\overline{CASx}$
DQ0–DQ7	$\overline{RAS0}$	$\overline{CAS0}$
DQ8–DQ15	$\overline{RAS0}$	$\overline{CAS1}$
DQ16–DQ23	$\overline{RAS2}$	$\overline{CAS2}$
DQ24–DQ31	$\overline{RAS2}$	$\overline{CAS3}$

Table 2. TM893CBK32H/I Connection Table

DATA BLOCK	$\overline{RASx}$		$\overline{CASx}$
	Side 1	Side 2	
DQ0–DQ7	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ8–DQ15	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ16–DQ23	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ24–DQ31	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$

single-in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM497BBK32H and TM893CBK32H: Nickel plate and gold plate over copper
Contact area for TM497BBK32I and TM893CBK32I: Nickel plate and tin-lead over copper

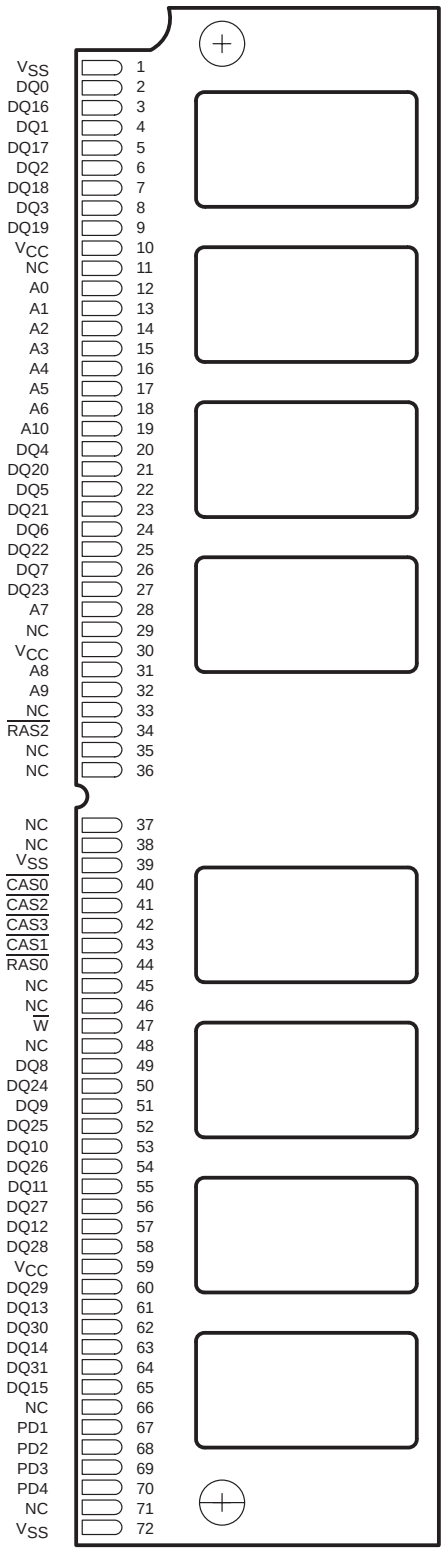
refresh

The refresh period is extended to 32 ms and, during this period, each of the 2 048 rows must be strobed with $\overline{RAS}$ to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

power up

To achieve proper operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

BK SINGLE-IN-LINE PACKAGE
(TOP VIEW)



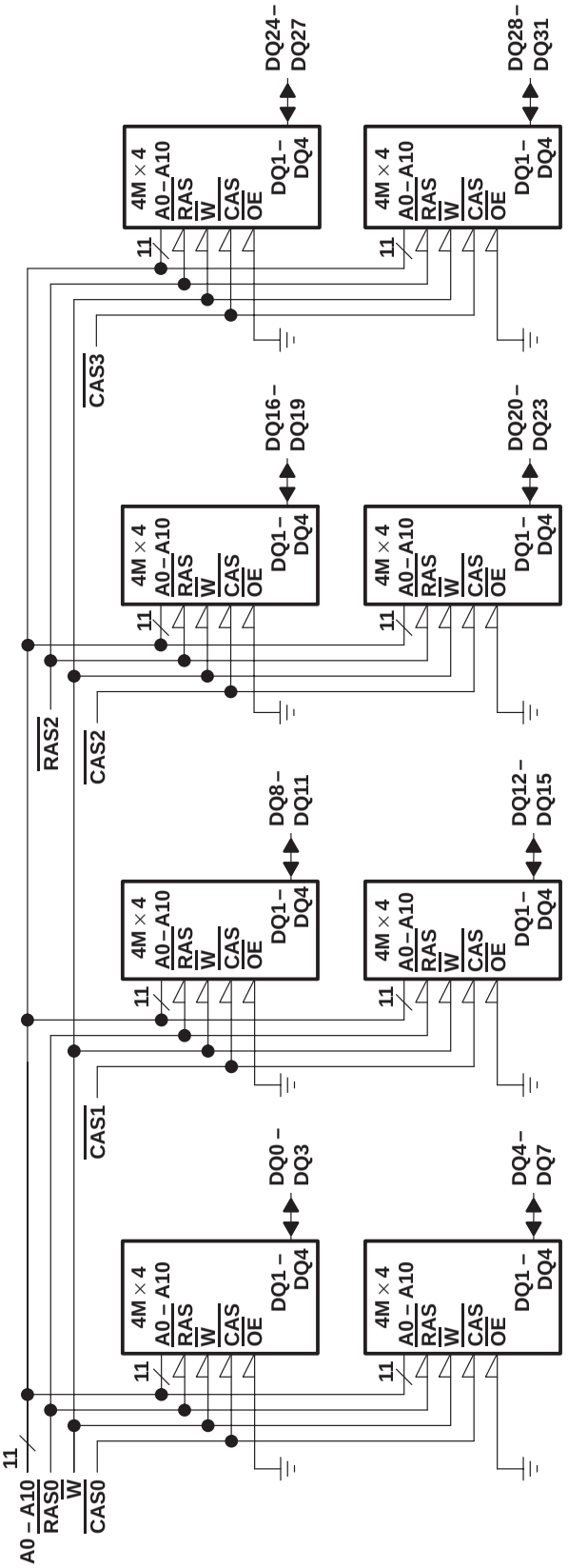
TM497BBK32H/I
(SIDE VIEW)

TM893CBK32H/I
(SIDE VIEW)

PIN NOMENCLATURE	
$\overline{A0}$–$\overline{A10}$	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ31	Data In/Data Out
NC	No Connection
$\overline{PD1}$–$\overline{PD4}$	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM497BBK32H/I	50 ns	V_{SS}	NC	V_{SS}	V_{SS}
	60 ns	V_{SS}	NC	NC	NC
	70 ns	V_{SS}	NC	V_{SS}	NC
TM893CBK32H/I	50 ns	NC	V_{SS}	V_{SS}	V_{SS}
	60 ns	NC	V_{SS}	NC	NC
	70 ns	NC	V_{SS}	V_{SS}	NC

functional block diagram of TM497BBK32H/I



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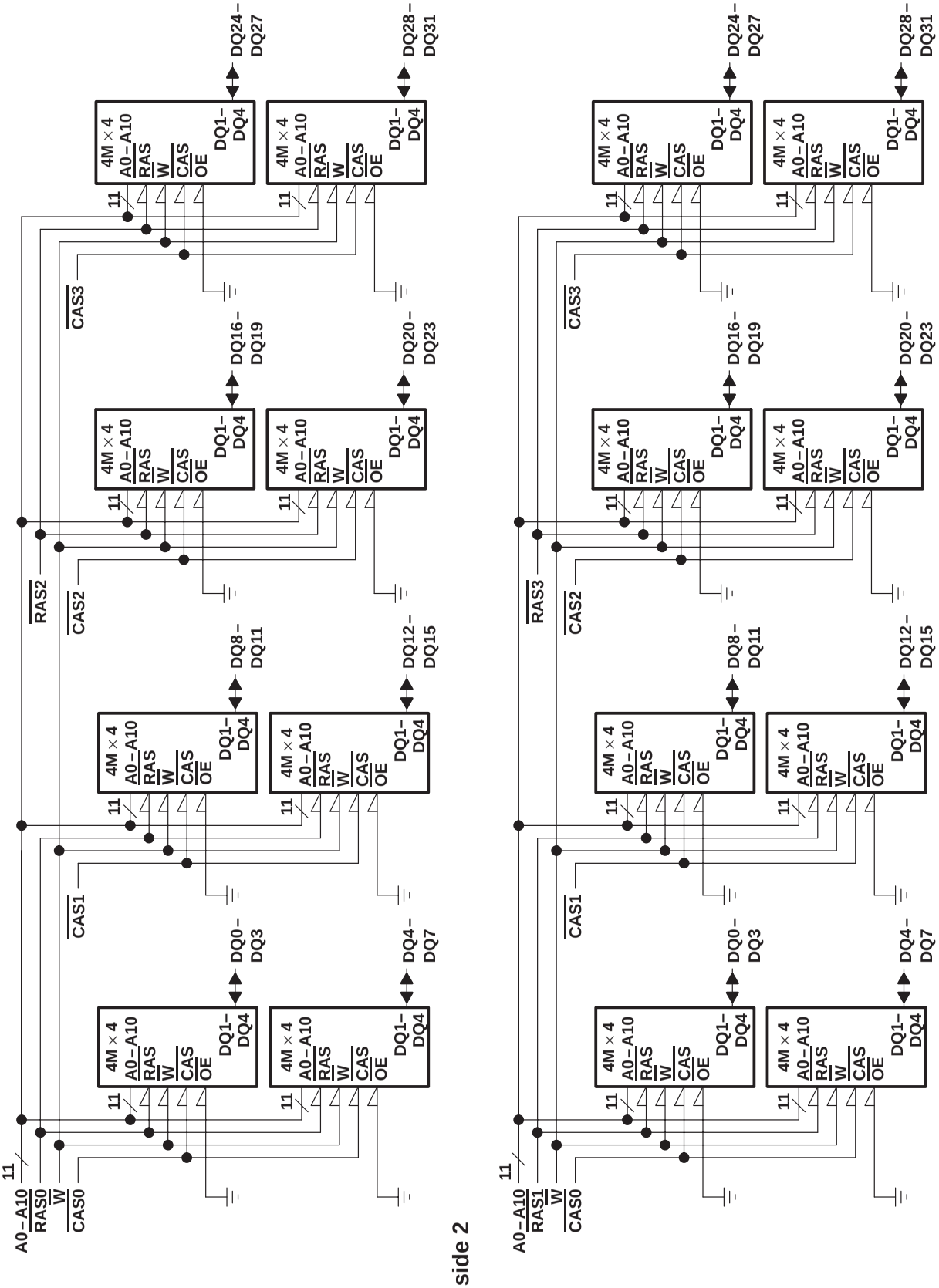
functional block diagram of TM893CBK32H/I



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . – 1 V to 7 V
Voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 16 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	'497BBK32H/I-50		'497BBK32H/I-60		'497BBK32H/I-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		1040		880		800	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		16		16		16	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		8		8		8	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, $\overline{RAS}$ cycling, ($\overline{RAS}$ only); $\overline{CAS}$ low (CBR)	Minimum cycle, $\overline{CAS}$ high $\overline{RAS}$ low after	1040		880		800	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, $\overline{RAS}$ low,	t_{PC} = MIN, $\overline{CAS}$ cycling	720		560		480	mA

‡ For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	'893CBK32H/I-50		'893CBK32H/I-60		'893CBK32H/I-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 20		± 20		± 20	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$x high		± 20		± 20		± 20	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		1048		888		808	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$x and $\overline{CAS}$x high		32		32		32	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$x and $\overline{CAS}$x high		16		16		16	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, $\overline{RAS}$x cycling, ($\overline{RAS}$x only); Minimum cycle $\overline{CAS}$x low (CBR) $\overline{CAS}$x high $\overline{RAS}$x low after		2080		1760		1600	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$x low, $\overline{CAS}$x cycling		1440		1120		960	mA

† For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		TM497BBK32H/I		TM893CBK32H/I		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		50		80	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs		33		28	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs		17		28	pF
$C_{i(W)}$	Input capacitance, write-enable input		66		112	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		9		14	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		’497BBK32H/I-50 ’893CBK32H/I-50		’497BBK32H/I-60 ’893CBK32H/I-60		’497BBK32H/I-70 ’893CBK32H/I-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		25		30		35	ns
t_{CAC}	Access time from $\overline{CAS}$ low		13		15		18	ns
t_{CPA}	Access time from column precharge		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		50		60		70	ns
t_{CLZ}	$\overline{CAS}$ to output in low-impedance state	0		0		0		ns
t_{OH}	Output disable time from start of $\overline{CAS}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	13	0	15	0	18	ns

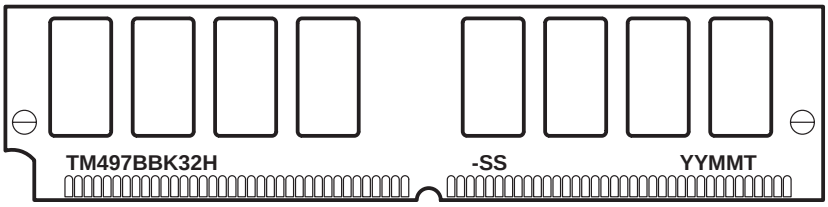
NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		’497BBK32H/I-50 ’893CBK32H/I-50		’497BBK32H/I-60 ’893CBK32H/I-60		’497BBK32H/I-70 ’893CBK32H/I-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	90		110		130		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 7 and 8)	35		40		45		ns
t_{RASP}	Pulse duration, page-mode, $\overline{RAS}$ low	50	100 000	60	100 000	70	100 000	ns
t_{RAS}	Pulse duration, non-page-mode, $\overline{RAS}$ low	50	10 000	60	10 000	70	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	13	10 000	15	10 000	18	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	8		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	30		40		50		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{CAS}$ low	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$-low before $\overline{CAS}$ high	13		15		18		ns
t_{RWL}	Setup time, $\overline{W}$-low before $\overline{RAS}$ high	13		15		18		ns
t_{WCS}	Setup time, $\overline{W}$-low before $\overline{CAS}$ low	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$-high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		10		15		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high after $\overline{CAS}$ precharge	30		35		40		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low	10		10		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	8		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low	10		10		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	50		60		70		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	5		5		5		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	13	25	15	30	15	35	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	25		30		35		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	25		30		35		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	18	37	20	45	20	52	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR only)	5		5		5		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	13		15		18		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	2	30	2	30	2	30	ns

NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. The maximum value is specified only to ensure access time.

device symbolization

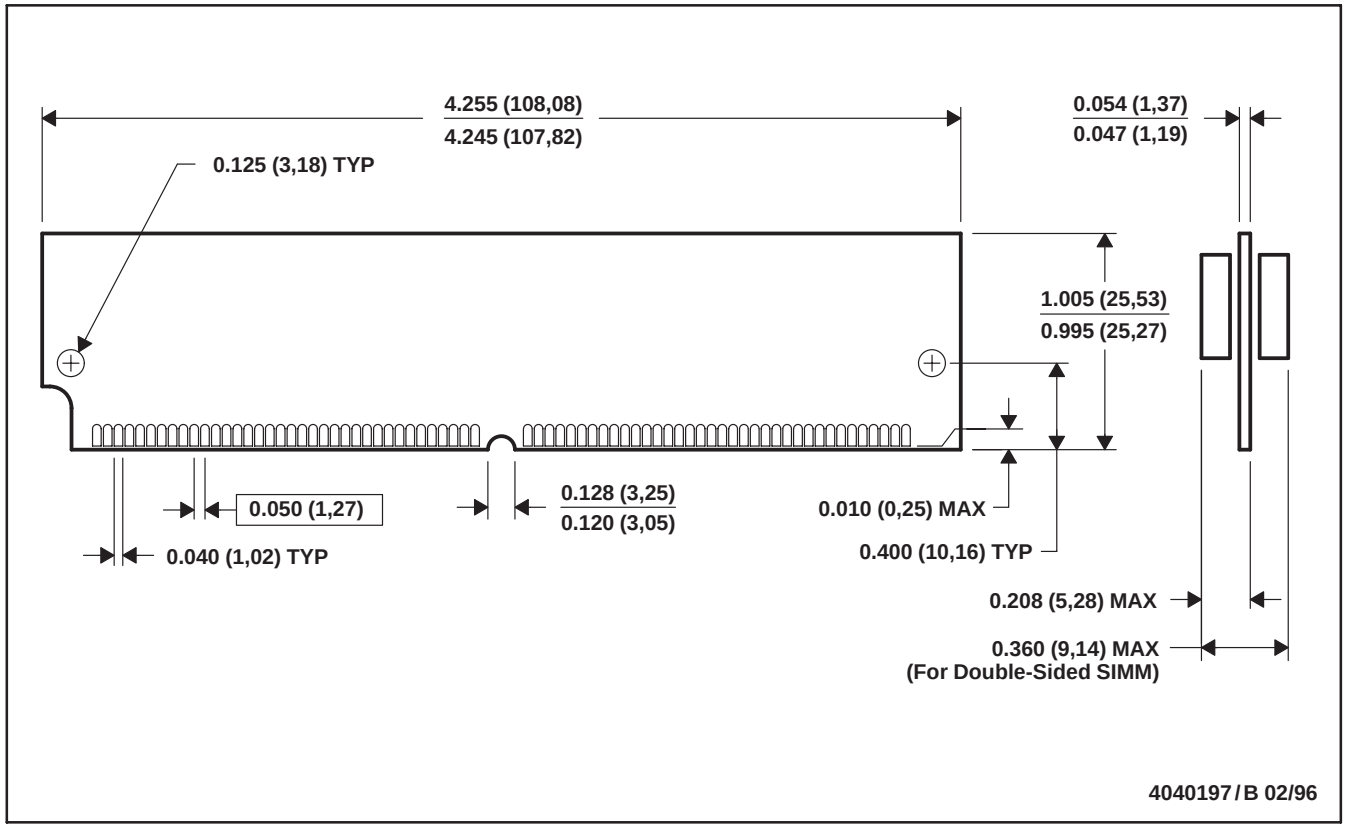


YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE A: The location of the part number may vary.

MECHANICAL DATA

BK (R-PSIM-N72) **SINGLE-IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

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