- **Organization:**
  – TM8TU72JPW . . . 8 388 608 × 72 Bits
- **Designed for 100-MHz, 72-Bit 4-Clock Systems**
- **JEDEC 168-Pin Dual-In-Line Memory Module (DIMM) With Register for Use With Socket**
- **TM8TU72JPW — Uses Nine 64M-Bit (8M × 8-Bit) SDRAMs in Plastic Thin Small-Outline Package (TSOP), Two SN74ALVC162836 20-Bit Universal Bus Drivers in Thin Shrink Small-Outline Package (TSSOP), and One CDC2510 Phase-Lock Loop (PLL) in TSSOP**
- **Single 3.3-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**
- **Byte-Read/Write Capability**
- **High-Speed, Low-Noise, Low-Voltage TTL (LVTTL) Interface**
- **Read Latencies 2 and 3 Supported**
- **Supports Burst-Interleave and Burst-Interrupt Operations**
- **Burst Length Programmable to 1, 2, 4, and 8**
- **Four Banks for On-Chip Interleaving (Gapless Access)**
- **Ambient Temperature Range 0°C to 70°C**
- **Gold-Plated Contacts**
- **Pipeline Architecture**
- **Serial Presence-Detect (SPD) Using EEPROM**

	SYNCHRONOUS CLOCK CYCLE TIME		ACCESS TIME CLOCK TO OUTPUT		REFRESH INTERVAL
	t_{CK3}	t_{CK2}	t_{AC3}	t_{AC2}	t_{REF}
’8TU72JPW-8	8 ns	10 ns	6 ns	6 ns	64 ms
’8TU72JPW-8A	8 ns	10 ns	6 ns	7.5 ns	64 ms

description

The TM8TU72JPW is a 64M-byte, 168-pin registered dual-in-line memory module (DIMM). The registered DIMM is composed of nine TMS664814DGE, 8 388 608 x 8-bit SDRAMs, each in a 400-mil, 54-pin plastic thin small-outline package (TSOP); two SN74ALVC162836DGG, 20-bit universal bus drivers, each in a 240-mil, 56-pin thin shrink small-outline package (TSSOP); and one CDC2510 phase-lock loop (PLL) in a 177-mil, 24-pin TSSOP mounted on a substrate with decoupling capacitors. See the TMS664814 data sheet (literature number SMOS695), the SN74ALVC162836 data sheet (literature number SCES129), and the CDC2510 data sheet (literature number SCAS597) for reference.

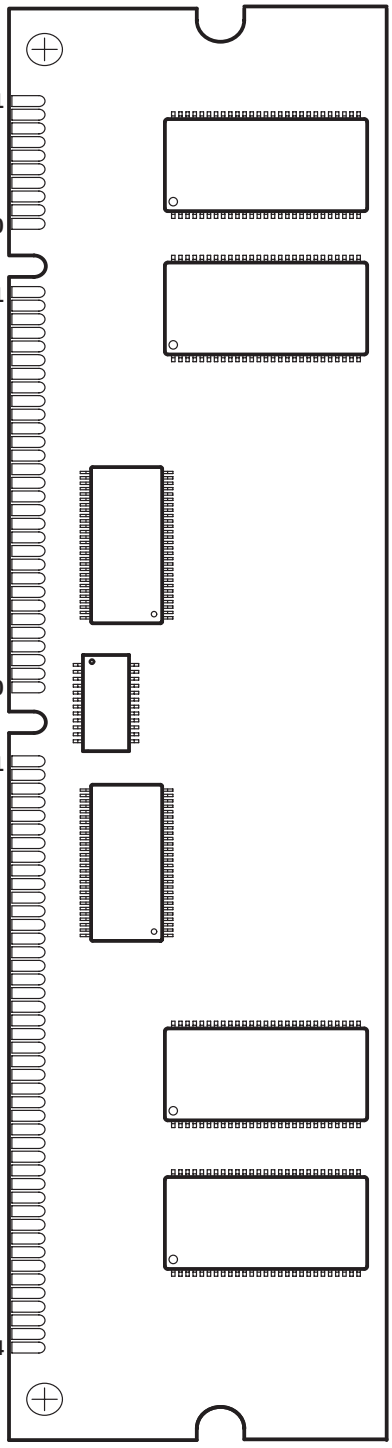
operation

The TM8TU72JPW operates as nine TMS664814DGE devices that are connected as shown in the TM8TU72JPW functional block diagram.

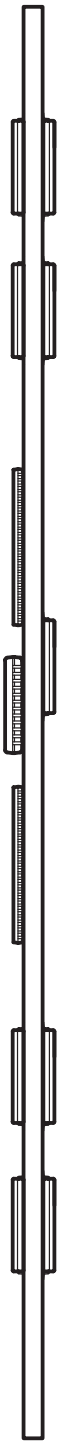
PRODUCT PREVIEW

PRODUCT PREVIEW

DUAL-IN-LINE MEMORY MODULE (TOP VIEW)



TM8TU72JPW (SIDE VIEW)



PIN NOMENCLATURE	
A[0:11]	Row-Address Inputs
A[0:8]	Column-Address Inputs
A13/BA0	Bank-Select Zero
A12/BA1	Bank-Select One
$\overline{\text{CAS}}$	Column-Address Strobe
CB[0:7]	Check-Bit In/Check-Bit Out
CKE[0:1]	Clock Enable
CK[0:3]	System Clock
DQ[0:63]	Data-In / Data-Out
DQMB[0:7]	Data-In/Data-Out Mask Enable
$\overline{\text{NC}}$	No Connect
$\overline{\text{RAS}}$	Row-Address Strobe
$\overline{\text{REGE}}$	Register Enable
$\overline{\text{S}}$[0:3]	Chip Select
SA[0:2]	Serial Presence-Detect (SPD) Device Address Input
SCL	SPD Clock
SDA	SPD Address / Data
V_{DD}	3.3-V Supply
$V_{\overline{SS}}$	Ground
$\overline{\text{WE}}$	Write Enable
WP	Write Protect

Pin Assignments

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	$\overline{S2}$	87	DQ33	129	$\overline{S3}$
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{DD}	48	NC	90	V_{DD}	132	NC
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	REGE
22	CB1	64	V_{SS}	106	CB5	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	$\overline{WE}$	69	DQ24	111	$\overline{CAS}$	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	$\overline{S0}$	72	DQ27	114	$\overline{S1}$	156	DQ59
31	NC	73	V_{DD}	115	$\overline{RAS}$	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	A13/BA0	164	NC
39	A12/BA1	81	WP	123	A11	165	SA0
40	V_{DD}	82	SDA	124	V_{DD}	166	SA1
41	V_{DD}	83	SCL	125	CK1	167	SA2
42	CK0	84	V_{DD}	126	NC	168	V_{DD}

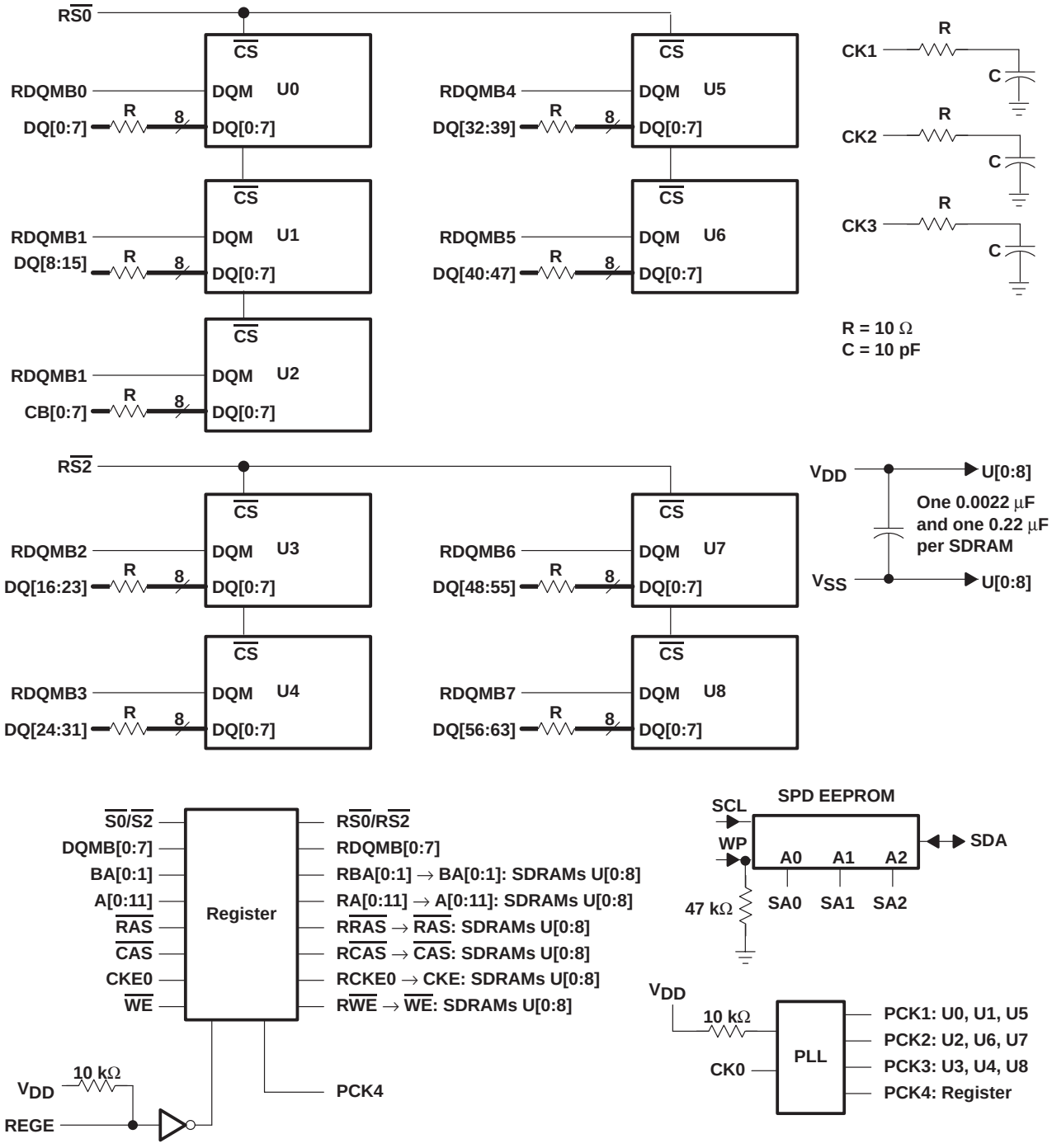
PRODUCT PREVIEW

dual-in-line memory module and components

The dual-in-line memory module and components include:

- PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

functional block diagram for the TM8TU72JPW



LEGEND: $\overline{CS}$ = Chip Select
SPD = Serial Presence Detect
PLL = Phase-Lock Loop

PRODUCT PREVIEW

absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . –0.5 V to 4.6 V
Voltage range on any pin (see Note 1) . . . . . – 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 9 W
Ambient temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2		V_{DD} + 0.3	V
V_{IH-SPD}	High-level input voltage for SPD device	2		5.5	V
V_{IL}	Low-level input voltage	–0.3		0.8	V
T_A	Ambient temperature	0		70	°C

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 2)

PARAMETER		MIN	MAX	UNIT
$C_{i(CK)}$	Input capacitance, CK input		38	pF
$C_{i(AC)}$	Input capacitance, address and control inputs: A0–A13, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$		10	pF
$C_{i(CKE)}$	Input capacitance, CKE input		10	pF
C_o	Output capacitance		15	pF
$C_{i(DQMBx)}$	Input capacitance, DQMBx input		10	pF
$C_{i(Sx)}$	Input capacitance, $\overline{Sx}$ input		9	pF
$C_{i/o(SDA)}$	SDA Input/output capacitance		12	pF
$C_{i(SPD)}$	Input capacitance, SA0, SA1, SA2, SCL inputs		10	pF

NOTE 2: V_{DD} = 3.3 V ± 0.3 V. Bias on pins under test is 0 V.

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 3)

PARAMETER		TEST CONDITIONS		'8TU72JPW-8		'8TU72JPW-8A		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
I_I	Input current (leakage)	0 V ≤ V_I ≤ V_{DD} + 0.3 V, All other pins = 0 V to V_{DD}			±10		±10	µA
I_O	Output current (leakage)	0 V ≤ V_O ≤ V_{DD} + 0.3 V, Output disabled			±10		±10	µA
I_{CC1}	Operating current	Burst length = 1, t_{RC} ≥ t_{RC} MIN, I_{OH}/I_{OL} = 0 mA (see Notes 4, 5, and 6)	CAS latency = 2		TBD		TBD	mA
			CAS latency = 3		TBD		TBD	
I_{CC2P}	Precharge standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 7)			TBD		TBD	mA
I_{CC2N}	Active standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 7)			TBD		TBD	mA
I_{CC3P}	Active standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Notes 4 and 7)			TBD		TBD	mA
I_{CC3N}	Precharge standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Notes 4 and 7)			TBD		TBD	mA
I_{CC4}	Burst current	Page burst, I_{OH}/I_{OL} = 0 mA All banks activated, n_{CCD} = one cycle (see Notes 9 and 10)	CAS latency = 2		TBD		TBD	mA
			CAS latency = 3		TBD		TBD	
I_{CC5}	Auto-refresh current	t_{RC} ≤ t_{RC} MIN (see Notes 5 and 8)	CAS latency = 2		TBD		TBD	mA
			CAS latency = 3		TBD		TBD	mA
I_{CC6}	Self-refresh current	CKE ≤ V_{IL} MAX			TBD		TBD	mA

NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
4. Only one bank is activated.
5. t_{RC} ≥ t_{RC}MIN
6. Control and address inputs change state twice during t_{RC}.
7. Control and address inputs change state once every 30 ns.
8. Control and address inputs do not change state (stable).
9. Control and address inputs change state once every cycle.
10. Continuous burst access, n_{CCD} = 1 cycle

PRODUCT PREVIEW

ac timing requirements†‡

			'8TU72JPW-8		'8TU72JPW-8A		UNIT
			MIN	MAX	MIN	MAX	
t_{CK2}	Cycle time, CK	CAS latency = 2	10		15		ns
t_{CK3}	Cycle time, CK	CAS latency = 3	8		8		ns
t_{CH}	Pulse duration, CK high (input clock duty cycle)		40	60	40	60	%
t_{CL}	Pulse duraction, CK low (input clock duty cycle)		40	60	40	60	%
t_{AC2}	Access time, CK high to data out (see Note 11)	CAS latency = 2		6		7.5	ns
t_{AC3}	Access time, CK high to data out (see Note 11)	CAS latency = 3		6		6	ns
t_{OH}	Hold time, CK high to data out with 50-pF load		3		3		ns
t_{LZ}	Delay time, CK high to DQ in low-impedance state (see Note 12)		1		1		ns
t_{HZ}	Delay time, CK high to DQ in high-impedance state (see Note 13)			8		8	ns
t_{IS}	Setup time, address, control, and data input		2		2		ns
t_{IH}	Hold time, address, control, and data input		1		1		ns
t_{RAS}	Delay time, ACTV command to DEAC or DCAB command		48	100 000	48		ns
t_{RC}	Delay time, ACTV, MRS, REFR, or SLFR to ACTV, MRS, REFR, or SLFR command		68		68		ns
t_{RCD}	Delay time, ACTV command to READ, READ-P, WRT, or WRT-P command (see Note 14)		20		20		ns
t_{RP}	Delay time, DEAC or DCAB command to ACTV, MRS, REFR, or SLFR command		20		20		ns
t_{RRD}	Delay time, ACTV command in one bank to ACTV command in the other bank		16		16		ns
t_{RSA}	Delay time, MRS command to ACTV, MRS, REFR, or SLFR command		16		16		ns
t_{APR}	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command		t_{RP} –(CL–1)*t_{CK}		t_{RP}–(CL–1)*t_{CK}		ns
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command		t_{RP} + 1 t_{CK}		t_{RP} + 1 t_{CK}		ns
t_T	Transition time		1	5	1	5	ms
t_{REF}	Refresh interval			64		64	ms
n_{CCD}	Delay time, READ or WRT command to an interrupting command		1		1		cycles
n_{CDD}	Delay time, CS low or high to input enabled or inhibited		0	0	0	0	cycles
n_{CESP}	Power down/self-refresh exit time		1		1		cycles
n_{CLE}	Delay time, CKE high or low to CLK enabled or disabled		1	1	1	1	cycles
n_{CWL}	Delay time, final data in of WRT operation to READ, READ-P, WRT, or WRT-P		1		1		cycles
n_{DID}	Delay time, ENBL or MASK command to enabled or masked data in		0	0	0	0	cycles
n_{DOD}	Delay time, ENBL or MASK command to enabled or masked data out		2	2	2	2	cycles
n_{HZP2}	Delay time, DEAC or DCAB, command to DQ in high-impedance state	CAS latency = 2		2		2	cycles
n_{HZP3}	Delay time, DEAC or DCAB, command to DQ in high-impedance state	CAS latency = 3		3		3	cycles
n_{WCD}	Delay time, WRT command to first data in		0	0	0	0	cycles
n_{WR}	Delay time, final data in of WRT operation to DEAC or DCAB command		1		1		cycles

† All references are made to the rising transition of CK unless otherwise noted.
‡ Specifications in this table represent a single SDRAM device.

NOTES: 11. t_{AC} is referenced from the rising transition of CK that precedes the data-out cycle. For example, the first data out t_{AC} is referenced from the rising transition of CK that is read latency (one cycle after the READ command). Access time is measured at output reference level 1.4 V.
12. t_{LZ} is measured from the rising transition of CK that is read latency (one cycle after the READ command).
13. t_{HZ} (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
14. For read or write operations with automatic deactivate, t_{RCD} must be set to satisfy minimum t_{RAS}.

PRODUCT PREVIEW

serial presence detect

The serial presence detect (SPD) is contained in a 256-byte serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, SDRAM organization, and timing parameters (see Table 1). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through an IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD Standard. See the Texas Instruments *Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.

Tables in this section list the SPD contents as follows:

Table 1—TM8TU72JPW

Table 1. Serial Presence-Detect Data for the TM8TU72JPW

BYTE NO.	DESCRIPTION OF FUNCTION	TM8TU72JPW-8		TM8TU72JPW-8A	
		ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM, . . .)	SDRAM	04h	SDRAM	04h
3	Number of row addresses on this assembly	12	0Ch	12	0Ch
4	Number of column addresses on this assembly	9	09h	9	09h
5	Number of module rows on this assembly	1 bank	01h	1 bank	01h
6	Data width of this assembly	72 bits	48h	72 bits	48h
7	Data width continuation		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL = X	t_{CK} = 8 ns	80h	t_{CK} = 8 ns	80h
10	SDRAM access from clock at CL = X	t_{AC} = 6 ns	60h	t_{AC} = 6 ns	60h
11	DIMM configuration type (non-parity, parity, error-correcting code [ECC])	ECC	02h	ECC	02h
12	Refresh rate/type	15.6 µs/ self-refresh	80h	15.6 µs/ self-refresh	80h
13	SDRAM width, primary DRAM	x8	08h	x8	08h
14	Error-checking SDRAM data width	x8	08h	x8	08h
15	Minimum clock delay, back-to-back random column addresses	1 CK cycle	01h	1 CK cycle	01h
16	Burst lengths supported	1, 2, 4, 8	0Fh	1, 2, 4, 8	0Fh
17	Number of banks on each SDRAM device	4 banks	04h	4 banks	04h
18	CAS latencies supported	2, 3	06h	2, 3	06h
19	CS latency	0	01h	0	01h
20	Write latency	0	01h	0	01h
21	SDRAM module attributes	Registered, PLL	16h	Registered, PLL	16h
22	SDRAM device attributes: general	V_{DD} tolerance = (±10%), Burst read/write, precharge all, auto precharge	0Eh	V_{DD} tolerance = (±10%), Burst read/write, precharge all, auto precharge	0Eh
23	Minimum clock cycle time at CL = X – 1	t_{CK} = 10 ns	A0h	t_{CK} = 15 ns	F0h
24	Maximum data-access time from clock at CL = X – 1	t_{AC} = 6 ns	60h	t_{AC} = 7.5 ns	75h
25	Minimum clock cycle time at CL = X – 2	N/A	00h	N/A	00h
26	Maximum data-access time from clock at CL = X – 2	N/A	00h	N/A	00h

PRODUCT PREVIEW

serial presence detect (continued)

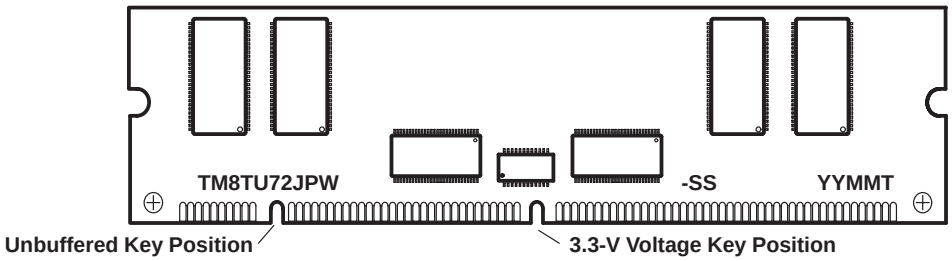
Table 1. Serial Presence-Detect Data for the TM8TU72JPW (Continued)

BYTE NO.	DESCRIPTION OF FUNCTION	TM8TU72JPW-8		TM8TU72JPW-8A	
		ITEM	DATA	ITEM	DATA
27	Minimum row precharge time	t_{RP} = 20 ns	14h	t_{RP} = 20 ns	14h
28	Minimum row-active to row-active delay	t_{RRD} = 16 ns	10h	t_{RRD} = 16 ns	10h
29	Minimum $\overline{RAS}$-to-$\overline{CAS}$ delay	t_{RCD} = 20 ns	14h	t_{RCD} = 20 ns	14h
30	Minimum $\overline{RAS}$ pulse width	t_{RAS} = 48 ns	30h	t_{RAS} = 48 ns	30h
31	Density of each bank on module	64M Bytes	10h	64M Bytes	10h
32	Command and address signal input setup time	t_{IS} = 2 ns	20h	t_{IS} = 2 ns	20h
33	Command and address signal input hold time	t_{IH} = 1 ns	10h	t_{IH} = 1 ns	10h
34	Data signal input setup time	t_{IS} = 2 ns	20h	t_{IS} = 2 ns	20h
35	Data signal input hold time	t_{IH} = 1 ns	10h	t_{IH} = 1 ns	10h
36–61	Superset features (may be used in the future)				
62	SPD revision	Rev. 1.2	12h	Rev. 1.2	12h
63	Checksum for byte 0–62	135	87h	236	ECh
64–71	Manufacturer's JEDEC ID code per JEP–106E	97h	9700... 00h	97h	9700... 00h
72	Manufacturing location†	TBD		TBD	
73	Manufacturer's part number	T	54h	T	54h
74	Manufacturer's part number	M	4Dh	M	4Dh
75	Manufacturer's part number	8	38h	8	38h
76	Manufacturer's part number	T	54h	T	54h
77	Manufacturer's part number	U	55h	U	55h
78	Manufacturer's part number	7	37h	7	37h
79	Manufacturer's part number	2	32h	2	32h
80	Manufacturer's part number	J	4Ah	J	4Ah
81	Manufacturer's part number	P	50h	P	50h
82	Manufacturer's part number	W	57h	W	57h
83	Manufacturer's part number	–	2Dh	–	2Dh
84	Manufacturer's part number	8	38h	8	38h
85	Manufacturer's part number	SPACE	20h	A	41h
86–90	Manufacturer's part number	SPACE	20h	SPACE	20h
91	Die revision code†	TBD		TBD	
92	PCB revision code†	TBD		TBD	
93–94	Manufacturing date†	TBD		TBD	
95–98	Assembly serial number†	TBD		TBD	
99–125	Manufacturer-specific data†	TBD		TBD	
126	Clock Frequency	100 MHz	64h	100 MHz	64h
127	SDRAM component and clock interconnection details	199	C7h	199	C7h
128–166	System-integrator-specific data‡	TBD		TBD	
167–255	Open				

† TBD indicates values are determined at manufacturing time and are module-dependent.
‡ These TBD values are determined and programmed by the customer (optional).

PRODUCT PREVIEW

device symbolization

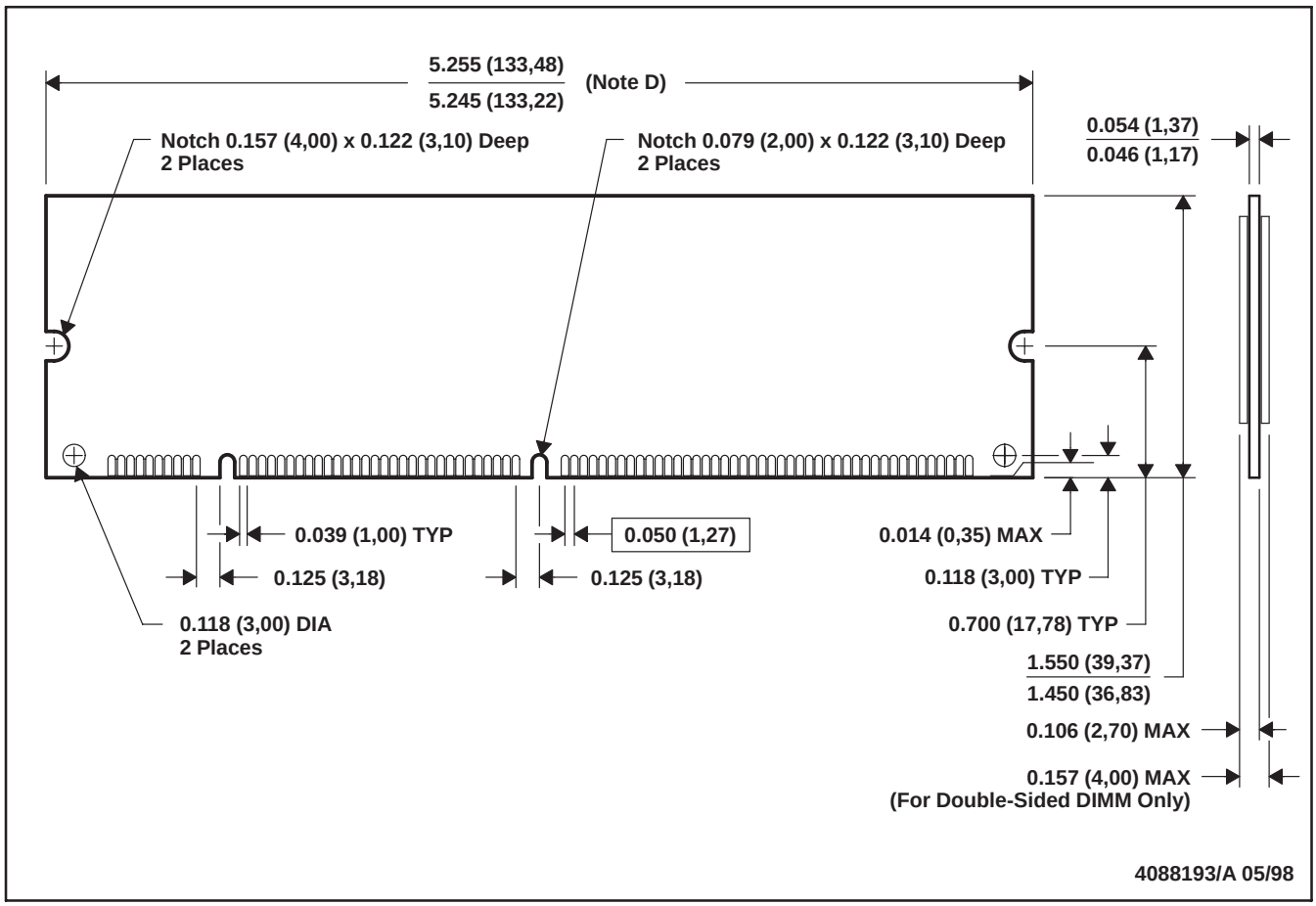


YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE A: Location of symbolization may vary.

PRODUCT PREVIEW

BVC (R-PDIM-N168) **DUAL-IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-161
D. Dimension includes depanelization variations; applies between notch and tab edge.
E. Outline may vary above notches to allow router/panelization irregularities.

PRODUCT PREVIEW

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.