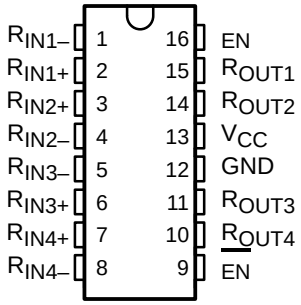
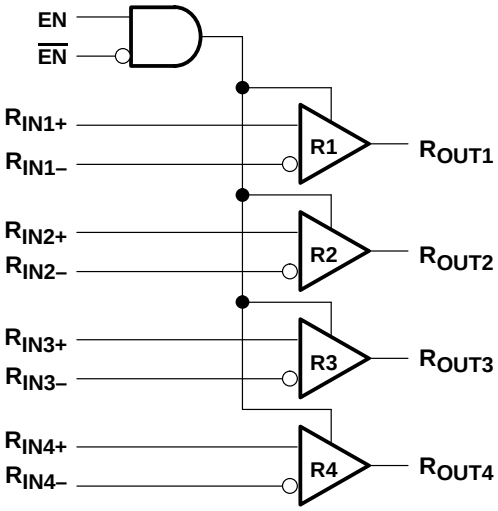
- **>400 Mbps (200 MHz) Signaling Rates**
- **Flow-Through Pinout Simplifies PCB Layout**
- **50 ps Channel-to-Channel Skew (Typ)**
- **200 ps Differential Skew (Typ)**
- **Propagation Delay Times 2.7 ns (Typ)**
- **3.3-V Power Supply Design**
- **High Impedance LVDS Inputs on Power Down**
- **Low-Power Dissipation (40 mW at 3.3 V Static)**
- **Accepts Small Swing (350 mV) Differential Signal Levels**
- **Supports Open, Short, and Terminated Input Fail-Safe**
- **Industrial Operating Temperature Range (–40°C to 85°C)**
- **Conforms to TIA/EIA-644 LVDS Standard**
- **Available in SOIC and TSSOP Packages**
- **Pin-Compatible With DS90LV048A From National**

SN65LVDS048AD (Marked as LVDS048A)
SN65LVDS048APW (Marked as DL048A)
(TOP VIEW)



functional diagram



description

The SN65LVDS048A is a quad differential line receiver that implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the quad differential receivers will provide a valid logical output state with a ±100-mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes.

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.

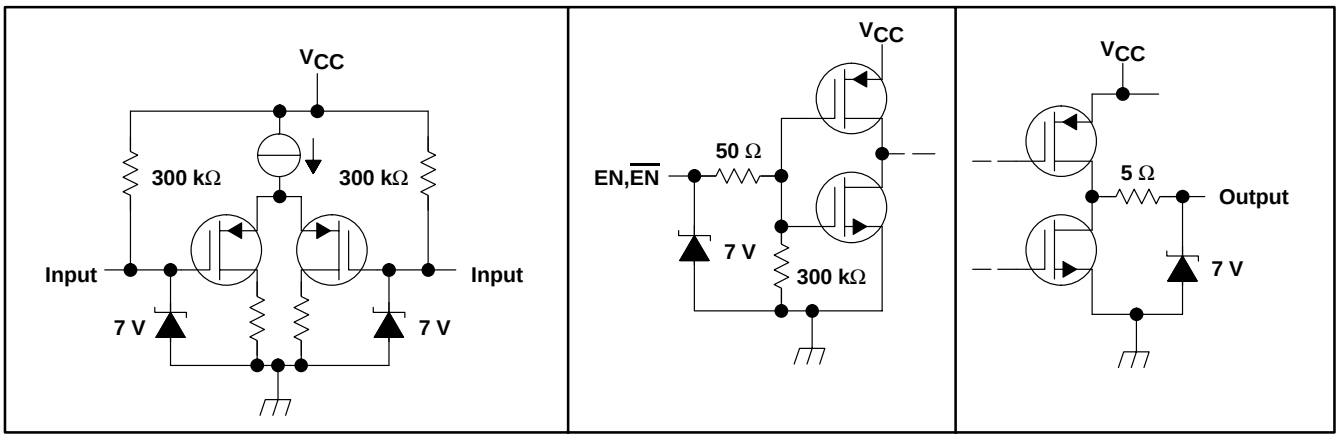
The SN65LVDS048A is characterized for operation from –40°C to 85°C.

TRUTH TABLE

DIFFERENTIAL INPUT	ENABLES		OUTPUT
$R_{IN+} - R_{IN-}$	EN	$\overline{EN}$	R_{OUT}
$V_{ID} \geq 100$ mV	H	L or OPEN	H
$V_{ID} \leq -100$ mV			L
Open/short or terminated			H
X	All other conditions		Z

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range (V_{CC}) . . . . . –0.3 V to 4 V
Input voltage range, V_I(R_{IN+}, R_{IN-}) . . . . . –0.3 V to 4 V
Enable input voltage (EN, $\overline{EN}$) . . . . . –0.3 V to (V_{CC} +0.3 V)
Output voltage, V_O(R_{OUT}) . . . . . –0.3 V to (V_{CC} +0.3 V)
Bus-pin (R_{IN+}, R_{IN-}) Electrostatic discharge (see Note 2) . . . . . > 10 kV
Continuous power dissipation . . . . . See Dissipation Rating Table
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
PW	774 mW	6.2 mW/°C	402 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Receiver input voltage	GND		3	V
Common–mode input voltage, V_{IC}	$\frac{\lvert V_{ID}\rvert}{2}$		$2.4 - \frac{\lvert V_{ID}\rvert}{2}$	V
			$V_{CC} - 0.8$	
Operating free-air temperature, T_A	–40	25	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Differential input high threshold voltage	V_{CM} = 1.2 V, 0.05 V, 2.35 V (see Note 4)				100	mV
$V_{IT–}$	Differential input low threshold voltage			–100			
$V_{(CMR)}$	Common mode voltage range	V_{ID} = 200 mV pk to pk (see Note 5)		0.1		2.3	V
I_{IN}	Input current	V_{IN} = 2.8 V	V_{CC} = 3.6 V or 0 V	–20	±1	20	µA
		V_{IN} = 0 V		–20	±1	20	µA
		V_{IN} = 3.6 V	V_{CC} = 0 V	–20	±1	20	µA
V_{OH}	Output high voltage	I_{OH} = –0.4 mA, V_{ID} = 200 mV		2.7	3.2		V
		I_{OH} = –0.4 mA, input terminated		2.7	3.2		V
		I_{OH} = –0.4 mA, input shorted		2.7	3.2		V
V_{OL}	Output low voltage	I_{OL} = 2 mA, V_{ID} = –200 mV			0.05	0.25	V
I_{OS}	Output short circuit current	Enabled, V_{OUT} = 0 V (see Note 6)			–65	–100	mA
$I_{O(Z)}$	Output 3-state current	Disabled, V_{OUT} = 0 V or V_{CC}		–1		1	µA
V_{IH}	Input high voltage			2.0		V_{CC}	V
V_{IL}	Input low voltage			GND		0.8	V
I_I	Input current (enables)	V_{IN} = 0 V or V_{CC}, Other input = V_{CC} or GND		–10		10	µA
V_{IK}	Input clamp voltage	I_{CL} = –18 mA		–1.5	–0.8		V
I_{CC}	No load supply current, receivers enabled	EN = V_{CC}, Inputs open			8	15	mA
$I_{CC(Z)}$	No load supply current, receivers disabled	EN = GND, Inputs open			0.6	1.5	mA

† All typical values are at 25°C and with a 3.3-V supply.

NOTES: 3. Current into device pin is defined as positive. Current out of the device is defined as negative. All voltages are referenced to ground, unless otherwise specified.

4. V_{CC} is always higher than R_{IN+} and $R_{IN–}$ voltage, $R_{IN–}$ and R_{IN+} have a voltage range of –0.2 V to V_{CC}–V_{ID}/2. To be compliant with ac specifications the common voltage range is 0.1 V to 2.3 V.

5. The VCMR range is reduced for larger V_{ID}, Example: If V_{ID} = 400 mV, the VCMR is 0.2 V to 2.2 V. The fail-safe condition with inputs shorted is not supported over the common-mode range of 0 V to 2.4 V, but is supported only with inputs shorted and no external common-mode voltage applied. A V_{ID} up to V_{CC}–0 V may be applied to the R_{IN+} and $R_{IN–}$ inputs with the common-mode voltage set to V_{CC}/2. Propagation delay and differential pulse skew decrease when V_{ID} is increased from 200 mV to 400 mV. Skew specifications apply for 200 mV < V_{ID} < 800 mV over the common-mode range.

6. Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time. Do not exceed maximum junction temperature specification.

switching characteristics over recommended operating conditions (unless otherwise noted) (see Notes 7)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Differential propagation delay, high-to-low	C_L = 15 pF, V_{ID} = 200 mV (see Figure 1 and 2)	1.9	2.7	3.7	ns
t_{PLH}	Differential propagation delay, low-to-high		1.9	2.9	3.7	ns
$t_{SK(p)}$	Differential pulse skew ($t_{PHLD} – t_{PLHD}$) (see Note 8)			200	450	ps
$t_{SK(o)}$	Differential channel-to-channel skew; same device (see Note 8)			50	500	ps
$t_{SK(pp)}$	Differential part-to-part skew (see Note 10)				1	ns
$t_{SK(lim)}$	Differential part-to-part skew (see Note11)				1.5	ns
t_r	Rise time			0.5	1	ns
t_f	Fall time			0.5	1	ns
t_{PHZ}	Disable time high to Z	R_L = 2 K Ω, C_L = 15 pF (see Figure 3 and 4)		8	9	ns
t_{PLZ}	Disable time low to Z			6	8	ns
t_{PZH}	Enable time Z to high			8	10	ns
t_{PZL}	Enable time Z to low			7	8	ns
$f_{(MAX)}$	Maximum operating frequency (see Note 12)	All channels switching	200	250		MHz

† All typical values are at 25°C and with a 3.3-V supply.

NOTES: 7. Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, tr and tf (0% – 100%) ≤ 3 ns for R_{IN}.

8. $t_{SK(p)}|t_{PLH} − t_{PHL}|$ is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

9. $t_{SK(o)}$ is the differential channel-to-channel skew of any event on the same device.

10. $t_{SK(pp)}$ is the differential part-to-part skew, and is defined as the difference between the minimum and the maximum specified differential propagation delays. This specification applies to devices at the same VCC and within 5°C of each other within the operating temperature range.

11. $t_{sk(lim)}$ part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. $t_{sk(lim)}$ is defined as |Min – Max| differential propagation delay.

12. $f_{(MAX)}$ generator input conditions: $t_r = t_f$ < 1 ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output criteria: duty cycle = 45% to 55%, V_{OD} > 250 mV, all channels switching

PARAMETER MEASUREMENT INFORMATION

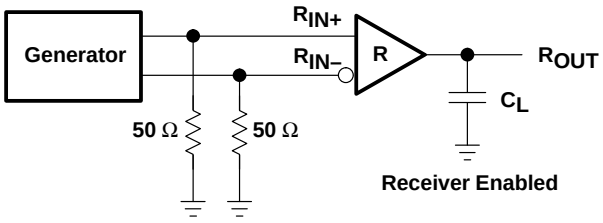


Figure 1. Receiver Propagation Delay and Transition Time Test Circuit

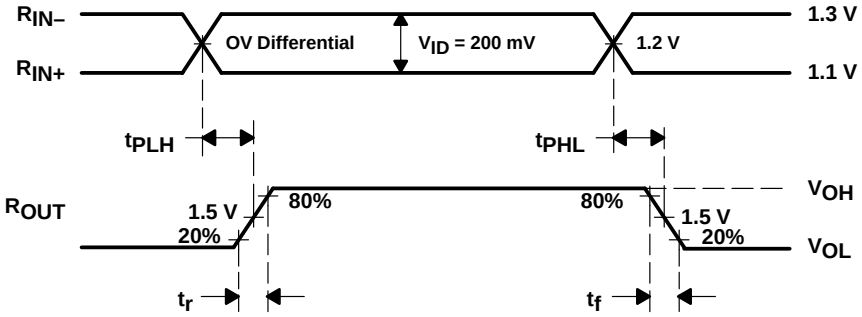
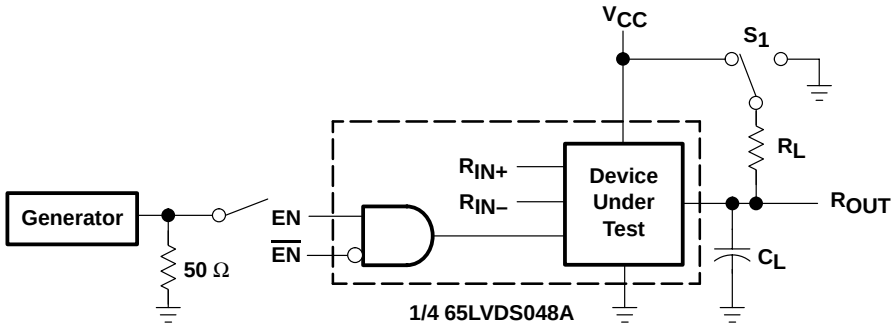


Figure 2. Receiver Propagation Delay and Transition Time Waveforms

PARAMETER MEASUREMENT INFORMATION



C_L Includes Load and Test Jig Capacitance.
S_1 = V_{CC} for t_{PZL} and t_{PLZ} Measurements.
S_1 = GND for t_{PZH} and t_{PHZ} Measurements.

Figure 3. Receiver 3-State Delay Test Circuit

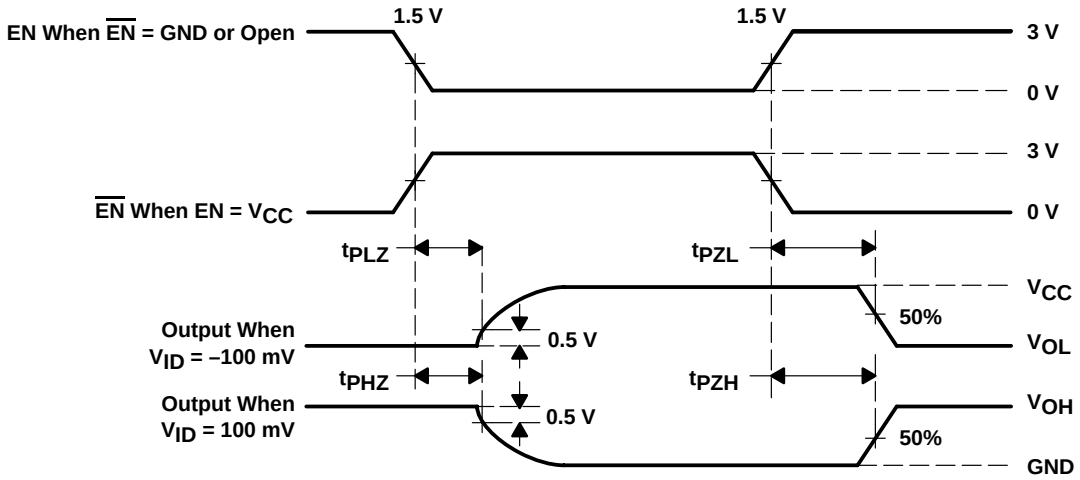


Figure 4. Receiver 3-State Delay Waveforms

TYPICAL CHARACTERISTICS

OUTPUT HIGH VOLTAGE vs POWER SUPPLY VOLTAGE

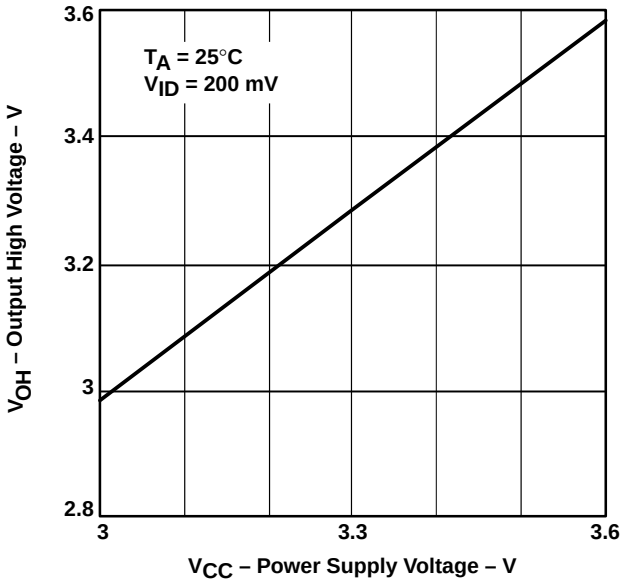


Figure 5

OUTPUT LOW VOLTAGE vs POWER SUPPLY VOLTAGE

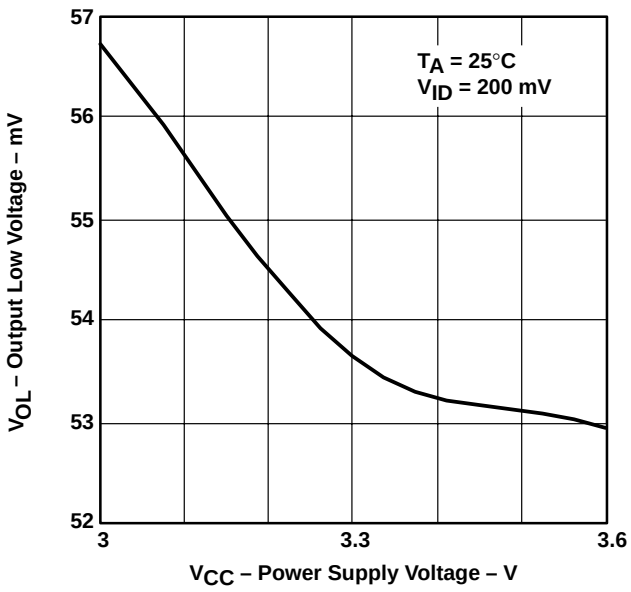


Figure 6

OUTPUT SHORT CIRCUIT CURRENT vs POWER SUPPLY VOLTAGE

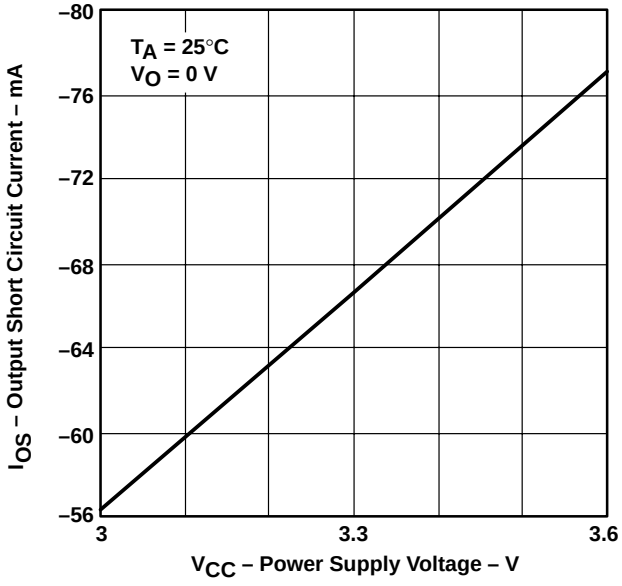


Figure 7

DIFFERENTIAL TRANSITION VOLTAGE vs POWER SUPPLY VOLTAGE

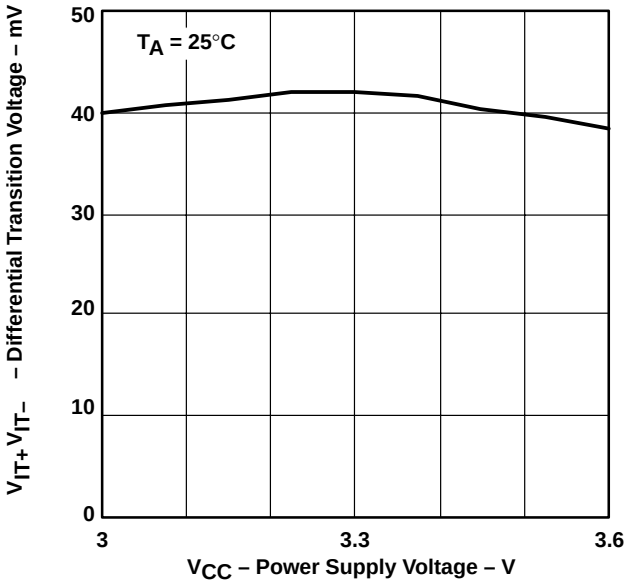


Figure 8

TYPICAL CHARACTERISTICS

DIFFERENTIAL PROPAGATION DELAY
vs
DIFFERENTIAL INPUT VOLTAGE

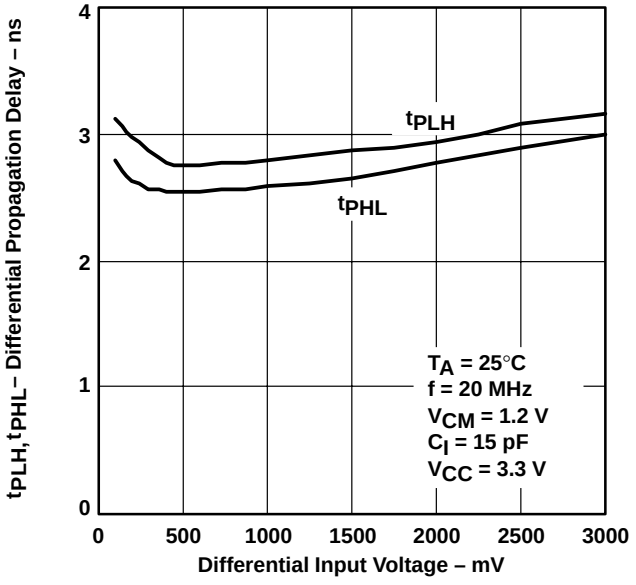


Figure 9

DIFFERENTIAL PROPAGATION DELAY
vs
COMMON-MODE VOLTAGE

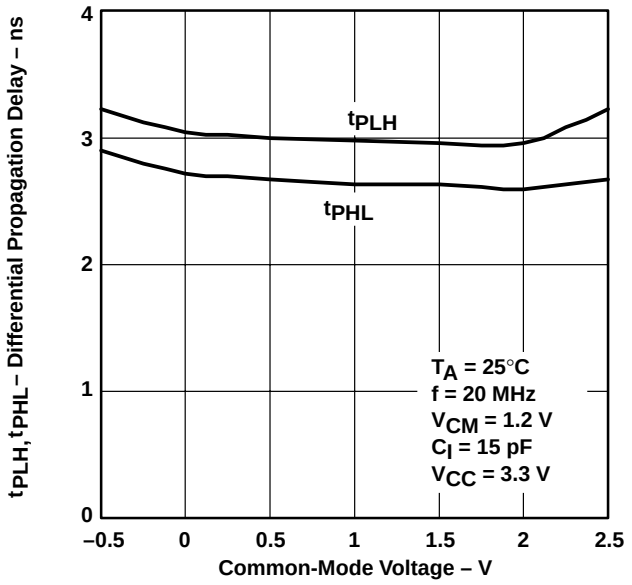


Figure 10

DATA TRANSFER RATE
vs
FREE-AIR TEMPERATURE

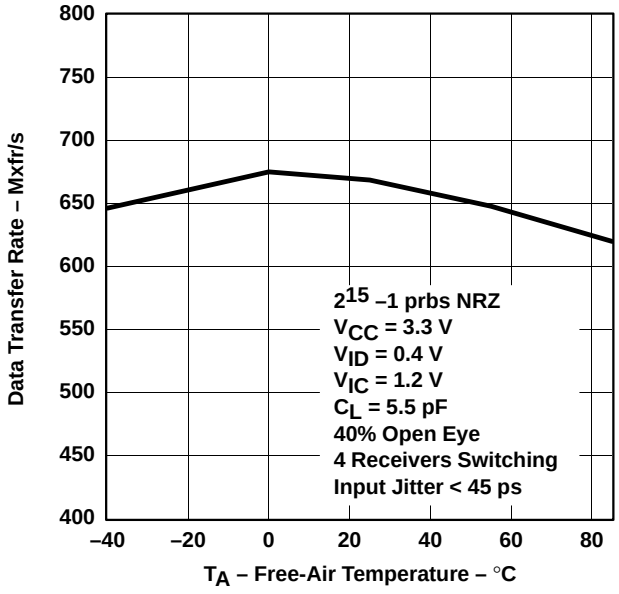


Figure 11

APPLICATION INFORMATION

fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near V_{CC} through 300-kΩ resistors as shown in Figure 10. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

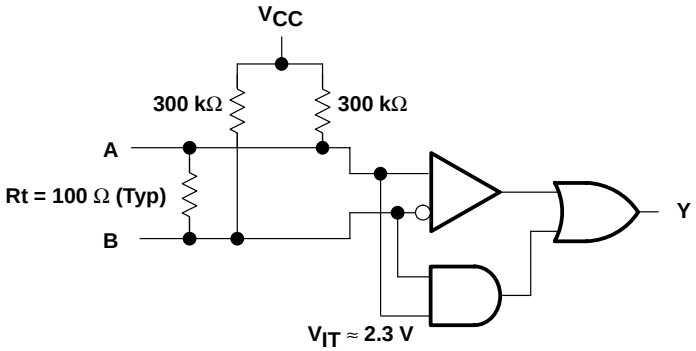


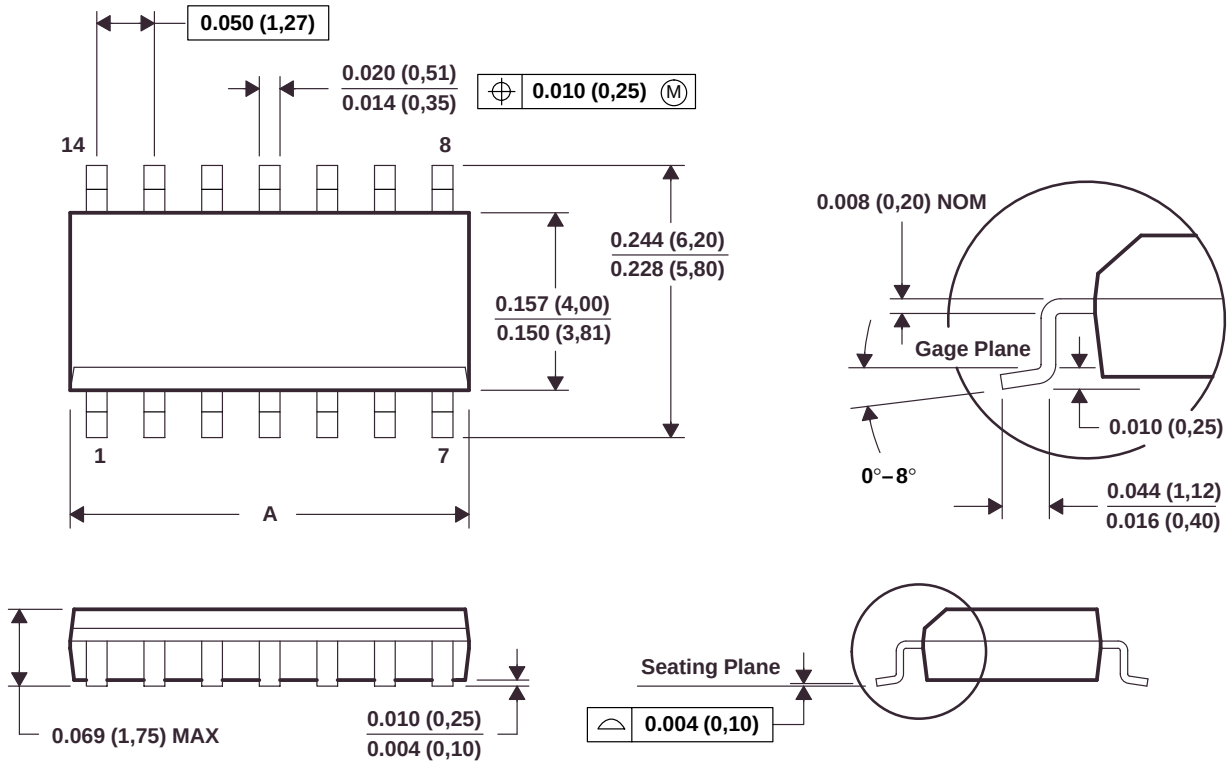
Figure 12. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

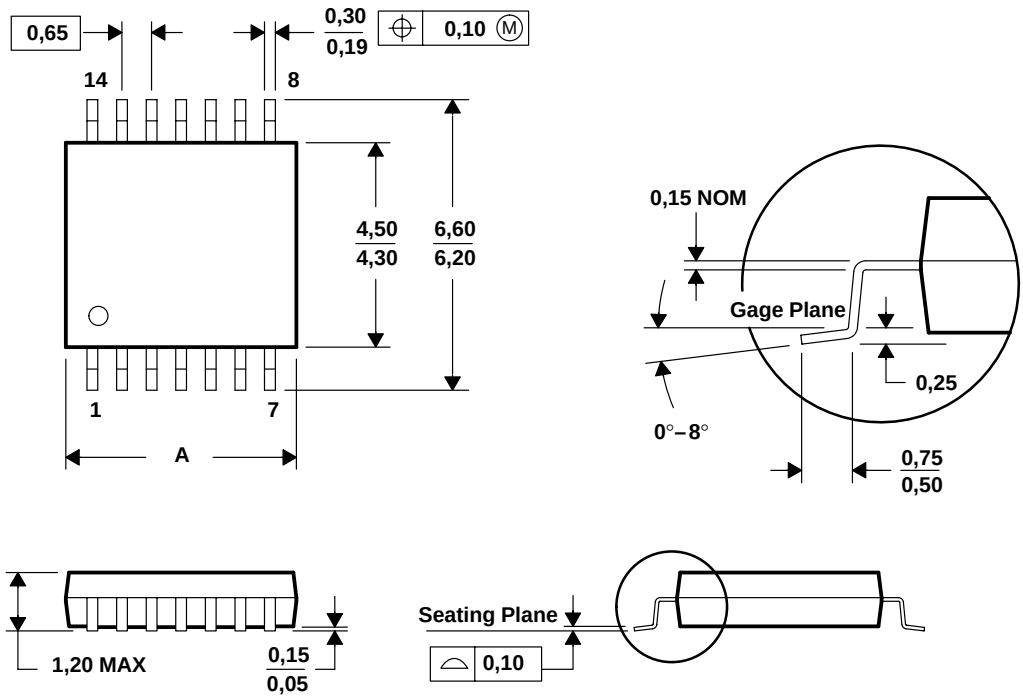
4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265