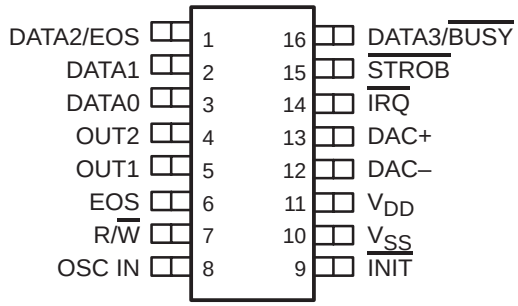
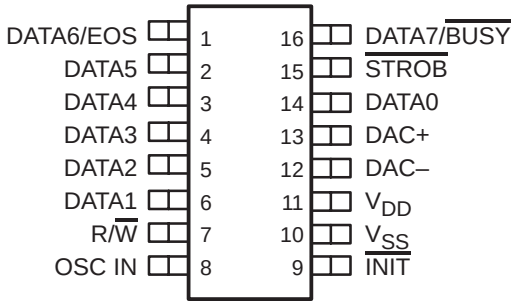
- **Slave Speech Synthesizers, LPC, MELP, CELP**
- **Two Channel FM Synthesis, PCM**
- **8-Bit Microprocessor With 61 instructions**
- **3.3V to 6.5V CMOS Technology for Low Power Dissipation**
- **Direct Speaker Drive Capability**
- **Internal Clock Generator That Requires No External Components**
- **Two Software-Selectable Clock Speeds**
- **10-kHz or 8-kHz Speech Sample Rate**

MSP53C391
N PACKAGE
(TOP VIEW)



MSP53C392
N PACKAGE
(TOP VIEW)



description

The MSP53C391 and MSP53C392 are catalog MSP50C3x codes which implements the functionality of a slave speech synthesizer. They communicate with a master microprocessor using two control lines (R/$\overline{W}$ and $\overline{STROBE}$) and either a 4-bit data bus (MSP53C391) or an 8-bit data bus (MSP53C392).

Either the MSP53C391 or the MSP53C392 can synthesize speech using several different compression algorithms; LPC, MELP, or CELP. They also can synthesize two-channel music using FM synthesis.

See the MSP50C3x User's Guide (literature number: SLOU006B) for more information about the MSP50C3x family.

Table 1. MSP53C39x Family

DEVICE	FEATURES
MSP53C391	4-bit data bus
MSP53C392	8-bit data bus

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.3 V to 8 V
Supply current, I_{DD} or I_{SS} (see Note 2) . . . . . 100 mA
Input voltage range, V_I (see Note 1) . . . . . –0.3 V to V_{DD} + 0.3 V
Output voltage range, V_O (see Note 1) . . . . . –0.3 V to V_{DD} + 0.3 V
Storage temperature range . . . . . –30°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground.
2. The total supply current includes the current out of all the I/O terminals and DAC terminals as well as the operating current of the device.

recommended operating conditions

			MAX	MAX	UNIT
V_{DD}	Supply voltage†		3.3	6.5	V
V_{IH}	High-level input voltage	V_{DD} = 3.3 V	2.5	3.3	V
		V_{DD} = 5 V	3.8	5	
		V_{DD} = 6 V	4.5	6	
V_{IL}	Low-level input voltage	V_{DD} = 3.3 V	0	0.65	V
		V_{DD} = 5 V	0	1	
		V_{DD} = 6 V	0	1.3	
T_A	Operating free-air temperature	Device functionality	0	70	°C
Rspeaker	Minimum speaker impedance	Direct speaker drive using 2 pin push-pull DAC option	32		Ω

† Unless otherwise noted, all voltages are with respect to V_{SS}.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{T+}	Positive-going threshold voltage (INIT)	V_{DD} = 3.5 V			2		V
		V_{DD} = 6 V			3.4		
V_{T-}	Negative-going threshold voltage (INIT)	V_{DD} = 3.5 V			1.6		V
		V_{DD} = 6 V			2.3		
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$) (INIT)	V_{DD} = 3.5 V			0.4		V
		V_{DD} = 6 V			1.1		
I_{lkg}	Input leakage current (except for OSC IN)					2	µA
$I_{standby}$	Standby current ($\overline{INIT}$ low, SETOFF)					10	µA
I_{DD}†	Supply current	V_{DD} = 3.3 V,	V_{OH} = 2.75 V		2.1		mA
		V_{DD} = 5 V,	V_{OH} = 4.5 V		3.1		
		V_{DD} = 6 V,	V_{OH} = 5.5 V		4.5		
I_{OH}	High-level output current (DATA0 – DATA7, OUT1, OUT2)	V_{DD} = 3.3 V,	V_{OH} = 2.75 V	–4	–12		mA
		V_{DD} = 5 V,	V_{OH} = 4.5 V	–5	–14		
		V_{DD} = 6 V,	V_{OH} = 5.5 V	–6	–15		
		V_{DD} = 3.3 V,	V_{OH} = 2.2 V	–8	–20		mA
		V_{DD} = 5 V,	V_{OH} = 3.33 V	–14	–40		
		V_{DD} = 6 V,	V_{OH} = 4 V	–20	–51		
I_{OL}	Low-level output current (DATA0 – DATA7, OUT1, OUT2)	V_{DD} = 3.3 V,	V_{OL} = 0.5 V	5	9		mA
		V_{DD} = 5 V,	V_{OL} = 0.5 V	5	9		
		V_{DD} = 6 V,	V_{OL} = 0.5 V	5	9		
		V_{DD} = 3.3 V,	V_{OL} = 1.1 V	10	19		mA
		V_{DD} = 5 V,	V_{OL} = 1.67 V	20	29		
		V_{DD} = 6 V,	V_{OL} = 2 V	25	35		
I_{OH}	High-level output current (DAC)	V_{DD} = 3.3 V,	V_{OH} = 2.75 V	–30	–50		mA
		V_{DD} = 5 V,	V_{OH} = 4.5 V	–35	–60		
		V_{DD} = 6 V,	V_{OH} = 5.5 V	–40	–65		
		V_{DD} = 3.3 V,	V_{OH} = 2.3 V	–50	–90		mA
		V_{DD} = 5 V,	V_{OH} = 4 V	–90	–140		
		V_{DD} = 6 V,	V_{OH} = 5 V	–100	–150		
I_{OL}	Low-level output current (DAC)	V_{DD} = 3.3 V,	V_{OL} = 0.5 V	50	80		mA
		V_{DD} = 5 V,	V_{OL} = 0.5 V	70	90		
		V_{DD} = 6 V,	V_{OL} = 0.5 V	80	110		
		V_{DD} = 3.3 V,	V_{OL} = 1 V	100	140		mA
		V_{DD} = 5 V,	V_{OL} = 1 V	140			
		V_{DD} = 6 V,	V_{OL} = 1 V	150			
$f_{osc(low)}$	Oscillator frequency‡	V_{DD} = 5 V, T_A = 25°C, Target frequency = 15.36 MHz		14.89	15.36	15.86	MHz
$f_{osc(high)}$	Oscillator frequency‡	V_{DD} = 5 V, T_A = 25°C, Target frequency = 19.2 MHz		18.62	19.2	19.7	MHz

† Operating current assumes all inputs are tied to either V_{SS} or V_{DD} with no input currents due to programmed pullup resistors. The DAC output and other outputs are open circuited.

‡ The frequency of the internal clock has a temperature coefficient of approximately –0.2 %/°C and a V_{DD} coefficient of approximately ±1%/V.

switching characteristics

PARAMETER		TEST CONDITIONS			MIN	NOM	MAX	UNIT
t_r	Rise time, DATA0 – DATA7, DAC	V_{DD} = 3.3 V,	C_L = 100 pF,	10% to 90%		50		ns
t_f	Fall time, DATA0– DATA7, DAC	V_{DD} = 3.3 V,	C_L = 100 pF,	10% to 90%		50		ns

timing requirements

		MIN	MAX	UNIT
Initialization				
t_{INIT}	$\overline{INIT}$ pulsed low while the MSP53C39x has power applied (see Figure 1)	1		µs
t_{SETUP}	Delay between rising edge of $\overline{INIT}$ and device initialization complete	5		ms
Writing (Slave Mode)				
$t_{su1(R/W)}$	Setup time, R/$\overline{W}$ low before $\overline{STROB}$ goes low (see Figure 2)	20		ns
$t_{su(d)}$	Setup time, data valid before $\overline{STROB}$ goes high (see Figure 2)	100		ns
$t_{h1(R/W)}$	Hold time, R/$\overline{W}$ low after $\overline{STROB}$ goes high (see Figure 2)	20		ns
$t_{h(d)}$	Hold time, data valid after $\overline{STROB}$ goes high (see Figure 2)	30		ns
t_w	Pulse duration, $\overline{STROB}$ low (see Figure 2)	100		ns
t_r	Rise time, $\overline{STROB}$ (see Figure 2)		50	ns
t_f	Fall time, $\overline{STROB}$ (see Figure 2)		50	ns
Reading (Slave Mode)				
$t_{su2(R/W)}$	Setup time, R/$\overline{W}$ before $\overline{STROB}$ goes low (see Figure 3)	20		ns
$t_{h2(R/W)}$	Hold time, R/$\overline{W}$ after $\overline{STROB}$ goes high (see Figure 3)	20		ns
t_{dis}	Output disable time, data valid after $\overline{STROB}$ goes high (see Figure 3)	0	30	ns
t_w	Pulse duration, $\overline{STROB}$ low (see Figure 3)	100		ns
t_r	Rise time, $\overline{STROB}$ (see Figure 3)		50	ns
t_f	Fall time, $\overline{STROB}$ (see Figure 3)		50	ns
t_d	Delay time for $\overline{STROB}$ low to data valid (see Figure 3)		50	ns

PARAMETER MEASUREMENT INFORMATION

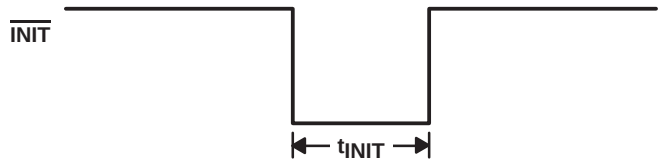


Figure 1. Initialization Timing Diagram

PARAMETER MEASUREMENT INFORMATION

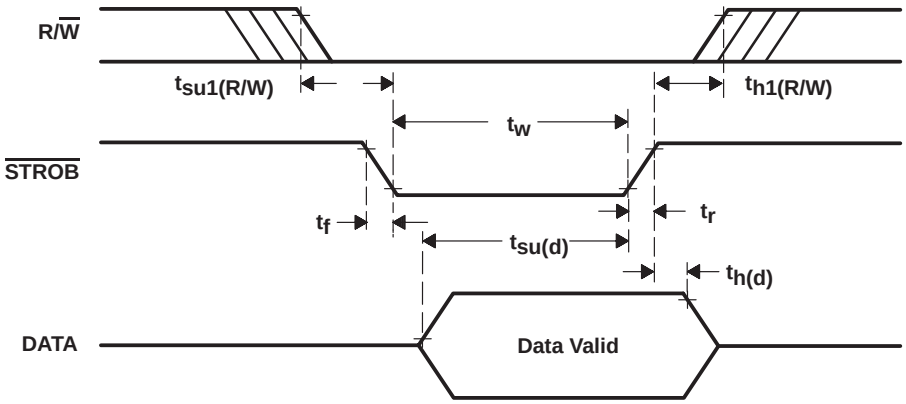


Figure 2. Write Timing Diagram (Slave Mode)

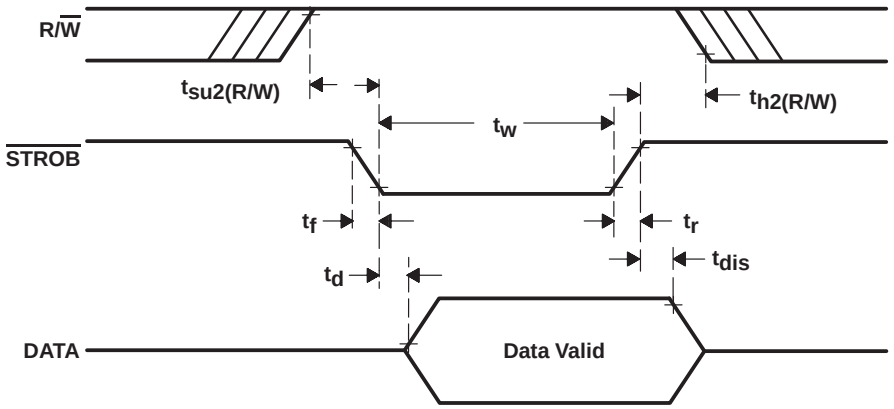


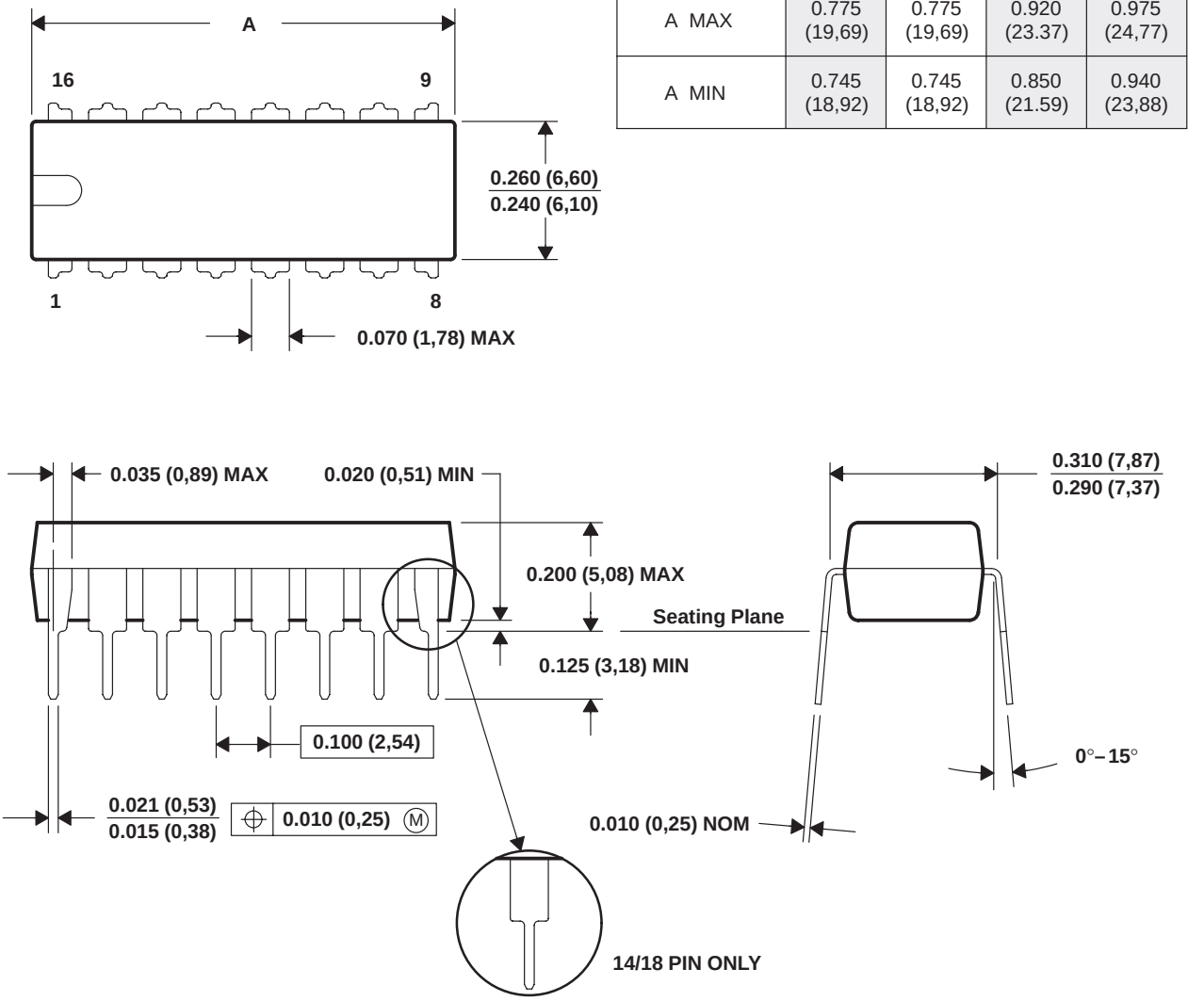
Figure 3. Read Timing Diagram (Slave Mode)

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.