LOW-DISTORTION HIGH-SPEED VOLTAGE FEEDBACK AMPLIFIER
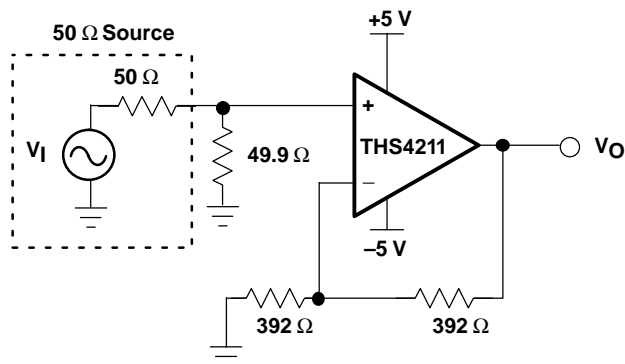
FEATURES

- **Unity Gain Stability**
- **Wide Bandwidth: 1 GHz**
- **High Slew Rate: 970 V/μs**
- **Low Distortion**
  - **–90 dBc THD at 30 MHz**
- **High Output Drive, I_O = 200 mA**
- **Excellent Video Performance**
  - **130 MHz Bandwidth (0.1 dB, G = 2)**
  - **0.007% Differential Gain**
  - **0.003° Differential Phase**
- **Supply Voltages**
  - **+5 V, $\pm$5 V, +12 V, +15 V**
- **Power Down Functionality (THS4215)**
- **Evaluation Module Available**

DESCRIPTION

The THS4211 and THS4215 are high slew rate, unity gain stable voltage feedback amplifiers designed to run from supply voltages as low as 5 V and as high as 15 V. The THS4215 offers the same performance as the THS4211 with the addition of power-down capability. The combination of high slew rate, wide bandwidth, low distortion, and unity gain stability make the THS4211 and THS4215 high performance devices across multiple ac specifications.
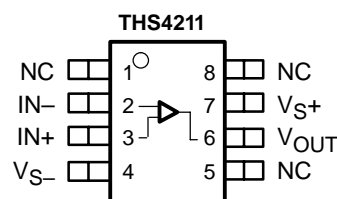
APPLICATIONS

- **High Linearity ADC Preamplifier**
- **Differential to Single-Ended Conversion**
- **DAC Output Buffer**
- **Active Filtering**
- **Video Applications**

THS4211

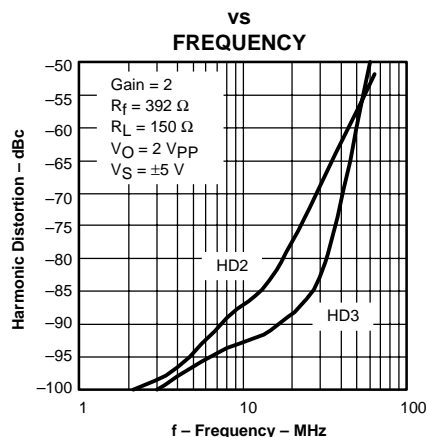|			
NC	1	8	NC
IN–	2	7	V_S+
IN+	3	6	V_{OUT}
V_S–	4	5	NC

Designers using the THS4211 are rewarded with higher dynamic range over a wider frequency band without the stability concerns of decompensated amplifiers. The devices are available in SOIC, MSOP with PowerPAD™, and leadless MSOP with PowerPAD™ packages.

RELATED DEVICES

DEVICE	DESCRIPTION
THS4271	1.4 GHz voltage feedback amplifier
THS4503	Wideband fully differential amplifier
THS3202	Dual, wideband current feedback amplifier

Low-Distortion, Wideband Application Circuit

NOTE: Power supply decoupling capacitors not shown

HARMONIC DISTORTION vs FREQUENCY

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted

		UNIT
Supply voltage, V_S		16.5 V
Input voltage, V_I		$\pm V_S$
Output current, I_O [1]		100 mA
Continuous power dissipation	See Dissipation Rating Table	
Maximum junction temperature, T_J		150°C
Operating free-air temperature range, T_A		−40°C to 85°C
Storage temperature range, T_{stg}		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C

[1] The THS4211/5 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heat sink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical briefs SLMA002 and SLMA004 for more information about utilizing the PowerPAD thermally enhanced package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING	
			$T_A \leq 25°C$	$T_A = 85°C$
D (8 pin)[1]	38.3	176	710 mW	370 mW
DGN (8 pin)[2]	4.7	58.4	2.14 W	1.11 W
DRB (8 pin)[2]	5	45.8	2.73 W	1.42 W

[1] This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC Proposed High-K test PCB, θ_{JA} is 95°C/W with power rating at $T_A = 25°C$ of 1.32 W.

[2] This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 in. x 3 in. PCB. For further information, refer to *Application Information* section of this data sheet.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, (V_{S+} and V_{S-})	Dual supply	±2.5	±7.5	V
	Single supply	5	15	
Input common-mode voltage range		V_{S-} +1.2	V_{S+} −1.2	V

PACKAGING/ORDERING INFORMATION

TEMPERATURE	ORDERABLE PACKAGE AND NUMBER				
	PLASTIC SMALL OUTLINE[1] (D)	LEADLESS MSOP 8[1]		PLASTIC MSOP[1]	
		(DRB)	PACKAGE MARKING	(DGN)	PACKAGE MARKING
	THS4211D	THS4211DRB	BET	THS4211DGN	BFN
	THS4215D	THS4215DRB	BEU	THS4215DGN	BFQ

[1] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., THS4211DGNR)

PIN ASSIGNMENTS

(TOP VIEW)   D, DRB, AND DGN

THS4211

NC	1	8 NC
IN−	2	7 V_{S+}
IN+	3	6 V_{OUT}
V_{S-}	4	5 NC

(TOP VIEW)   D, DRB, AND DGN

THS4215

REF	1	8 $\overline{PD}$
IN−	2	7 V_{S+}
IN+	3	6 V_{OUT}
V_{S-}	4	5 NC

ELECTRICAL CHARACTERISTICS $V_S = \pm 5$ V

$R_F = 392\ \Omega$, $R_L = 499\ \Omega$, G = +1, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				MIN/ TYP/ MAX
		25°C	25°C	0°C TO 70°C	−40°C TO 85°C	UNITS	
AC PERFORMANCE							
Small signal bandwidth	G = 1, $P_{OUT} = -7$ dBm	1				GHz	Typ
	G = −1, $P_{OUT} = -16$ dBm	325				MHz	Typ
	G = 2, $P_{OUT} = -16$ dBm	325				MHz	Typ
	G = 5, $P_{OUT} = -16$ dBm	70				MHz	Typ
	G = 10, $P_{OUT} = -16$ dBm	35				MHz	Typ
0.1 dB flat bandwidth	G = 1, $P_{OUT} = -7$ dBm	70				MHz	Typ
Gain bandwidth product	G > 10 , f = 1 MHz	350				MHz	Typ
Full-power bandwidth	G = −1, $V_O = 2\ V_p$	77				MHz	Typ
Slew rate	G = 1, $V_O = 2$ V Step	970				V/μs	Typ
	G = −1, $V_O = 2$ V Step	850				V/μs	Typ
Settling time to 0.1%	G = −1, $V_O = 4$ V Step	22				ns	Typ
Settling time to 0.01%	G = −1, $V_O = 4$ V Step	55				ns	Typ
Harmonic distortion	G = 1, $V_O = 1\ V_{PP}$, f = 30 MHz						
Second harmonic distortion	$R_L = 150\ \Omega$	−78				dBc	Typ
	$R_L = 499\ \Omega$	−90				dBc	Typ
Third harmonic distortion	$R_L = 150\ \Omega$	−100				dBc	Typ
	$R_L = 499\ \Omega$	−100				dBc	Typ
Harmonic distortion	G = 2, $V_O = 2\ V_{PP}$, f = 30 MHz						
Second harmonic distortion	$R_L = 150\ \Omega$	−68				dBc	Typ
	$R_L = 499\ \Omega$	−70				dBc	Typ
Third harmonic distortion	$R_L = 150\ \Omega$	−80				dBc	Typ
	$R_L = 499\ \Omega$	−82				dBc	Typ
Third order intermodulation (IMD_3)	G = 2, $V_O = 2\ V_{PP}$, $R_L = 150\ \Omega$, f = 70 MHz	−53				dBc	Typ
Third order output intercept (OIP_3)	G = 2, $V_O = 2\ V_{PP}$, $R_L = 150\ \Omega$, f = 70 MHz	32				dBm	Typ
Differential gain (NTSC, PAL)	G = 2, $R_L = 150\ \Omega$	0.007				%	Typ
Differential phase (NTSC, PAL)	G = 2, $R_L = 150\ \Omega$	0.003				°	Typ
Input voltage noise	f = 1 MHz	7				nV/√Hz	Typ
Input current noise	f = 1 MHz	4				pA√Hz	Typ
DC PERFORMANCE							
Open-loop voltage gain (A_{OL})	$V_O = \pm 0.3$ V, $R_L = 499\ \Omega$	70	65	62	60	dB	Min
Input offset voltage	$V_{CM} = 0$ V	3	12	14	14	mV	Max
Average offset voltage drift	$V_{CM} = 0$ V			±40	±40	μV/°C	Typ
Input bias current	$V_{CM} = 0$ V	7	15	18	20	μA	Max
Average bias current drift	$V_{CM} = 0$ V			±10	±10	nA/°C	Typ
Input offset current	$V_{CM} = 0$ V	0.3	6	7	8	μA	Max
Average offset current drift	$V_{CM} = 0$ V			±10	±10	nA/°C	Typ

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ELECTRICAL CHARACTERISTICS $V_S = \pm5$ V (continued)

$R_F = 392\ \Omega$, $R_L = 499\ \Omega$, G = +1, unless otherwise noted.

PARAMETER	TEST CONDITIONS		TYP 25°C	OVER TEMPERATURE			UNITS	MIN/ TYP/ MAX
				25°C	0°C to 70°C	−40°C to 85°C		
INPUT CHARACTERISTICS								
Common-mode input range			±4	±3.8	±3.7	±3.6	V	Min
Common-mode rejection ratio	$V_{CM} = \pm 1$ V		56	52	50	48	dB	Min
Input resistance	Common-mode		4				MΩ	Typ
Input capacitance	Common-mode / differential		0.3 / 0.2				pF	Typ
OUTPUT CHARACTERISTICS								
Output voltage swing			±4.0	±3.8	±3.7	±3.6	V	Min
Output current (sourcing)	$R_L = 10\ \Omega$		220	200	190	180	mA	Min
Output current (sinking)	$R_L = 10\ \Omega$		170	140	130	120	mA	Min
Output impedance	f = 1 MHz		0.3				Ω	Typ
POWER SUPPLY								
Specified operating voltage			±5	±7.5	±7.5	±7.5	V	Max
Maximum quiescent current			19	22	23	24	mA	Max
Minimum quiescent current			19	16	15	14	mA	Min
Power supply rejection (+PSRR)	$V_{S+} = 5.5$ V to 4.5 V, $V_{S−} = 5$ V		64	58	54	54	dB	Min
Power supply rejection (−PSRR)	$V_{S+} = 5$ V, $V_{S−} = −5.5$ V to −4.5 V		65	60	56	56	dB	Min
POWER-DOWN CHARACTERISTICS (THS4215 ONLY)								
Power-down voltage level	REF = 0 V, or $V_{S−}$	Enable		REF+1.8			V	Min
		Power-down		REF+1			V	Max
	REF = V_{S+} or Floating	Enable		REF−1			V	Min
		Power-down		REF−1.5			V	Max
Power-down quiescent current	PD = Ref +1.0 V, Ref = 0 V		650	850	900	1000	μA	Max
	PD = Ref −1.5 V, Ref = 5 V		450	650	800	900	μA	Max
Turnon time delay($t_{(ON)}$)	50% of final supply current value		4				μs	Typ
Turnoff time delay ($t_{(Off)}$)	50% of final supply current value		3				μs	Typ
Input impedance			4				GΩ	Typ
Output impedance	f = 1 MHz		250				kΩ	Typ

ELECTRICAL CHARACTERISTICS V_S = 5 V

R_F = 392 Ω, R_L = 499 Ω, G = +1, unless otherwise noted

PARAMETER	TEST CONDITIONS	TYP 25°C	OVER TEMPERATURE			UNITS	MIN/ TYP/ MAX
			25°C	0°C to 70°C	−40°C to 85°C		
AC PERFORMANCE							
Small signal bandwidth	G = 1, P_{OUT} = −7 dBm	980				MHz	Typ
	G = −1, P_{OUT} = −16 dBm	300				MHz	Typ
	G = 2, P_{OUT} = −16 dBm	300				MHz	Typ
	G = 5, P_{OUT} = −16 dBm	65				MHz	Typ
	G = 10, P_{OUT} = −16 dBm	30				MHz	Typ
0.1 dB flat bandwidth	G = 1, P_{OUT} = −7 dBm	90				MHz	Typ
Gain bandwidth product	G > 10, f = 1 MHz	300				MHz	Typ
Full-power bandwidth	G = −1, V_O = 2 V_p	64				MHz	Typ
Slew rate	G = 1, V_O = 2 V Step	800				V/μs	Typ
	G = −1, V_O = 2 V Step	750				V/μs	Typ
Settling time to 0.1%	G = −1, V_O = 2 V Step	22				ns	Typ
Settling time to 0.01%	G = −1, V_O = 2 V Step	84				ns	Typ
Harmonic distortion	G = 1, V_O = 1 V_{PP}, f = 30 MHz						
Second harmonic distortion	R_L = 150 Ω	−60				dBc	Typ
	R_L = 499 Ω	−60				dBc	Typ
Third harmonic distortion	R_L = 150 Ω	−68				dBc	Typ
	R_L = 499 Ω	−68				dBc	Typ
Third order intermodulation (IMD_3)	G = 1, V_O = 1 V_{PP} , R_L = 150 Ω, f = 70 MHz	−70				dBc	Typ
Third order output intercept (OIP_3)	G = 1, V_O = 1 V_{PP}, R_L = 150 Ω, f = 70 MHz	34				dBm	Typ
Input-voltage noise	f = 1 MHz	7				nV/√Hz	Typ
Input-current noise	f = 10 MHz	4				pA/√Hz	Typ
DC PERFORMANCE							
Open-loop voltage gain (A_{OL})	V_O = ± 0.3 V, R_L = 499 Ω	68	63	60	60	dB	Min
Input offset voltage	V_{CM} = V_S/2	3	12	14	14	mV	Max
Average offset voltage drift	V_{CM} = V_S/2			±40	±40	μV/°C	Typ
Input bias current	V_{CM} = V_S/2	7	15	17	18	μA	Max
Average bias current drift	V_{CM} = V_S/2			±10	±10	nA/°C	Typ
Input offset current	V_{CM} = V_S/2	0.3	6	7	8	μA	Max
Average offset current drift	V_{CM} = V_S/2			±10	±10	nA/°C	Typ
INPUT CHARACTERISTICS							
Common-mode input range		1 / 4	1.2 / 3.8	1.3 / 3.7	1.4 / 3.6	V	Min
Common-mode rejection ratio	V_{CM} = ± 0.5 V, V_O = 2.5 V	54	50	48	45	dB	Min
Input resistance	Common-mode	4				MΩ	Typ
Input capacitance	Common-mode / differential	0.3 / 0.2				pF	Typ
OUTPUT CHARACTERISTICS							
Output voltage swing		1 / 4	1.2 / 3.8	1.3 / 3.7	1.4 / 3.6	V	Min
Output current (sourcing)	R_L = 10 Ω	230	210	190	180	mA	Min
Output current (sinking)	R_L = 10 Ω	150	120	100	90	mA	Min
Output impedance	f = 1 MHz	0.3				Ω	Typ

ELECTRICAL CHARACTERISTICS V_S = 5 V (continued)

R_F = 392 Ω, R_L = 499 Ω, G = +1, unless otherwise noted

PARAMETER	TEST CONDITIONS		TYP	OVER TEMPERATURE			UNITS	MIN/
			25°C	25°C	0°C to 70°C	−40°C to 85°C		TYP/ MAX
POWER SUPPLY								
Specified operating voltage			5	15	15	15	V	Max
Maximum quiescent current			19	22	23	24	mA	Max
Minimum quiescent current			19	16	15	14	mA	Min
Power supply rejection (+PSRR)	V_{S+} = 5.5 V to 4.5 V, V_{S-} = 0 V		63	58	54	54	dB	Min
Power supply rejection (−PSRR)	V_{S+} = 5 V, V_{S-} = −0.5 V to 0.5 V		65	60	56	56	dB	Min
POWER-DOWN CHARACTERISTICS (THS4215 ONLY)								
Power-down voltage level	REF = 0 V, or V_{S-}	Enable		REF+1.8			V	Min
		Power down		REF+1			V	Max
	REF = V_{S+} or floating	Enable		REF−1			V	Min
		Power down		REF−1.5			V	Max
Power-down quiescent current	PD = Ref +1.0 V, Ref = 0 V		450	650	750	850	µA	Max
Power-down quiescent current	PD = Ref −1.5 V, Ref = 5 V		400	650	750	850	µA	Max
Turnon-time delay ($t_{(ON)}$)	50% of final value		4				µs	Typ
Turnoff-time delay ($t_{(Off)}$)	50% of final value		3				µns	Typ
Input impedance			6				GΩ	Typ
Output impedance	f = 1 MHz		75				kΩ	Typ

TYPICAL CHARACTERISTICS

Table of Graphs (±5 V)

	FIGURE
Small-signal unity gain frequency response	1
Small-signal frequency response	2
0.1 dB gain flatness frequency response	3
Large-signal frequency response	4
Slew rate vs Output voltage	5
Harmonic distortion vs Frequency	6, 7, 8, 9
Harmonic distortion vs Output voltage swing	10, 11, 12, 13
Third order intermodulation distortion vs Frequency	14, 16
Third order output intercept point vs Frequency	15, 17
Voltage and current noise vs Frequency	18
Differential gain vs Number of loads	19
Differential phase vs Number of loads	20
Settling time	21
Quiescent current vs supply voltage	22
Output voltage vs Load resistance	23
Frequency response vs Capacitive load	24
Open-loop gain and phase vs Frequency	25
Open-loop gain vs Case temperature	26
Rejection ratios vs Frequency	27
Rejection ratios vs Case temperature	28
Common-mode rejection ratio vs Input common-mode range	29
Input offset voltage vs Case temperature	30
Input bias and offset current vs Case temperature	31
Small signal transient response	32
Large signal transient response	33
Overdrive recovery	34
Closed-loop output impedance vs Frequency	35
Power-down quiescent current vs Supply voltage	36
Power-down output impedance vs Frequency	37
Turnon and turnoff delay times	38

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TYPICAL CHARACTERISTICS

Table of Graphs (5 V)

	FIGURE
Small-signal unity gain frequency response	39
Small-signal frequency response	40
0.1 dB gain flatness frequency response	41
Large signal frequency response	42
Slew rate vs Output voltage	43
Harmonic distortion vs Frequency	44, 45, 46, 47
Harmonic distortion vs Output voltage swing	48, 49, 50, 51
Third order intermodulation distortion vs Frequency	52, 54
Third order intercept point vs Frequency	53, 55
Voltage and current noise vs Frequency	56
Settling time	57
Quiescent current vs Supply voltage	58
Output voltage vs Load resistance	59
Frequency response vs Capacitive load	60
Open-loop gain and phase vs Frequency	61
Open-loop gain vs Case temperature	62
Rejection ratios vs Frequency	63
Rejection ratios vs Case temperature	64
Common-mode rejection ratio vs Input common-mode range	65
Input offset voltage vs Case temperature	66
Input bias and offset current vs Case temperature	67
Small signal transient response	68
Large signal transient response	69
Overdrive recovery	70
Closed-loop output impedance vs Frequency	71
Power-down quiescent current vs Supply voltage	72
Power-down output impedance vs Frequency	73
Turnon and turnoff delay times	74

TYPICAL CHARACTERISTICS (±5 V GRAPHS)

SMALL SIGNAL UNITY GAIN FREQUENCY RESPONSE

Figure 1

SMALL SIGNAL FREQUENCY RESPONSE

Figure 2

0.1 dB GAIN FLATNESS FREQUENCY RESPONSE

Figure 3

LARGE SIGNAL FREQUENCY RESPONSE

Figure 4

SLEW RATE vs OUTPUT VOLTAGE

Figure 5

HARMONIC DISTORTION vs FREQUENCY

Figure 6

HARMONIC DISTORTION vs FREQUENCY

Figure 7

HARMONIC DISTORTION vs FREQUENCY

Figure 8

HARMONIC DISTORTION vs FREQUENCY

Figure 9

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HARMONIC DISTORTION
vs
OUTPUT VOLTAGE SWING

Gain = 1
f = 8 MHz
$V_S = \pm5$ V

HD3, $R_L = 150\Omega$
HD3, $R_L = 499\Omega$
HD2, $R_L = 150\Omega$
HD2, $R_L = 499\Omega$

Harmonic Distortion – dBc
V_O – Output Voltage Swing – $\pm$V

Figure 10

HARMONIC DISTORTION
vs
OUTPUT VOLTAGE SWING

Gain = 1
f = 32 MHz
$V_S = \pm5$ V

HD3, $R_L = 150\Omega$
HD2, $R_L = 499\Omega$
HD2, $R_L = 150\Omega$
HD3, $R_L = 499\Omega$

Harmonic Distortion – dBc
V_O – Output Voltage Swing – $\pm$V

Figure 11

HARMONIC DISTORTION
vs
OUTPUT VOLTAGE SWING

Gain = 2
$R_f = 249\ \Omega$
f = 8 MHz
$V_S = \pm5$ V

HD2, $R_L = 499\Omega$
HD3, $R_L = 150\Omega$
HD3, $R_L = 499\Omega$
HD2, $R_L = 150\Omega$

Harmonic Distortion – dBc
V_O – Output Voltage Swing – $\pm$V

Figure 12

HARMONIC DISTORTION
vs
OUTPUT VOLTAGE SWING

Gain = 2
$R_f = 249\ \Omega$
f = 32 MHz
$V_S = \pm5$ V

HD3, $R_L = 150\Omega$
HD3, $R_L = 499\Omega$
HD2, $R_L = 499\Omega$
HD2, $R_L = 150\Omega$

Harmonic Distortion – dBc
V_O – Output Voltage Swing – $\pm$V

Figure 13

THIRD ORDER INTERMODULATION
DISTORTION
vs
FREQUENCY

Gain = 1
$R_L = 150\ \Omega$
$V_S = \pm5$ V
200 kHz Tone Spacing

$V_O = 2\ V_{PP}$
$V_O = 1\ V_{PP}$

Third-Order Intermodulation Distortion – dBc
f – Frequency – MHz

Figure 14

THIRD ORDER OUTPUT INTERCEPT
POINT
vs
FREQUENCY

Gain = 1
$R_L = 150\ \Omega$
$V_S = \pm5$ V
200 kHz Tone Spacing

$V_O = 1\ V_{PP}$
$V_O = 2\ V_{PP}$

Third-Order Output Intercept Point – dBm
f – Frequency – MHz

Figure 15

THIRD ORDER INTERMODULATION
DISTORTION
vs
FREQUENCY

Gain = 2
$R_L = 150\ \Omega$
$V_S = \pm5$ V
200 kHz Tone Spacing

$V_O = 2\ V_{PP}$
$V_O = 1\ V_{PP}$

Third-Order Intermodulation Distortion – dBc
f – Frequency – MHz

Figure 16

THIRD ORDER OUTPUT INTERCEPT
POINT
vs
FREQUENCY

Gain = 2
$R_L = 150\ \Omega$
$V_S = \pm5$ V
200 kHz Tone Spacing

$V_O = 1\ V_{PP}$
$V_O = 2\ V_{PP}$

Third-Order Output Intercept Point – dBm
f – Frequency – MHz

Figure 17

VOLTAGE AND CURRENT NOISE
vs
FREQUENCY

V_n
I_n

V_n – Voltage Noise – nV/$\sqrt{Hz}$
I_n – Current Noise – pA/$\sqrt{Hz}$
f – Frequency – Hz

Figure 18

DIFFERENTIAL GAIN
vs
NUMBER OF LOADS

Gain = 2
R_f = 392 Ω
V_S = ±5 V
40 IRE – NTSC and Pal
Worst Case ±100 IRE Ramp

PAL

NTSC

Figure 19

DIFFERENTIAL PHASE
vs
NUMBER OF LOADS

Gain = 2
R_f = 392 Ω
V_S = ±5 V
40 IRE – NTSC and Pal
Worst Case ±100 IRE Ramp

PAL

NTSC

Figure 20

SETTLING TIME

Rising Edge

Gain = –1
R_L = 499 Ω
R_f = 392 Ω
f= 1 MHz
V_S = ±5 V

Falling Edge

Figure 21

QUIESCENT CURRENT
vs
SUPPLY VOLTAGE

T_A = 85°C

T_A = 25°C

T_A = –40°C

Figure 22

OUTPUT VOLTAGE
vs
LOAD RESISTANCE

T_A = –40 to 85°C

Figure 23

FREQUENCY RESPONSE
vs
CAPACITIVE LOAD

$R_{(ISO)}$ = 10 Ω
C_L = 100 pF

V_S =±5 V

$R_{(ISO)}$ = 15 Ω
C_L = 50 pF

$R_{(ISO)}$ = 25 Ω
C_L = 10 pF

Figure 24

OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY

V_S = ±5 V

Figure 25

OPEN-LOOP GAIN
vs
CASE TEMPERATURE

T_A = 85°C

T_A = 25°C

T_A = –40°C

Figure 26

REJECTION RATIOS
vs
FREQUENCY

V_S = ±5 V

PSRR–

CMRR

PSRR+

Figure 27

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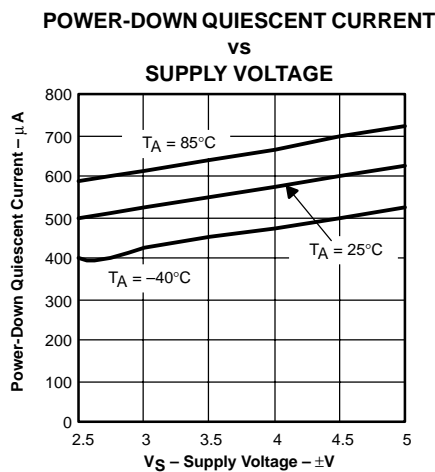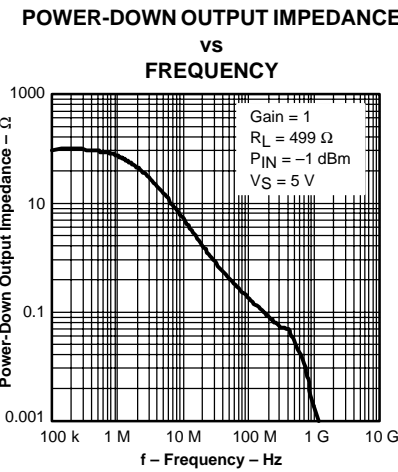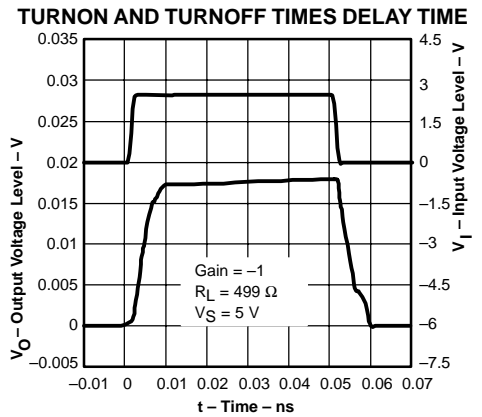**Figure 74**

APPLICATION INFORMATION

HIGH-SPEED OPERATIONAL AMPLIFIERS

The THS4211 and the THS4215 operational amplifiers set new performance levels, combining low distortion, high slew rates, low noise, and a unity-gain bandwidth in excess of 1 GHz. To achieve the full performance of the amplifier, careful attention must be paid to printed-circuit board layout and component selection.

The THS4215 provides a power-down mode, providing the ability to save power when the amplifier is inactive. A reference pin is provided to allow the user the flexibility to control the threshold levels of the power-down control pin.

Applications Section Contents

- Wideband, Noninverting Operation
- Wideband, Inverting Gain Operation
- Single Supply Operation
- Saving Power With Power-Down Functionality and Setting Threshold Levels With the Reference Pin
- Power Supply Decoupling Techniques and Recommendations
- Using the THS4211 as a DAC Output Buffer
- Driving an ADC With the THS4211
- Active Filtering With the THS4211
- Building a Low-Noise Receiver With the THS4211
- Linearity: Definitions, Terminology, Circuit Techniques and Design Tradeoffs
- An Abbreviated Analysis of Noise in Amplifiers
- Driving Capacitive Loads
- Printed-Circuit Board Layout Techniques for Optimal Performance
- Power Dissipation and Thermal Considerations
- Performance vs Package Options
- Evaluation Fixtures, Spice Models, and Applications Support
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WIDEBAND, NONINVERTING OPERATION

The THS4211 and the THS4215 are unity gain stable 1-GHz voltage feedback operational amplifiers, with and without power-down capability, designed to operate from a single 5-V to 15-V power supply.

Figure 75 is the noninverting gain configuration of 2 V/V used to demonstrate the typical performance curves. Most of the curves were characterized using signal sources with

50-Ω source impedance, and with measurement equipment presenting a 50-Ω load impedance. In Figure 75, the 49.9-Ω shunt resistor at the V_{IN} terminal matches the source impedance of the test generator. The total 499-Ω load at the output, combined with the 784-Ω total feedback network load, presents the THS4211 and THS4215 with an effective output load of 305 Ω for the circuit of Figure 75.

Voltage feedback amplifiers, unlike current feedback designs, can use a wide range of resistors values to set their gain with minimal impact on their stability and frequency response. Larger-valued resistors decrease the loading effect of the feedback network on the output of the amplifier, but this enhancement comes at the expense of additional noise and potentially lower bandwidth. Feedback resistor values between 392 Ω and 1 kΩ are recommended for most situations.
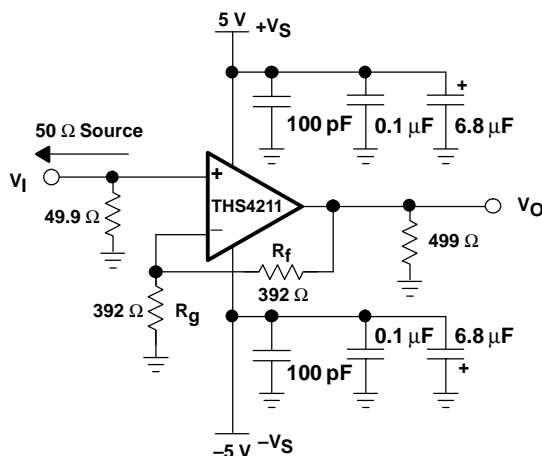

Figure 75. Wideband, Noninverting Gain Configuration

WIDEBAND, INVERTING GAIN OPERATION

Since the THS4211 and THS4215 are general-purpose, wideband voltage-feedback amplifiers, several familiar operational amplifier applications circuits are available to the designer. Figure 76 shows a typical inverting configuration where the input and output impedances and noise gain from Figure 75 are retained in an inverting circuit configuration. Inverting operation is one of the more common requirements and offers several performance benefits. The inverting configuration shows improved slew rates and distortion due to the pseudo-static voltage maintained on the inverting input.
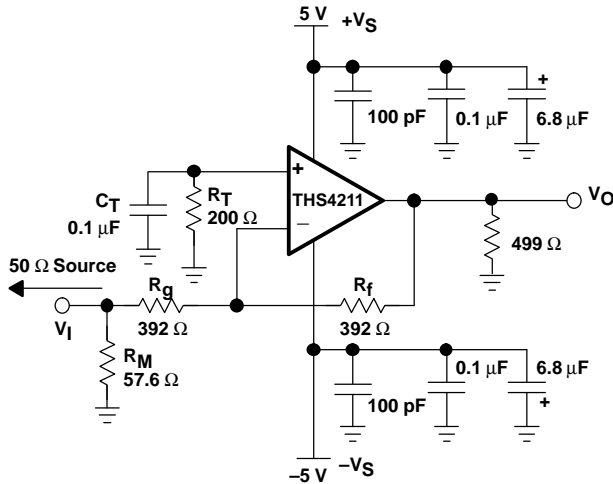
Figure 76. Wideband, Inverting Gain Configuration

In the inverting configuration, some key design considerations must be noted. One is that the gain resistor (R_g) becomes part of the signal channel input impedance. If the input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PC board trace, or other transmission line conductors), R_g may be set equal to the required termination value and R_f adjusted to give the desired gain. However, care must be taken when dealing with low inverting gains, as the resultant feedback resistor value can present a significant load to the amplifier output. For an inverting gain of 2, setting R_g to 49.9 Ω for input matching eliminates the need for R_M but requires a 100-Ω feedback resistor. This has an advantage of the noise gain becoming equal to 2 for a 50-Ω source impedance—the same as the noninverting circuit in Figure 75. However, the amplifier output now sees the 100-Ω feedback resistor in parallel with the external load. To eliminate this excessive loading, it is preferable to increase both R_g and R_f, values, as shown in Figure 76, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_g and R_M.

The next major consideration is that the signal source impedance becomes part of the noise gain equation and hence influences the bandwidth. For example, the R_M value combines in parallel with the external 50-Ω source impedance (at high frequencies), yielding an effective source impedance of 50 Ω || 57.6 Ω = 26.8 Ω. This impedance is then added in series with R_g for calculating the noise gain. The result is 1.9 for Figure 76, as opposed to the 1.8 if R_M is eliminated. The bandwidth is lower for the gain of –2 circuit, Figure 76, (NG=+1.9) than for the gain of +2 circuit in Figure 75.

The last major consideration in inverting amplifier design is setting the bias current cancellation resistor on the noninverting input. If the resistance is set equal to the total dc resistance looking out of the inverting terminal, the output dc error, due to the input bias currents, is reduced to (input offset current) multiplied by R_f in Figure 76, the dc source impedance looking out of the inverting terminal is $392\,\Omega\,||\,(392\,\Omega + 26.8\,\Omega) = 200\,\Omega$. To reduce the additional high-frequency noise introduced by the resistor at the noninverting input, and power-supply feedback, R_T is bypassed with a capacitor to ground.

SINGLE SUPPLY OPERATION

The THS4211 is designed to operate from a single 5-V to 15-V power supply. When operating from a single power supply, care must be taken to ensure the input signal and amplifier are biased appropriately to allow for the maximum output voltage swing. The circuits shown in Figure 77 demonstrate methods to configure an amplifier in a manner conducive for single supply operation.
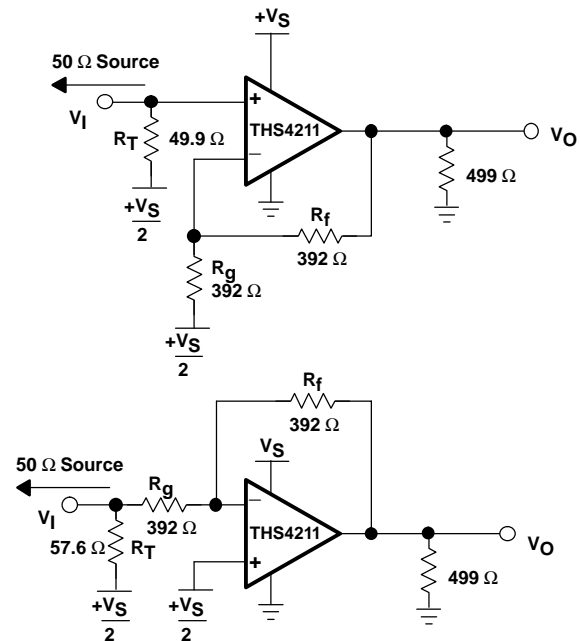

Figure 77. DC-Coupled Single Supply Operation

Saving Power With Power-Down Functionality and Setting Threshold Levels With the Reference Pin

The THS4215 features a power-down pin ($\overline{PD}$) which lowers the quiescent current from 19-mA down to 650-μA, ideal for reducing system power.

The power-down pin of the amplifiers defaults to the positive supply voltage in the absence of an applied voltage, putting the amplifier in the power-on mode of operation. To turn off the amplifier in an effort to conserve power, the power-down pin can be driven towards the

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negative rail. The threshold voltages for power-on and power-down are relative to the supply rails and given in the specification tables. Above the *Enable Threshold Voltage*, the device is on. Below the *Disable Threshold Voltage*, the device is off. Behavior in between these threshold voltages is not specified.

Note that this power-down functionality is just that; the amplifier consumes less power in power-down mode. The power-down mode is not intended to provide a high-impedance output. In other words, the power-down functionality is not intended to allow use as a 3-state bus driver. When in power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain setting resistors, but the output impedance of the device itself varies depending on the voltage applied to the outputs.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach 50% of the nominal quiescent current. The time delays are on the order of microseconds because the amplifier moves in and out of the linear mode of operation in these transitions.

Power-Down Reference Pin Operation

In addition to the power-down pin, the THS4215 also features a reference pin (REF) which allows the user to control the enable or disable power-down voltage levels applied to the $\overline{PD}$ pin. Operation of the reference pin as it relates to the power-down pin is described below.

In most split-supply applications, the reference pin will be connected to ground. In some cases, the user may want to connect it to the negative or positive supply rail. In either case, the user needs to be aware of the voltage level thresholds that apply to the power-down pin. The table below illustrates the relationship between the reference voltage and the power-down thresholds.

REFERENCE VOLTAGE	POWER-DOWN PIN VOLTAGE	
	DEVICE DISABLED	DEVICE ENABLED
V_{S-} to $0.5(V_{S-} + V_{S+})$	$\leq$ Ref + 1.0 V	$\geq$ Ref + 1.8 V
$0.5(V_{S-} + V_{S+})$ to V_{S+}	$\leq$ Ref – 1.5 V	$\geq$ Ref – 1 V

The recommended mode of operation is to tie the reference pin to mid-rail, thus setting the threshold levels to mid-rail +1.0 V and midrail +1.8 V.

NO. OF CHANNELS	PACKAGES
Single (8-pin)	THS4215D, THS4215DGN, and THS4215DRB

Power Supply Decoupling Techniques and Recommendations

Power supply decoupling is a critical aspect of any high-performance amplifier design process. Careful decoupling provides higher quality ac performance (most notably improved distortion performance). The following guidelines ensure the highest level of performance.

1. Place decoupling capacitors as close to the power supply inputs as possible, with the goal of minimizing the inductance of the path from ground to the power supply.

2. Placement priority should put the smallest valued capacitors closest to the device.

3. Use of solid power and ground planes is recommended to reduce the inductance along power supply return current paths, with the exception of the areas underneath the input and output pins.

4. Recommended values for power supply decoupling include a bulk decoupling capacitor (6.8 to 22 µF), a mid-range decoupling capacitor (0.1 µF) and a high frequency decoupling capacitor (1000 pF) for each supply. A 100 pF capacitor can be used across the supplies as well for extremely high frequency return currents, but often is not required.

APPLICATION CIRCUITS

Driving an Analog-to-Digital Converter With the THS4211

The THS4211 can be used to drive high-performance analog-to-digital converters. Two example circuits are presented below.

The first circuit uses a wideband transformer to convert a single-ended input signal into a differential signal. The differential signal is then amplified and filtered by two THS4211 amplifiers. This circuit provides low intermodulation distortion, suppressed even-order distortion, 14 dB of voltage gain, a 50-Ω input impedance, and a single-pole filter at 100 MHz. For applications without signal content at dc, this method of driving ADCs can be very useful. Where dc information content is required, the THS4500 family of fully differential amplifiers may be applicable.
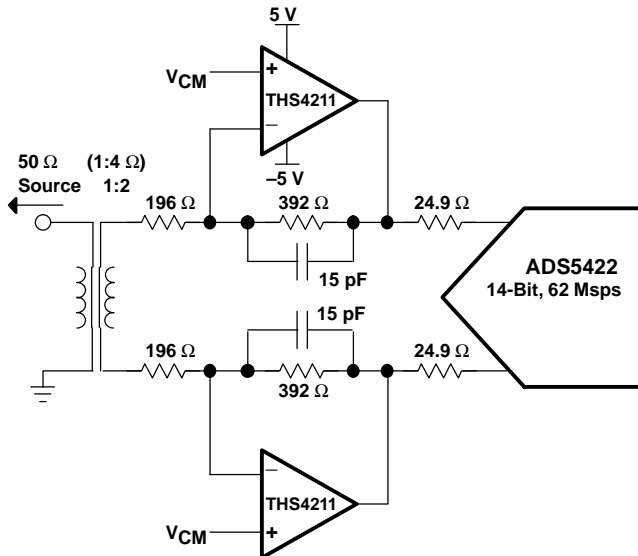
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**Figure 78. A Linear, Low Noise, High Gain
ADC Preamplifier**

The second circuit depicts single-ended ADC drive. While not recommended for optimum performance using converters with differential inputs, satisfactory performance can sometimes be achieved with single-ended input drive. An example circuit is shown here for reference.
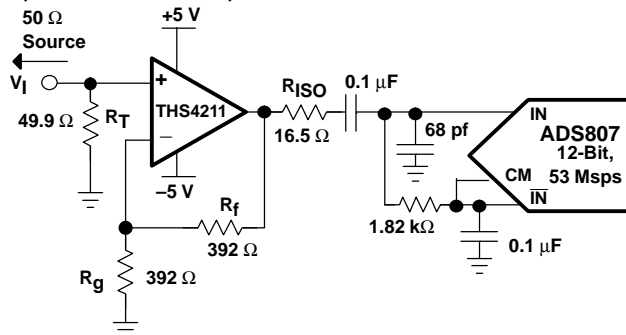
NOTE: For best performance, high-speed ADCs should be driven differentially. See the THS4500 family of devices for more information.

**Figure 79. Driving an ADC With a
Single-Ended Input**

Using the THS4211 as a DAC Output Buffer

Two example circuits are presented here showing the THS4211 buffering the output of a digital-to-analog converter. The first circuit performs a differential to single-ended conversion with the THS4211 configured as a difference amplifier. The difference amplifier can double as the termination mechanism for the DAC outputs as well.
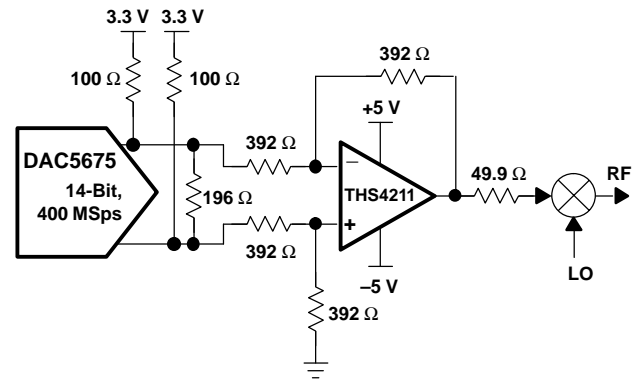
**Figure 80. Differential to Single-Ended
Conversion of a High-Speed DAC Output**

For cases where a differential signaling path is desirable, a pair of THS4211 amplifiers can be used as output buffers. The circuit depicts differential drive into a mixer's IF inputs, coupled with additional signal gain and filtering.
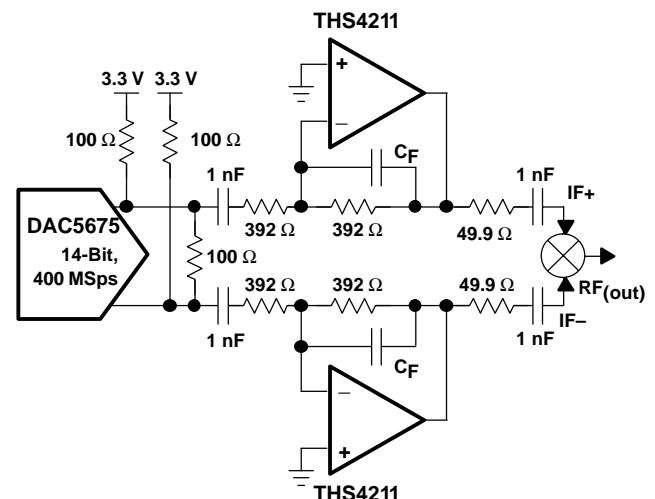
**Figure 81. Differential Mixer Drive Circuit Using
the DAC5675 and the THS4211**

Active Filtering With the THS4211

High-frequency active filtering with the THS4211 is achievable due to the amplifier's high slew-rate, wide bandwidth, and voltage feedback architecture. Several options are available for high-pass, low-pass, bandpass, and bandstop filters of varying orders. A simple two-pole low pass filter is presented here as an example, with two poles at 100 MHz.
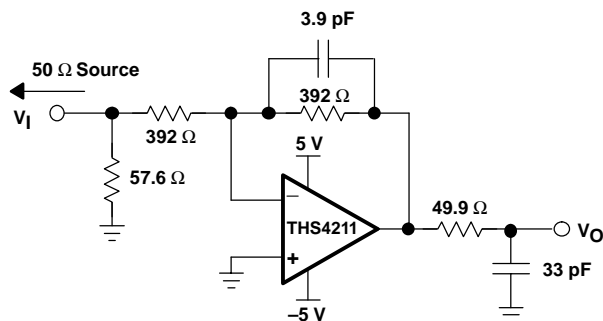
Figure 82. A Two-Pole Active Filter With Two Poles Between 90 MHz and 100 MHz

A Low-Noise Receiver With the THS4211

A combination of two THS4211 amplifiers can create a high-speed, low-distortion, low-noise differential receiver circuit as depicted in Figure 83. With both amplifiers operating in the noninverting mode of operation, the circuit presents a high load impedance to the source. The designer has the option of controlling the impedance through termination resistors if a matched termination impedance is desired.
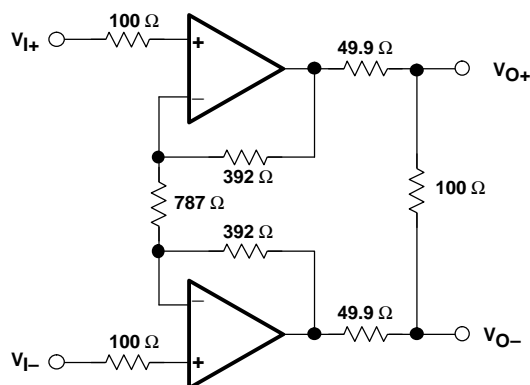

Figure 83. A High Input Impedance, Low Noise, Differential Receiver

A modification on this circuit to include a difference amplifier turns this circuit into a high-speed instrumentation amplifier, as shown in Figure 84.
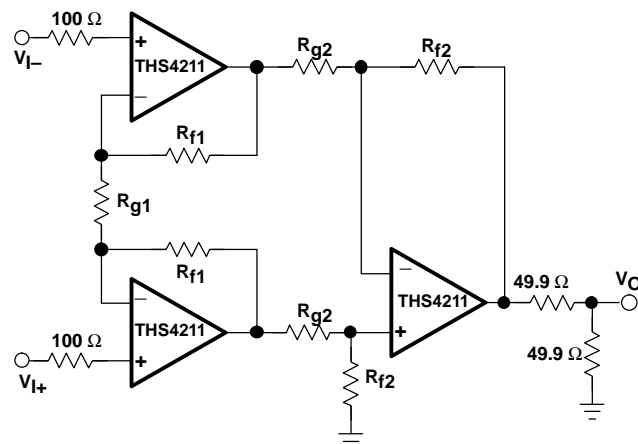

Figure 84. A High-Speed Instrumentation Amplifier

$$V_O = \frac{1}{2}\left(1 + \frac{2R_{f1}}{R_{g1}}\right)(V_{i+} - V_{i-})\left(\frac{R_{f2}}{R_{g2}}\right) \qquad (1)$$

THEORY AND GUIDELINES

Distortion Performance

The THS4211 provides excellent distortion performance into a 150-Ω load. Relative to alternative solutions, it provides exceptional performance into lighter loads, as well as exceptional performance on a single 5-V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd harmonic will dominate the total harmonic distortion with a negligible 3rd harmonic component. Focusing then on the 2nd harmonic, increasing the load impedance improves distortion directly. The total load includes the feedback network; in the noninverting configuration (Figure 75) this is the sum of R_f and R_g, while in the inverting configuration (Figure 76), only R_f needs to be included in parallel with the actual load.

LINEARITY: DEFINITIONS, TERMINOLOGY, CIRCUIT TECHNIQUES, AND DESIGN TRADEOFFS

The THS4211 features execellent distortion performance for monolithic operational amplifiers. This section focuses on the fundamentals of distortion, circuit techniques for reducing nonlinearity, and methods for equating distortion of operational amplifiers to desired linearity specifications in RF receiver chains.

Amplifiers are generally thought of as *linear* devices. The output of an amplifier is a linearly scaled version of the input signal applied to it. However, amplifier transfer functions are nonlinear. Minimizing amplifier nonlinearity is a primary design goal in many applications.

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Intercept points are specifications long used as key design criteria in the RF communications world as a metric for the intermodulation distortion performance of a device in the signal chain (e.g., amplifiers, mixers, etc.). Use of the intercept point, rather than strictly the intermodulation distortion, allows simpler system-level calculations. Intercept points, like noise figures, can be easily cascaded back and forth through a signal chain to determine the overall receiver chain's intermodulation distortion performance. The relationship between intermodulation distortion and intercept point is depicted in Figure 85 and Figure 86.
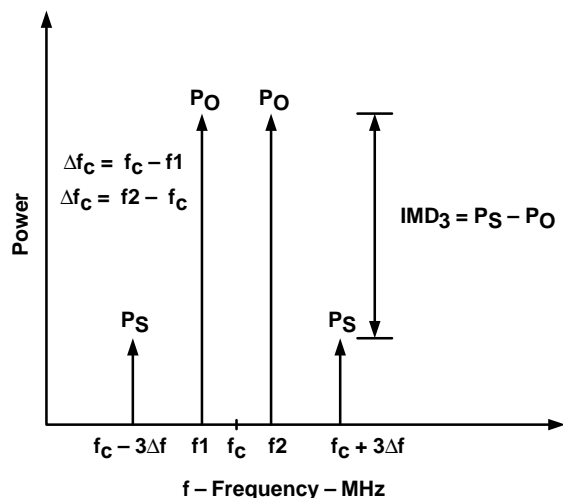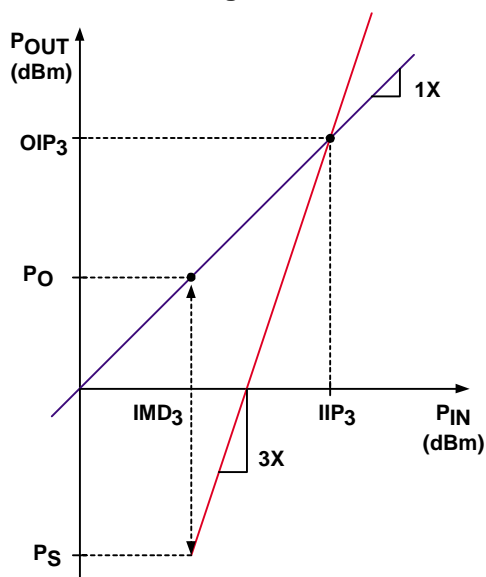

Figure 85

Figure 86

Due to the intercept point's ease of use in system level calculations for receiver chains, it has become the specification of choice for guiding distortion-related design decisions. Traditionally, these systems use primarily class-A, single-ended RF amplifiers as gain blocks. These RF amplifiers are typically designed to operate in a 50-Ω environment. Giving intercept points in dBm implies an associated impedance (50 Ω).

However, with an operational amplifier, the output does not require termination as an RF amplifier would. Because closed-loop amplifiers deliver signals to their outputs regardless of the impedance present, it is important to comprehend this when evaluating the intercept point of an operational amplifier. The THS4211 yields optimum distortion performance when loaded with 150 Ω to 1 kΩ, very similar to the input impedance of an analog-to-digital converter over its input frequency band.

As a result, terminating the input of the ADC to 50 Ω can actually be detrimental to systems performance.

The discontinuity between open-loop, class-A amplifiers and closed-loop, class-AB amplifiers becomes apparent when comparing the intercept points of the two types of devices. Equations 1 and 2 gives the definition of an intercept point, relative to the intermodulation distortion.

$$OIP_3 = P_O + \left(\frac{|IMD_3|}{2}\right) \text{ where} \tag{2}$$

$$P_O = 10 \log\left(\frac{V_P^2}{2R_L \times 0.001}\right) \tag{3}$$

NOTE: P_O is the output power of a single tone, R_L is the load resistance, and V_P is the peak voltage for a single tone.

NOISE ANALYSIS

High slew rate, unity gain stable, voltage-feedback operational amplifiers usually achieve their slew rate at the expense of a higher input noise voltage. The 7 nV/$\sqrt{Hz}$ input voltage noise for the THS4211 and THS4215 is, however, much lower than comparable amplifiers. The input-referred voltage noise, and the two input-referred current noise terms (4 pA/$\sqrt{Hz}$), combine to give low output noise under a wide variety of operating conditions. Figure 87 shows the amplifier noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

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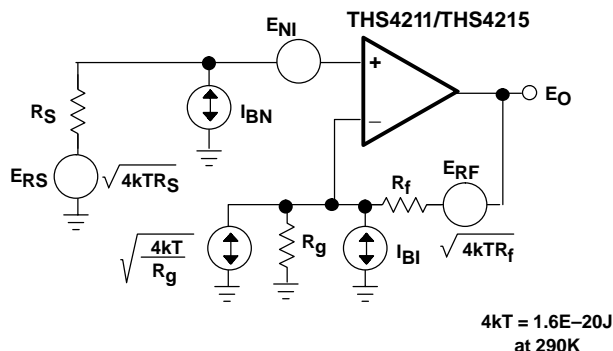
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Figure 87. Noise Analysis Model

The total output shot noise voltage can be computed as the square of all square output noise voltage contributors. Equation 3 shows the general form for the output noise voltage using the terms shown in Figure 87:

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_f\right)^2 + 4kTR_f NG} \quad (4)$$

Dividing this expression by the noise gain ($NG = (1 + R_f/R_g)$) gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 4:

$$E_O = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_f}{NG}\right)^2 + \frac{4kTR_f}{NG}} \quad (5)$$

Driving Capacitive Loads

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter, including additional external capacitance, which may be recommended to improve A/D linearity. A high-speed, high open-loop gain amplifier like the THS4211 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. When the primary considerations are frequency response flatness, pulse response fidelity, or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended isolation resistor vs capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2 pF can begin to degrade the performance

of the THS4211. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the THS4211 output pin (see Board Layout Guidelines).

The criterion for setting this $R_{(ISO)}$ resistor is a maximum bandwidth, flat frequency response at the load. For a gain of +2, the frequency response at the output pin is already slightly peaked without the capacitive load, requiring relatively high values of $R_{(ISO)}$ to flatten the response at the load. Increasing the noise gain also reduces the peaking.
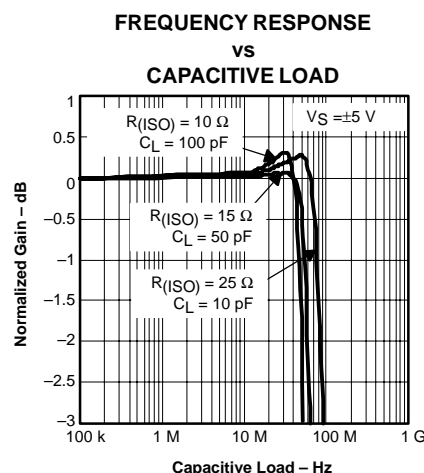

Figure 88. Isolation Resistor Diagram

BOARD LAYOUT

Achieving optimum performance with a high frequency amplifier like the THS4211 requires careful attention to board layout parasitics and external component types.

Recommendations that optimize performance include the following:

1. **Minimize parasitic capacitance to any ac ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

2. **Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1-μF de-coupling capacitors.** At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the

decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

3. **Careful selection and placement of external components preserves the high frequency performance of the THS4211.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wire-wound type resistors in a high frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input-termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 2.0 kΩ, this parasitic capacitance can add a pole and/or a zero below 400 MHz that can effect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations. A good starting point for design is to set the R_f to 249 Ω for low-gain, noninverting applications. This setting automatically keeps the resistor noise terms low and minimizes the effect of their parasitic capacitance.

4. **Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines.** For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic capacitive loads (<4 pF) may not need an $R_{(ISO)}$, since the THS4211 is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an $R_{(ISO)}$ are allowed as the signal gain increases (increasing the unloaded phase margin). If

a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and in fact a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined on the basis of board material and trace dimensions, a matching series resistor into the trace from the output of the THS4211 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of $R_{(ISO)}$ vs capacitive load. This setting does not preserve signal integrity or a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

5. **Socketing a high speed part like the THS4211 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create a troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS4211 onto the board.

PowerPAD™ DESIGN CONSIDERATIONS

The THS4211 and THS4215 are available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 89(a) and Figure 89(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 89(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows both assembly and thermal management in one manufacturing operation.

During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package.

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Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the heretofore awkward mechanical methods of heatsinking.
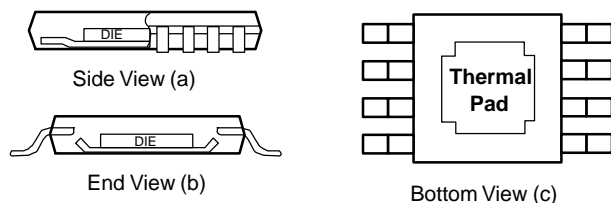

Figure 89. Views of Thermally Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.
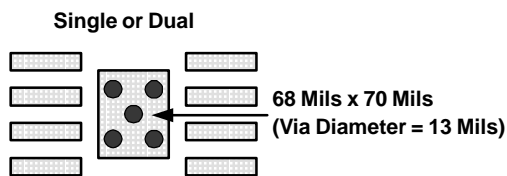

Figure 90. PowerPAD PCB Etch and Via Pattern

PowerPAD PCB LAYOUT CONSIDERATIONS

1. Prepare the PCB with a top side etch pattern as shown in Figure 90. There should be etching for the leads as well as etch for the thermal pad.

2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.

3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. They help dissipate the heat generated by the THS4211 and THS4215 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so wicking is not a problem.

4. Connect all holes to the internal ground plane.

5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the

heat transfer during soldering operations. This resistance makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS4211 and THS4215 PowerPAD package should make their connection to the internal ground plane, with a complete connection around the entire circumference of the plated-through hole.

6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.

7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For a given θ_{JA}, the maximum power dissipation is shown in Figure 91 and is calculated by the equation 5:

$$P_D = \frac{T_{max} - T_A}{\theta_{JA}} \qquad (6)$$

where
P_D = Maximum power dissipation of THS4211 (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient temperature (°C)
$\qquad \theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to the case
θ_{CA} = Thermal coefficient from the case to ambient air (°C/W).

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class AB), most of the heat dissipation is at low output voltages with high output currents.

The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. For a single package, the sum of the RMS output currents and voltages should be used to choose the proper package.

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THERMAL ANALYSIS

The THS4211 device does not incorporate automatic thermal shutoff protection, so the designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of 150° C is exceeded.

The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using the following formula:

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}}$$

where

P_{Dmax} is the maximum power dissipation in the amplifier (W).
T_{max} is the absolute maximum junction temperature (°C).
T_A is the ambient temperature (°C).
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

For systems where heat dissipation is more critical, the THS4211 is offered in an 8-pin MSOP with PowerPAD. The thermal coefficient for the MSOP PowerPAD package is substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in the graph for the two packages. The data for the DGN package assumes a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application notes in the *Additional Reference Material* section at the end of the data sheet.
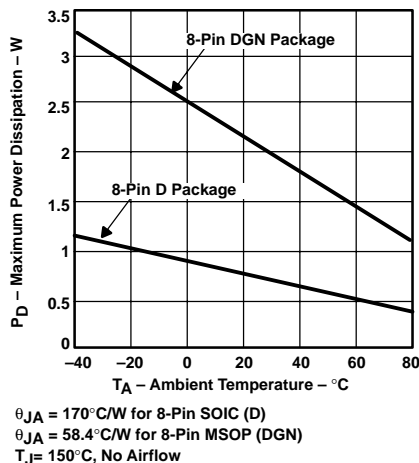

θ_{JA} = 170°C/W for 8-Pin SOIC (D)
θ_{JA} = 58.4°C/W for 8-Pin MSOP (DGN)
T_J= 150°C, No Airflow

**Figure 91. Maximum Power Dissipation vs
Ambient Temperature**

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to consider not only quiescent power dissipation, but also dynamic power dissipation. Often maximum power dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

DESIGN TOOLS

Performance vs Package Options

The THS4211 and THS4215 are offered in a different package options. However, performance may be limited due to package parasitics and lead inductance in some packages. In order to achieve maximum performance of the THS4211 and THS4215, Texas Instruments recommends using the leadless MSOP (DRB) or MSOP (DGN) packages, in additions to proper high-speed PCB layout. Figure 92 shows the unity gain frequency response of the THS4211 using the leadless MSOP, MSOP, and SOIC package for comparison. Using the THS4211 and THS4215 in a unity gain with the SOIC package may result in the device becoming unstable. In higher gain configurations, this effect is mitigated by the reduced bandwidth. As such, the SOIC is suitable for application with gains equal to or higher than +2 V/V or (–1 V/V).
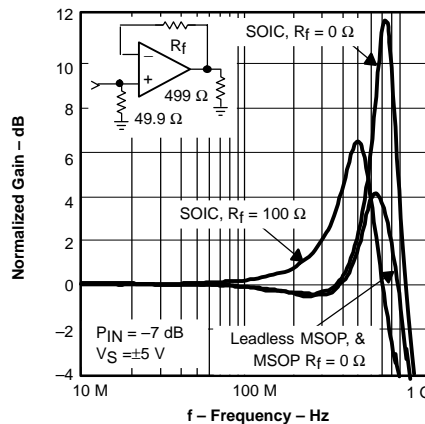

**Figure 92. Effects of Unity Gain Frequency
Response for Differential Packages**

Evaluation Fixtures, Spice Models, and Applications Support

Texas Instruments is committed to providing its customers with the highest quality of applications support. To support this goal, evaluation boards have been developed for the THS4211 operational amplifier. Three evaluation boards are available: one THS4211 and one THS4215, both configurable for different gains, and a third for a gain of +1 (THS4211 only). These boards are easy to use, allowing for straightforward evaluation of the device. These evaluation boards can be ordered through the Texas Instruments web site, www.ti.com, or through your local Texas Instruments sales representative. Schematics for the evaluation boards are shown below.

The THS4211/THS4215 EVM board shown in Figure 96 through Figure 99 accommodates different gain configurations. Its default component values are set to give a gain of 2. The EVM can be configured in a gain of +1; however, it is strongly not recommended. Evaluating the THS4211/THS4215 in a gain of +1 using this EVM may cause the part to become unstable. The stability of the device can be controlled by adding a large resistor in the feedback path, but the performance is sacrificed. Figure 93 shows the small signal frequency response of the THS4211 with different feedback resistors in the feedback path. Figure 94 is the small frequency response of the THS4211 using the gain of +1 EVM.
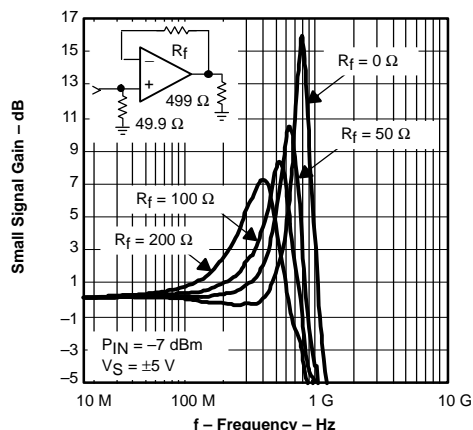

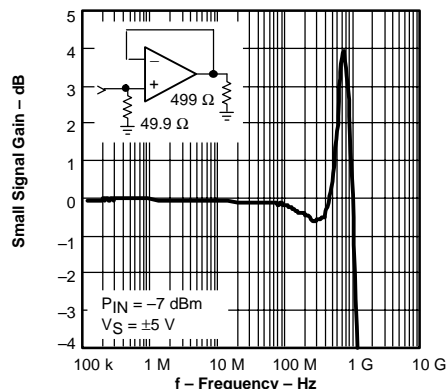**Figure 93. Frequency Response vs Feedback Resistor Using the EDGE #6439527 EVM**

Figure 94. Frequency Response Using the EDGE # 6443547 G = +1 EVM

The peaking in the frequency response is due to the lead inductance in the feedback path. Each pad and trace on a PCB has an inductance associated with it, which in conjunction with the inductance associated with the package may cause peaking in the frequency response, causing the device to become unstable.

In order to achieve the maximum performance of the device, PCB layout is very critical. Texas Instruments has developed an EVM for the evaluation of the THS4211 in a gain of 1. The EVM is shown in Figure 101 through Figure 104. This EVM is designed to minimize peaking in the unity gain configuration.

Minimizing the inductance in the feedback path is critical for reducing the peaking of the frequency response in unity gain. The recommended maximum inductance allowed in the feedback path is 4 nH. This inductance can be calculated by using equation 7:

$$L(nH) = K\ell \left[\ln \frac{2\ell}{W + T} + 0.223 \frac{W + T}{\ell} + 0.5 \right] \quad (7)$$

where
W = Width of trace in inches.
ℓ = Length of the trace in inches.
T = Thickness of the trace in inches.
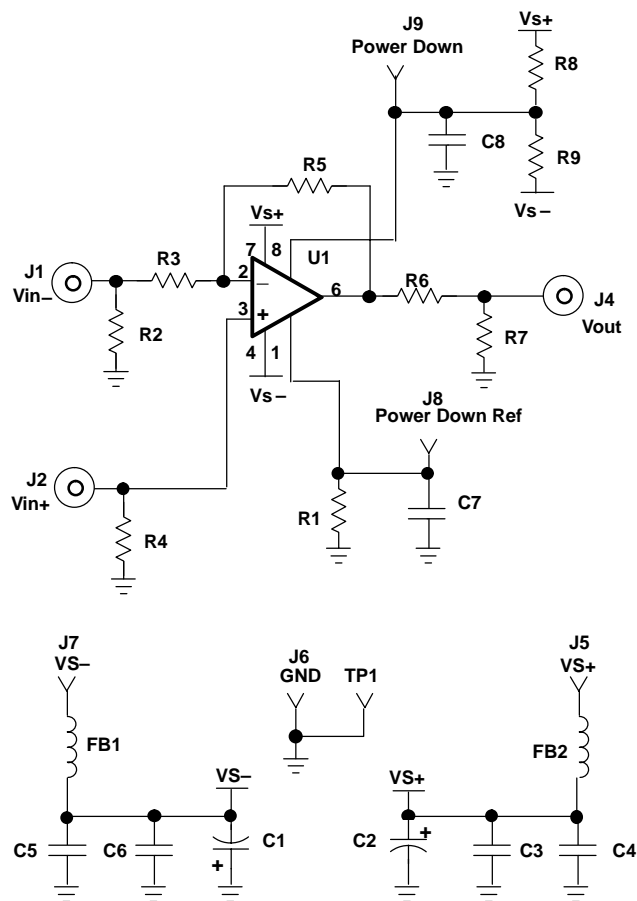K = 5.08 for dimensions in inches, and K = 2 for dimensions in cm.

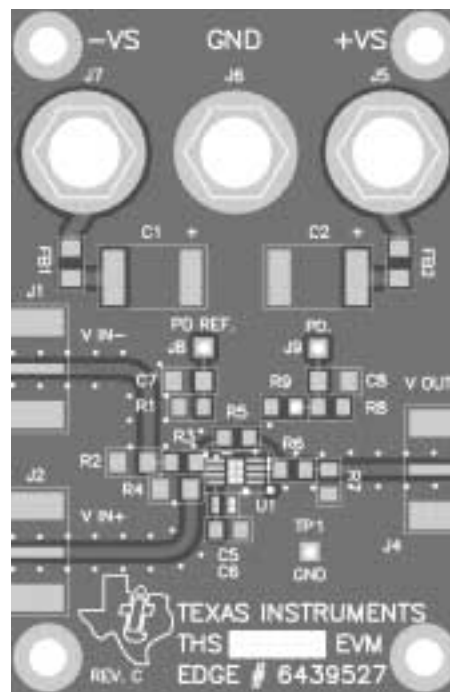**Figure 95. THS4211/THS4215 EVM Circuit Configuration**

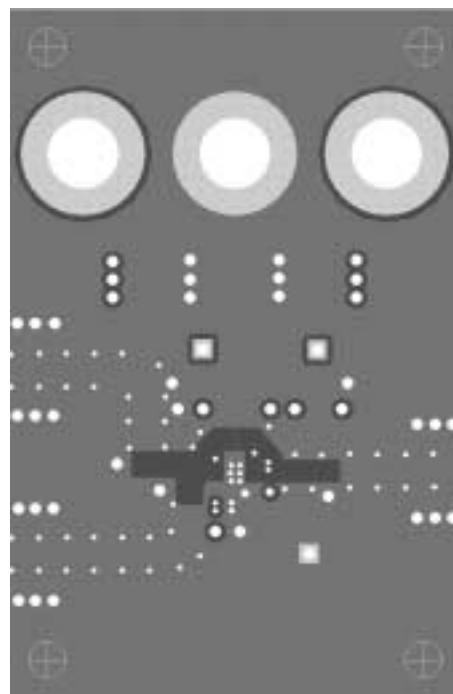**Figure 96. THS4211/THS4215 EVM Board Layout (Top Layer)**

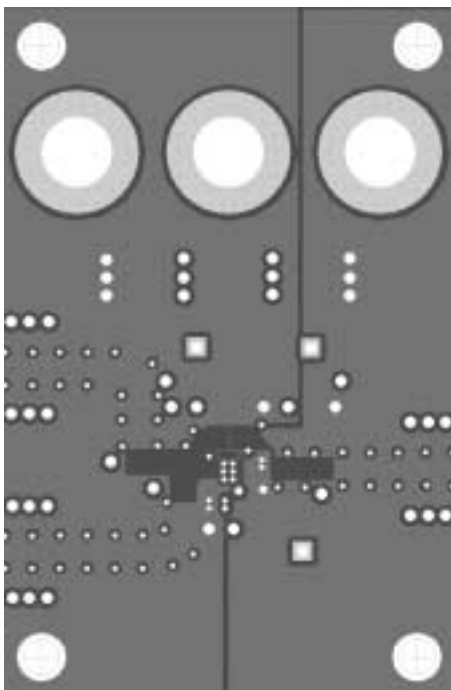**Figure 97. THS4211/THS4215 EVM Board Layout (Second Layer, Ground)**

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Figure 98. THS4211/THS4215 EVM Board Layout (Third Layer, Power)
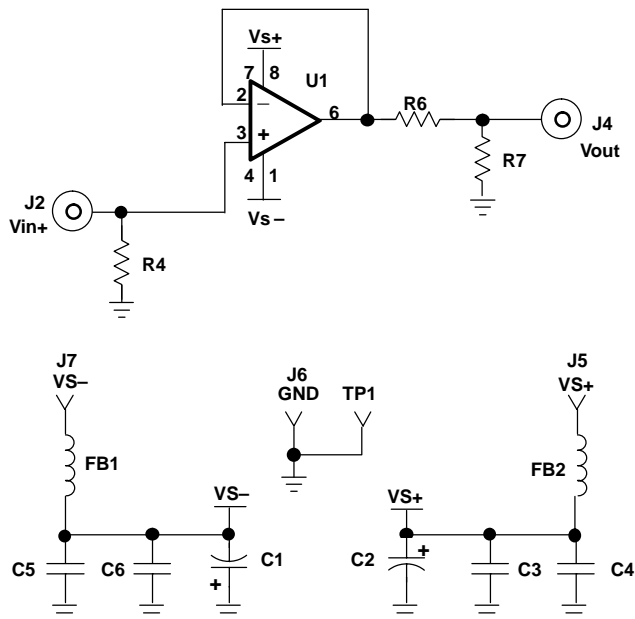

Figure 100. THS4211 Unity Gain EVM Circuit Configuration

Figure 99. THS4211/THS4215 EVM Board Layout (Bottom Layer)
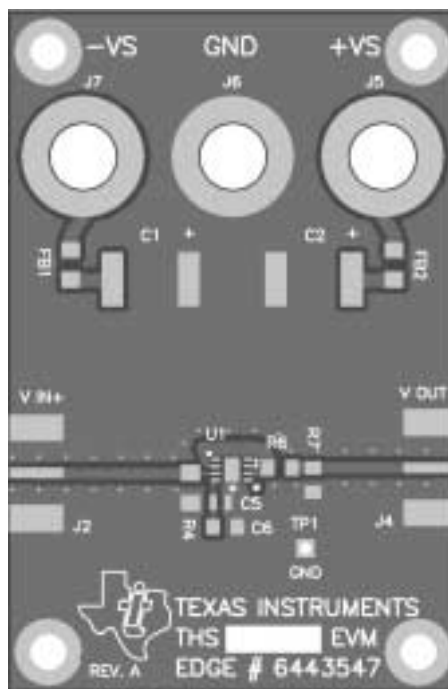
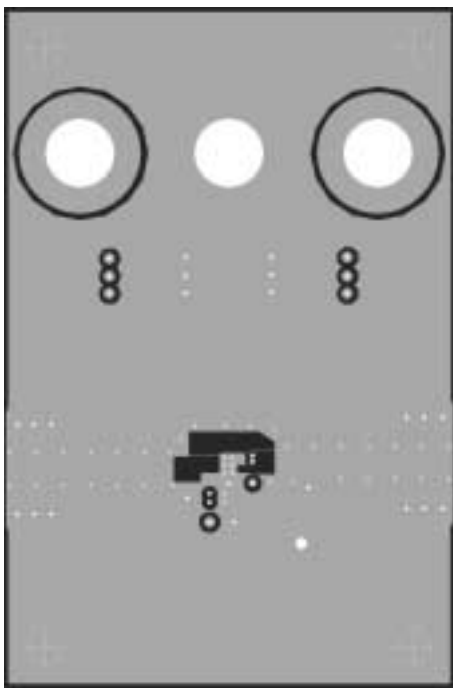

Figure 101. THS4211 Unity Gain EVM Board Layout (Top Layer)

Figure 102. THS4211 Unity Gain EVM Board Layout (Second Layer, Ground)

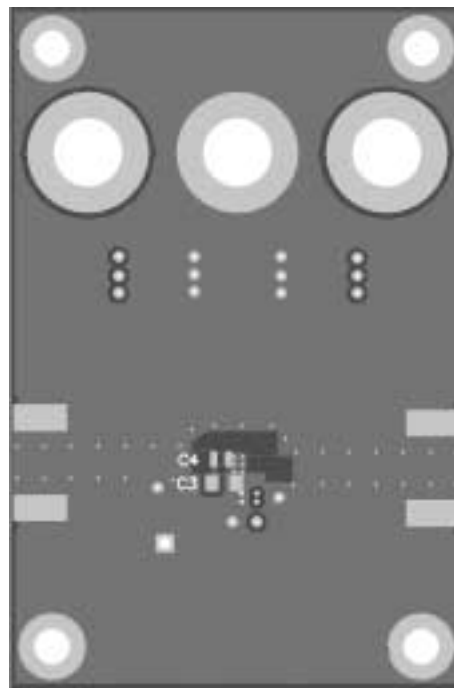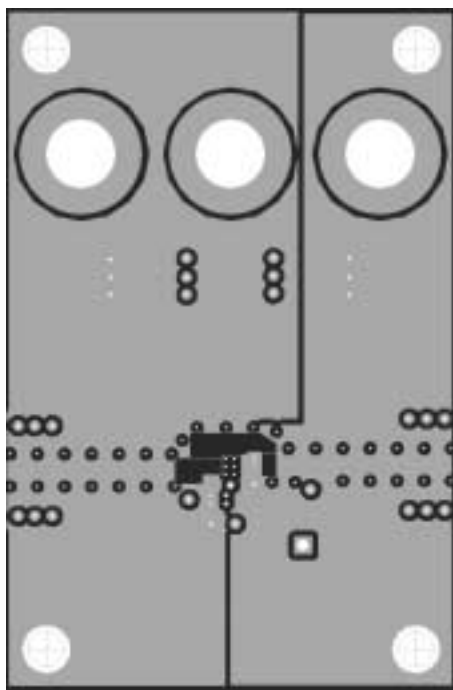**Figure 104. THS4211 Unity Gain EVM Board Layout (Bottom Layer)**

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits, where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS4211 is available through either the Texas Instruments web site (www.ti.com) or as one model on a disk from the Texas Instruments Product Information Center (1–800–548–6132). The PIC is also available for design assistance and detailed product information at this number. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They are not intended to model the distortion characteristics of the amplifier, nor do they attempt to distinguish between the package types in their small-signal ac performance. Detailed information about what is and is not modeled is contained in the model file itself.
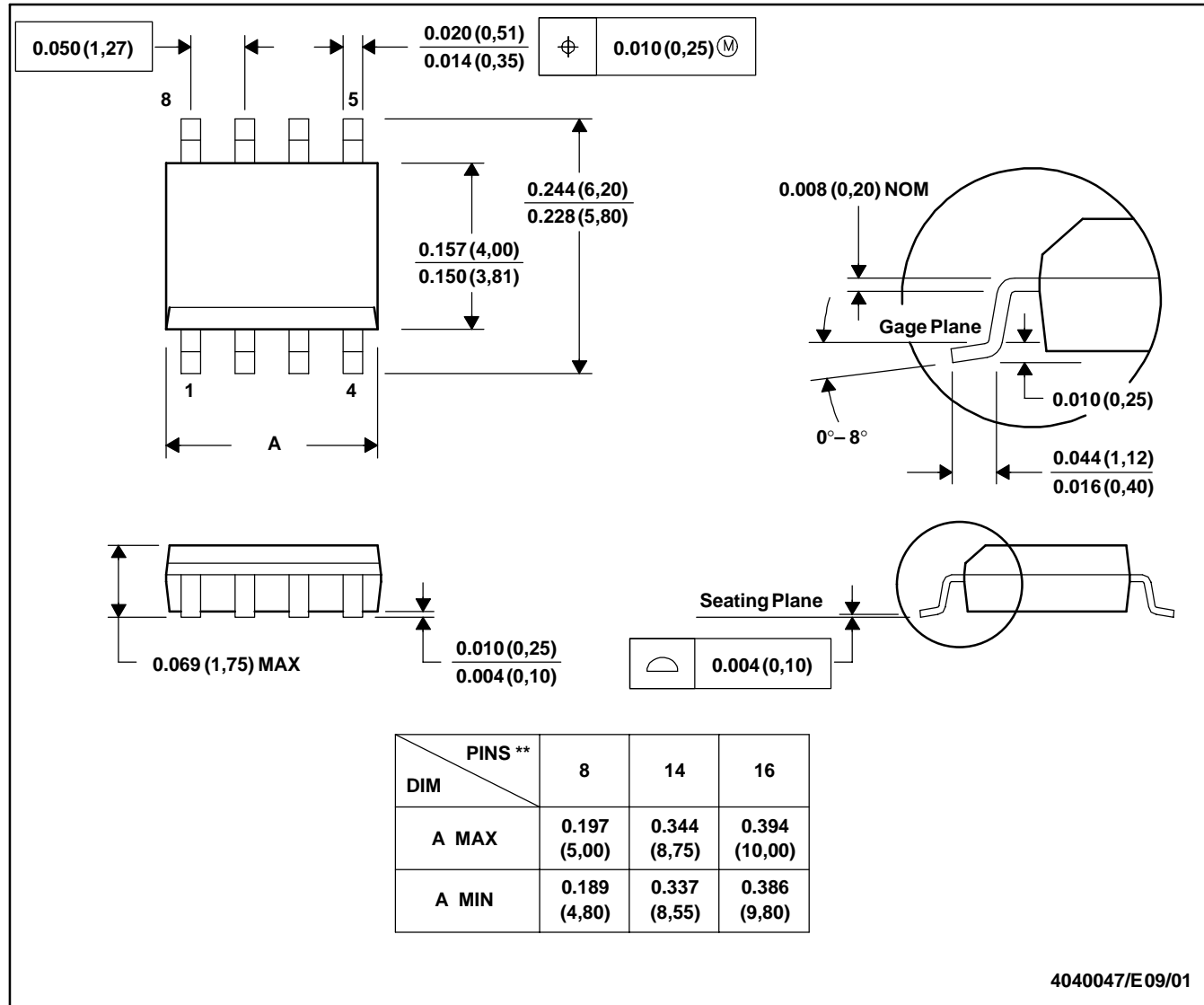
ADDITIONAL REFERENCE MATERIAL

- *PowerPAD Made Easy*, application brief (SLMA004)

- *PowerPAD Thermally Enhanced Package*, technical brief (SLMA002)

Figure 103. THS4211 Unity Gain EVM Board Layout (Third Layer, Power)

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MECHANICAL DATA

D (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN

PINS ** DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01
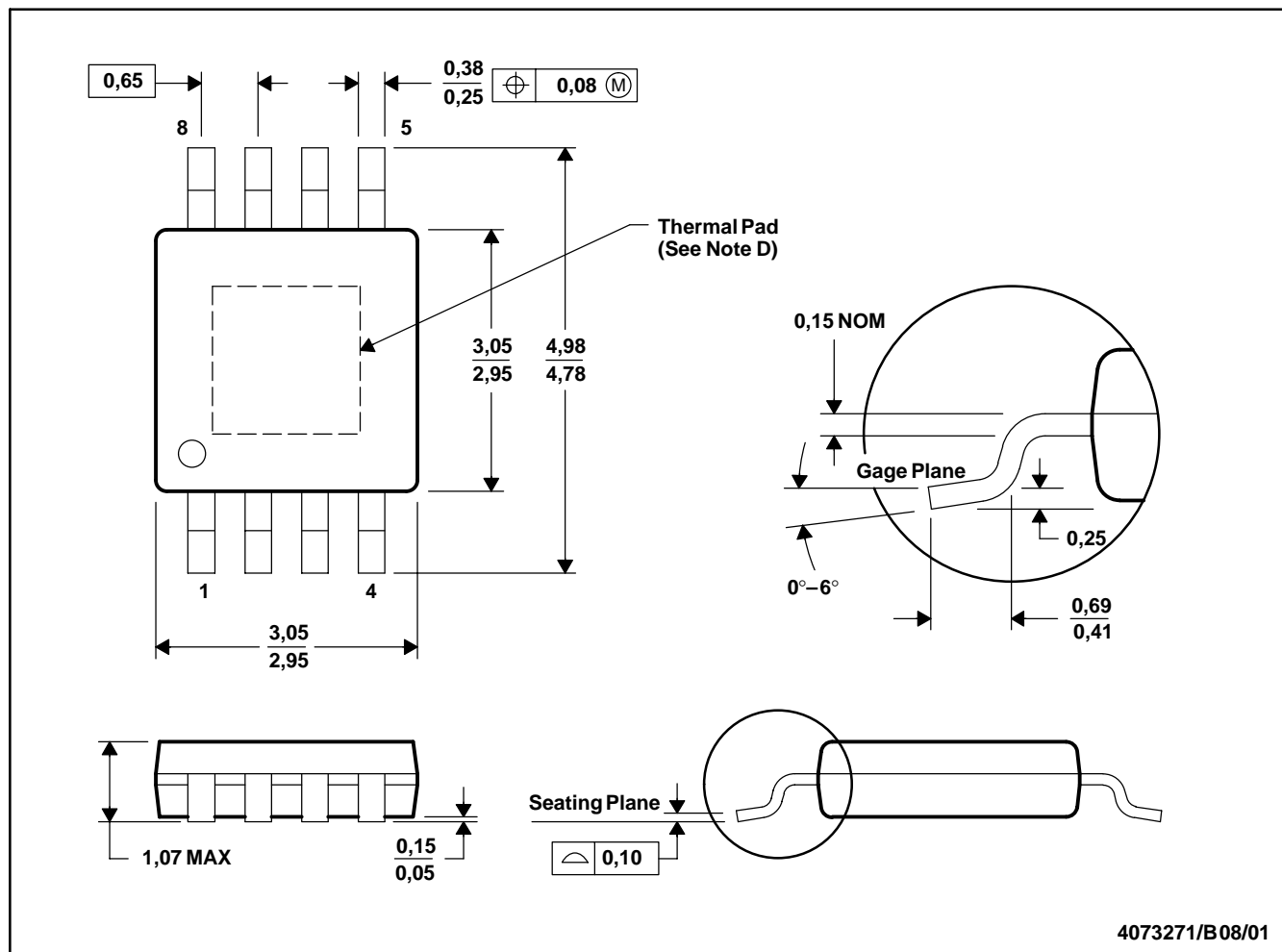
NOTES: A. All linear dimensions are in inches (millimeters).
     B. This drawing is subject to change without notice.
     C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
     D. Falls within JEDEC MS-012

MECHANICAL DATA

DGN (S-PDSO-G8)   **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**
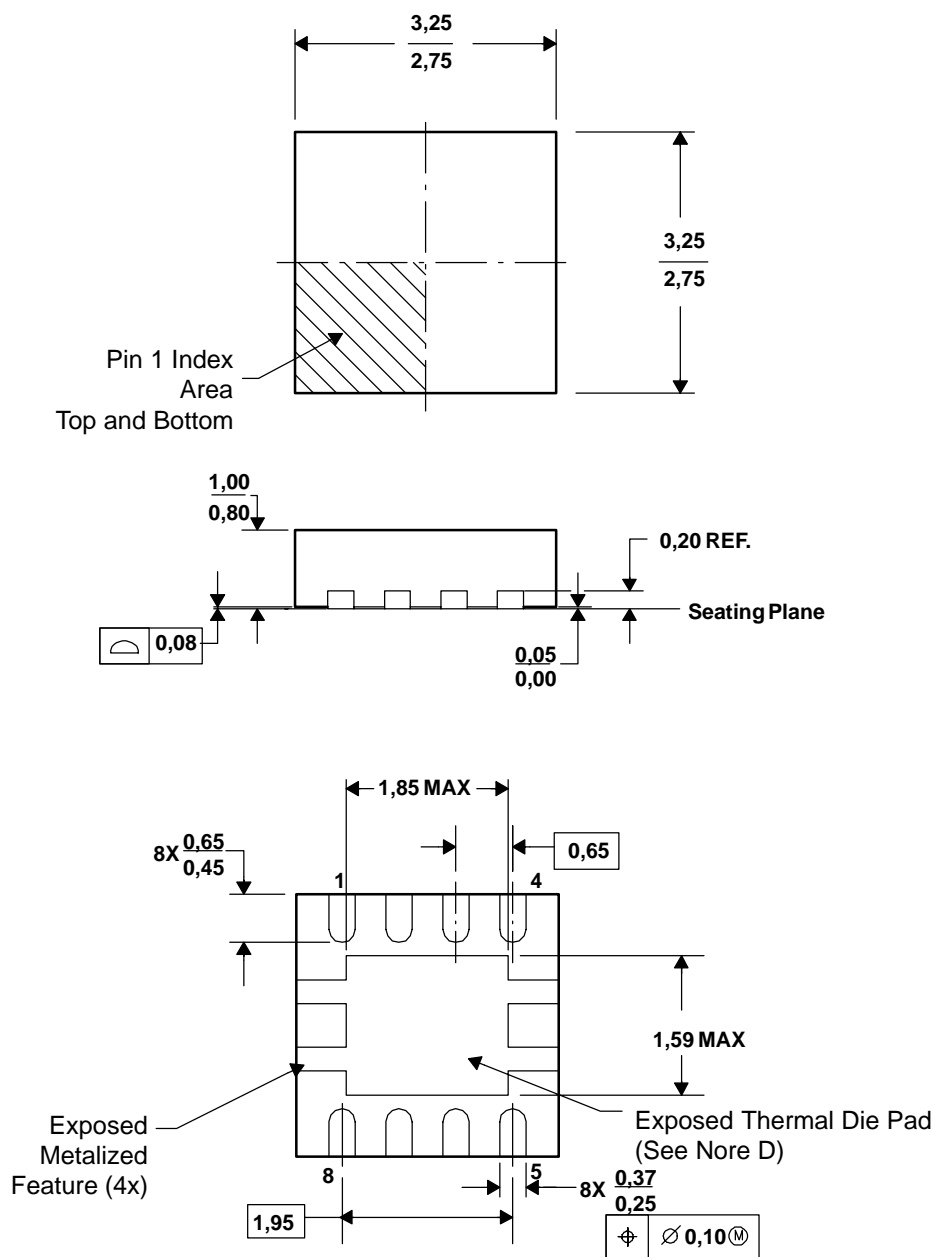

4073271/B 08/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal plane.
This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-187

PowerPAD is a trademark of Texas Instruments.

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MECHANICAL DATA

DRB (S-PDSO-N8)   **PLASTIC SMALL OUTLINE**

4203482/B 03/02

NOTES: A. All linear dimensions are in millimeters.
    B. This drawing is subject to change without notice.
    C. Small Outline No-lead (SON) package configuration.
    D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.

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