AUDIO CODEC WITH INTEGRATED HEADPHONE, SPEAKER AMPLIFIER AND TOUCH SCREEN CONTROLLER

FEATURES

- **Stereo Audio Playback Up to 48 ksps**
- **Mono Audio Record up to 48 ksps**
- **Integrated PLL for Audio Clock Generation**
- **Programmable Gain Amplifiers**
- **Hardware Automatic Gain Control**
- **Programmable Digital Audio Effects Processing**
- **Stereo Headset Interface**
- **Cellular Headset Interface**
- **8-Ω Speaker Driver**
- **32-Ω Receiver Driver**
- **Interface with Microphone**
- **Auto-Detection of Headset and Button Press**
- **Supports Both Cap and Cap-Less Interface for Headset**
- **Programmable Audio Routing**
- **4-Wire Touch Screen Interface**
- **Integrated Touch Screen Processor With Fully Automated Modes of Operation**
- **Programmable Converter Resolution, Speed, and Averaging**
- **Programmable Autonomous Timing Control**
- **Direct Battery Measurement**
- **Built-In Buffer for Touch Screen Data**
- **SPI™ Serial Interface**
- **Low Power**
- **Full Power-Down Control**
- **48-Pin QFN Package**

APPLICATIONS

- **Personal Digital Assistants**
- **Smart Cellular Phones**
- **MP3 Players**

DESCRIPTION

The TSC2101 is a low-power highly integrated high performance codec and touch screen controller, which supports stereo audio DAC, monaural voice ADC and SAR ADC.

The TSC2101 features a high-performance audio codec with 16, 20, 24, or 32-bit stereo playback, mono record functionality at up to 48 ksps. The device integrates several analog features such as support for headset interface, cellular headset interface, microphone interface, and speaker and receiver drivers. The device supports auto detection of headset and button press without any glue logic. The TCS2101 has fully programmable audio. The digital audio data format is programmable to work with popular audio standard protocols (I2S, DSP, left/right justified) in master or slave mode, and also includes an on-chip PLL for flexible clock generation capability.

The TSC2102 contains a 12-bit 4-wire resistive touch screen converter complete with drivers, and interfaces to the host controller through a standard SPI™ serial interface. The on-chip processor provides extensive features specifically designed to reduce host processor and bus overhead, with capabilities that include fully automated operating modes, programmable conversion resolution up to 12 bits, programmable sampling rates up to 125 kHz, programmable conversion averaging, and programmable on-chip timing generation.

The TSC2102 offers battery measurement inputs capable of reading battery voltages up to 6 V, while operating at only 3 V. It also has an on-chip temperature sensor capable of reading 0.3°C resolution. The TSC2102 is available in a 48-lead QFN.

US Patent No. 624639

PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

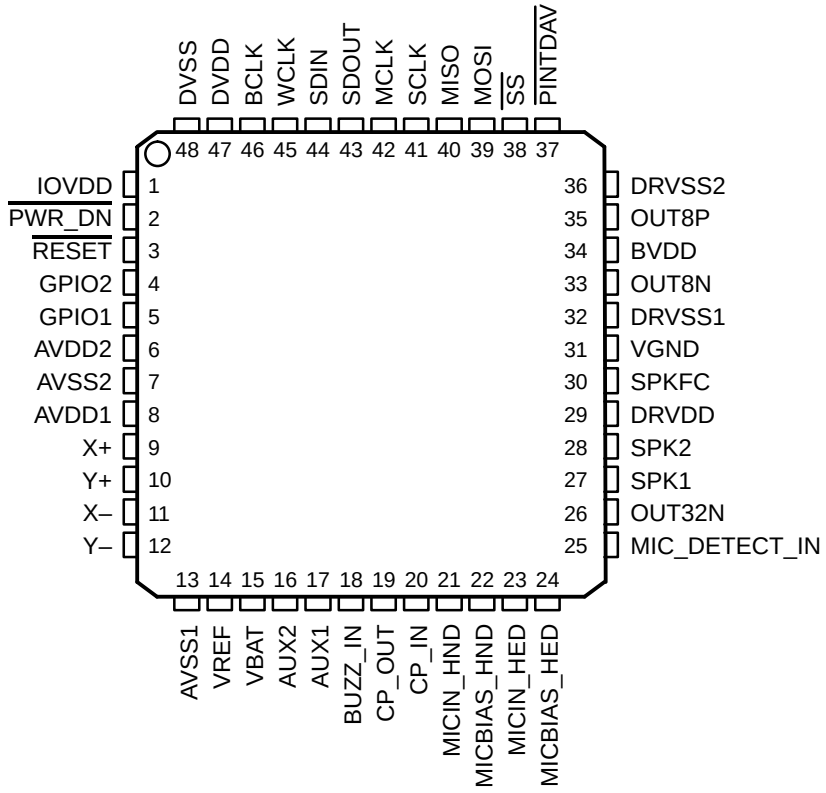
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA
TSC2101IRGZ	QFN-48	RGZ	–40°C to +85°C	TSC2101IRGZ	Rails, 52
				TSC2101IRGZR	Tape and Reel, 2000

PIN ASSIGNMENTS

(TOP VIEW) **QFN**



PRODUCT PREVIEW

Terminal Functions

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	IOVDD	IO Supply	25	MIC_DETECT_IN	Microphone detect input
2	$\overline{\text{PWR\_DN}}$	Hardware power down	26	OUT32N	Receiver driver output
3	$\overline{\text{RESET}}$	Hardware reset	27	SPK1	Headset driver output/receiver driver output
4	GPIO2	General purpose IO	28	SPK2	Headset driver output
5	GPIO1	General purpose IO	29	DRVDD	Headphone driver power supply
6	AVDD2	Touch screen drivers, PLL analog power supply	30	SPKFC	Driver feedback/ speaker detect input
7	AVSS2	Analog ground	31	VGND	Virtual ground for audio output
8	AVDD1	Audio ADC, DAC, reference, SAR, ADC analog power supply	32	DRVSS1	Driver ground
9	X+	X+ Position input and driver	33	OUT8N	Loudspeaker driver output
10	Y+	Y+ Position input and driver	34	BVDD	Battery power supply
11	X–	X– Position input and driver	35	OUT8P	Loudspeaker driver output
12	Y–	Y– Position input and driver	36	DRVSS2	Driver ground
13	AVSS1	Analog ground	37	$\overline{\text{PINTDAV}}$	Pin interrupt/data available output
14	VREF	Reference voltage	38	$\overline{\text{SS}}$	SPI Slave select input
15	VBAT	Battery monitor input	39	MOSI	SPI Serial data input
16	AUX2	Secondary auxiliary input	40	MISO	SPI Serial data output
17	AUX1	First auxiliary input	41	SCLK	SPI Serial clock input
18	BUZZ_IN	Buzzer input	42	MCLK	Master clock
19	CP_OUT	Output to cell phone module	43	SDOUT	Audio data output
20	CP_IN	Input from cell phone module	44	SDIN	Audio data input
21	MICIN_HND	Handset microphone input	45	WCLK	Audio word clock
22	MICBIAS_HND	Handset microphone bias voltage	46	BCLK	Audio bit clock
23	MICIN_HED	Headset microphone input	47	DVDD	Digital core supply
24	MICBIAS_HED	Headset microphone bias voltage	48	DVSS	Digital core and IO ground

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNITS
AVDD1/2 to AVSS1/2		–0.3 V to 3.9 V
DRVDD to DRVSS1/2		–0.3 V to 3.9 V
BVDD to DRVSS1/2		–0.3 V to 4.5 V
IOVDD to DVSS		–0.3 V to 3.9 V
Digital input voltage to GND		–0.3 V to IOVDD + 0.3 V
Operating temperature range		–40°C to 85°C
Storage temperature range		–65°C to 105°C
Junction temperature (T_J Max)		105°C
QFN package	Power dissipation	$(T_J \text{ Max} - T_A)/\theta_{JA}$
	θ_{JA} Thermal impedance	27°C/W
Lead temperature	Infrared (15 sec)	240°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

At +25°C, AVDD1, AVDD2, DRVDD, IOVDD = 3.3 V, BVDD = 3.9 V, DVDD = 1.8 V, V_{ref} = 2.5 V, Fs (Audio) = 48 kHz, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TOUCH SCREEN					
AUXILIARY ANALOG INPUT					
Input voltage range	AUX1/2 input selected as input by touch-screen	0		+VREF	V
Input capacitance			25		pF
Input leakage current			±1		µA
BATTERY MONITOR INPUTS					
Input voltage range		0.5		6.0	V
Input leakage current	Battery conversion not selected		±1		µA
Accuracy	Variation across temperature after system calibration at room temperature		±25		mV
TOUCH SCREEN A/D CONVERTER					
Resolution	Programmable: 8-, 10-,12-bits	8		12	Bits
No missing codes	12-Bit resolution		11		Bits
Integral nonlinearity		–5		5	LSB
Offset error		–6		6	LSB
Gain error		–6		6	LSB
Noise			50		µVrms
VOLTAGE REFERENCE	VREF				
Voltage range	VREF output programmed = 2.5 V		2.5		V
	VREF output programmed = 1.25 V		1.25		
Voltage range	External reference	1.1		2.5	V
Reference drift	Internal VREF = 1.25 V		200		ppm/°C
Current drain	Extra current drawn when the internal reference is turned on.		500		µA
AUDIO CODEC					
ADC CHANNEL FILTER CHARACTERISTICS					
Filter gain from 0 to 0.39 Fs			±0.1		dB
Filter gain at 0.4125 Fs			–0.6		dB
Filter gain at 0.45 Fs			–3.25		dB
Filter gain at 0.5 Fs			–17.5		dB
Filter gain from 0.55 Fs to 64 Fs			–75		dB
Group delay			17/Fs		sec

ELECTRICAL CHARACTERISTICS (continued)

At +25°C, AVDD1, AVDD2, DRVDD, IOVDD = 3.3 V, BVDD = 3.9 V, DVDD = 1.8 V, Int. V_{ref} = 2.5 V, Fs (Audio) = 48 kHz, unless otherwise noted (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MICROPHONE INPUT TO ADC	MICIN_HED 1020 Hz sine wave input, Fs = 48 ksps				
Full-scale input voltage (0 dB)			0.707		Vrms
Input common mode			1.5		V
SNR	Measured as idle channel noise, 0 dB gain, A-weighted		88		dBA
THD	0.63 Vrms input, 0-dB gain		80		dB
PSRR	217 Hz, 100 mV on AVDD1/2(1)		55		dB
	1020 Hz, 100 mV on AVDD1/2(1)		55		dB
Mute attenuation	Output code with 0.63 Vrms sine wave input at 1kHz		0000h		
Input resistance	Only ADC on	15		50	kΩ
	ADC and Sidetone on	8		16	kΩ
Input capacitance			10		pF
HEADSET MICROPHONE BIAS					
Voltage range	D7D8=00 control register 1DH/Page 2		3.3		V
	D7D8=01 control register 1DH/Page 2		2.5		
	D7D8=1X control register 1DH/Page 2		2		
PSRR	217 Hz, 100 mV on AVDD1/2		55		dB
	217 Hz, 100 mV on BVDD		70		
	1020 Hz, 100 mV on AVDD1/2		55		
	1020 Hz, 100 mV on BVDD		70		
Sourcing current			1		mA
HANDSET MICROPHONE BIAS					
Voltage range	D6=0 control register 1DH/Page 2		3		V
	D6=1 control register 1DH/Page 2		2.5		
PSRR	217 Hz, 100 mV on AVDD1/2		55		dB
	1020 Hz, 100 mV on AVDD1/2		55		
Sourcing current			1		mA
DAC INTERPOLATION FILTER					
Pass band		20		0.45Fs	Hz
Pass band ripple			±0.06		dB
Transition band		0.45Fs		0.5501Fs	Hz
Stop band		0.5501Fs		7.455Fs	Hz
Stop band attenuation			65		dB
Filter group delay			21/Fs		Sec
De-emphasis error			±0.1		dB

(1) ADC PSRR measurement is calculated as:

$$PSRR = 20 \log_{10}\left(\frac{VSIG_{sup}}{V_{ADCOUT}}\right)$$

where $VSIG_{sup}$ is the ac signal applied on AVDD, which is 100 mV_{PP} at 1 kHz, and

$$V_{ADCOUT} = \frac{\text{Amplitude of Digital Output}}{\text{Max Possible Digital Amplitude}}$$

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

At +25°C, AVDD1, AVDD2, DRVDD, IOVDD = 3.3 V, BVDD = 3.9 V, DVDD = 1.8 V, V_{ref} = 2.5 V, Fs (Audio) = 48 kHz, unless otherwise noted (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DAC HEADPHONE OUTPUT	Load = 16 Ω (single-ended), 50 pF				
Full-scale output voltage (0dB)			0.848		Vrms
Output common mode			1.5		V
SNR	Measured as idle channel noise, A-weighted		90		dBA
THD	–1 dBFS Input, 0-dB gain		–65		dB
PSRR	217 Hz, 100 mV on AVDD1/2(1)		55		dB
	1020 Hz, 100 mV on AVDD1/2(1)		55		dB
Interchannel isolation	Coupling from ADC to DAC		80		dB
Mute attenuation			90		dB
Maximum output power	Per channel		35		mW
Digital volume control		–63.5		0	dB
Digital volume control step size			0.5		dB
Channel separation	Between SPK1 and SPK2		–75		dB
DAC SPEAKER OUTPUT	Load = 8 Ω (differential), 50 pF				
Full-scale output voltage (0 dB)			1.838		Vrms
Output common mode			1.75		V
SNR	Measured as idle channel noise, A-weighted		95		dBA
THD	–1 dBFS Input, 0-dB gain		–65		dB
PSRR	217 Hz, 100 mV on AVDD1/2		70		dB
	217 Hz, 100 mV on BVDD		70		
	1020 Hz, 100 mV on AVDD1/2		70		
	1020 Hz, 100 mV on BVDD		70		
Interchannel isolation	Coupling from ADC to DAC		90		dB
Mute attenuation			90		dB
Maximum output power			335		mW
CELLPHONE					
MIC INPUT TO CPOUT	1020-Hz Sine wave input on MICIN_HND, load on CP_OUT = 10 kΩ, 50 pF				
Full-scale input voltage (0 dB)			0.707		Vrms
Input common mode			1.5		V
Full-scale output voltage (0 dB)			0.707		Vrms
Output common mode			1.5		V
SNR	Measured as idle channel noise, A-weighted		90		dBA
THD	0 dBFS Input, 0-dB gain		–72		dB
PSRR	217 Hz, 100 mV on AVDD1/2		45		dB
	1020 Hz, 100 mV on AVDD1/2		45		
Interchannel isolation	CP_IN to CP_OUT		75		dB
Mute attenuation	CP_OUT muted		90		dB

(1) DAC PSRR measurement is calculated as:

$$PSRR = 20 \log_{10}\left(\frac{VSIG_{sup}}{V_{SPK1/2}}\right)$$

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

At +25°C, AVDD1, AVDD2, DRVDD, IOVDD = 3.3 V, BVDD = 3.9 V, DVDD = 1.8 V, V_{ref} = 2.5 V, Fs (Audio) = 48 kHz, unless otherwise noted (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CP_IN TO 32Ω RECEIVER (SPK1–OUT32N)	1020-Hz Sine wave input on CP_IN, load on SPK1 – OUT32N = 32 Ω (differential), 50 pF				
Full-scale input voltage (0 dB)			0.707		Vrms
Input common mode			1.5		V
Full-scale output voltage (0 dB)			0.697		Vrms
Output common mode			1.5		V
SNR			95		dBA
THD			–80		dB
PSRR			45		dB
			45		
Interchannel isolation			76		dB
Mute attenuation			90		dB
DIGITAL INPUT / OUTPUT					
Logic family			CMOS		
Logic level: V_{IH}	I_{IH} = +5 µA	0.7xIOVDD			V
V_{IL}	I_{IL} = +5 µA	–0.3		0.3xIOVDD	V
V_{OH}	I_{OH} = 2 TTL loads	0.8xIOVDD			V
V_{OL}	I_{OL} = 2 TTL loads			0.1xIOVDD	V
Capacitive load			10		pF

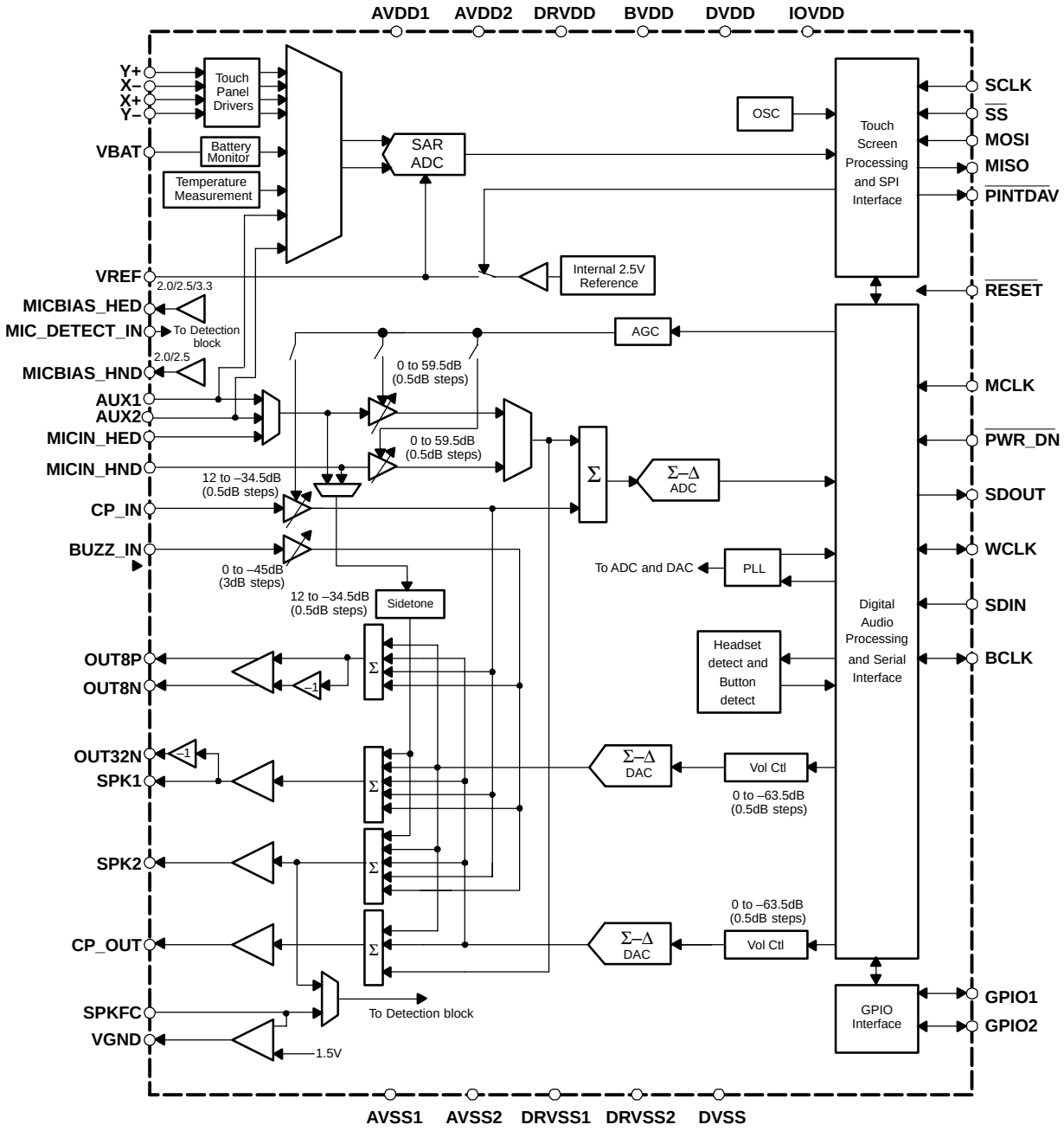
PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

At +25°C, AVDD1, AVDD2, DRVDD, IOVDD = 3.3 V, BVDD = 3.9 V, DVDD = 1.8 V, V_{ref} = 2.5 V, Fs (Audio) = 48 kHz, unless otherwise noted (continued)

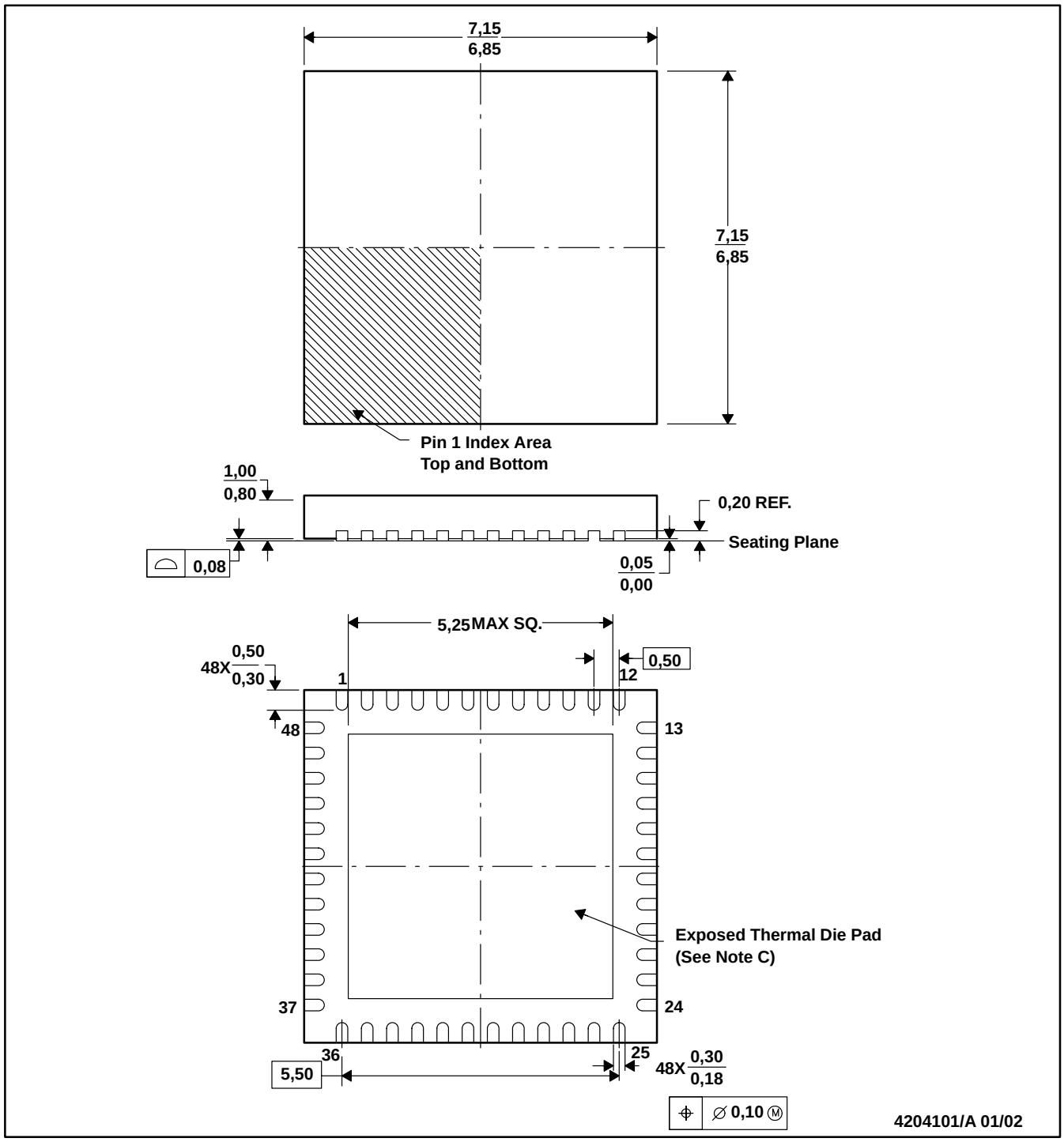
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS					
Power supply voltage					
AVDD1, AVDD2		3	3.3	3.6	V
DRVDD		3	3.3	3.6	V
BVDD		3.5		4.2	V
IOVDD	Max MCLK = 100 MHz	2		3.6	V
	Max MCLK = 50 MHz	1.1		3.6	V
DVDD		1.65	1.8	1.95	V
Touch-screen ADC quiescent current	IAVDD1, host controlled AUX1 conversion at 10 ksps with external reference		55		µA
	IDVDD, host controlled AUX1 conversion at 10 ksps		100		
Analog supply current – audio play back only	IAVDD1 with loudspeaker output (no signal), PLL off		2.4		mA
	IBVDD with loudspeaker output (no signal), PLL off		7.8		
	IAVDD1 with headphone output (no signal), VGND off, PLL off		2.2		
	IDRVDD with headphone output (no signal), VGND off, PLL off		3.1		
Digital supply current – audio play back only	IDVDD, PLL off		2.5		mA
Analog supply current – mic record only	IAVDD1, headset mic, PLL off		4.4		mA
	IBVDD, headset mic, PLL off		1.5		
	IAVDD1, handset mic, PLL off		5.4		
Digital supply current – mic record only	IDVDD, PLL off		1.5		mA
Analog supply current	IAVDD2, PLL on		1.1		mA
Digital supply current	IDVDD, PLL on		0.9		mA
Total current	Hardware power down		10		µA
	Only headset/button detection enabled		50		
	Only auto temperature measurement with 5.59 min delay		40		
	Headset/button detection and auto temperature measurement with 5.59 min delay		65		

FUNCTIONAL BLOCK DIAGRAM



PRODUCT PREVIEW

RGZ (R-PQFP-N48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads, (QFN) package configuration.
D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
E. Falls within JEDEC M0-220.

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