FAIRCHILD SEMICONDUCTOR®

April 2004

# RMPA2451

## 2.4–2.5 GHz GaAs MMIC Power Amplifier

### General Description

Fairchild Semiconductor's RMPA2451 is a partially matched monolithic power amplifier in a surface mount package for use in wireless applications in the 2.4 to 2.5 GHz ISM frequency band. The amplifier may be biased for linear, class AB or class F for high efficiency applications. External matching components are required to optimize the RF performance. The MMIC chip design utilizes our 0.25µm power Pseudomorphic High Electron Mobility (PHEMT) process.

### Features

- 38% power added efficiency
- 29dBm typical output power
- Small package outline: 0.28" x 0.28" x 0.07"
- Low power mode: 0 dBm

### Device


## Absolute Ratings

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| Vd1, Vd2 | Positive Drain DC Voltage | 0 | +8 | V |
| Vg1, Vg2 | Negative Gate DC Voltage | -5 | 0 | V |
| Vd–Vg | Simultaneous Drain to Gate Voltage | | +10 | V |
| $P_{IN}$ | RF Input Power (from 50Ω source) | | +10 | dBm |
| Id1 | Drain Current, First Stage | | 75 | mA |
| Id2 | Drain Current, Second Stage | | 525 | mA |
| Ig | Gate Current | | 5 | mA |
| $T_C$ | Channel Temperature | | 175 | °C |
| $T_{CASE}$ | Operating Case Temperature | -40 | 85 | °C |
| $T_{STG}$ | Storage Temperature Range | -40 | 125 | °C |
| $R_{JC}$ | Thermal Resistance (Channel to Case) | | 33 | °C/W |

## Electrical Characteristics[1]

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Frequency Range | 2400 | | 2500 | MHz |
| Gain[1] | 28.5 | 33 | | dB |
| Output Power, P1dB[1] | 27 | 29 | | dBm |
| Power Added Efficiency | | 38 | | % |
| 3rd order Intermod. Product[2] | | -35 | -27 | dBc |
| Drain Current (Id1 + Id2) | | 430 | | mA |
| Gate Current (Ig1 + Ig2) | | | 5 | mA |
| Input Return Loss (50W) | | 2:1 | | dB |
| Low Power Mode, Pout[3] | 0 | | | dBm |

**Notes:**
1. Production Testing includes Gain, Output Power at1-dB gain compression (P1dB) and Input Return Loss at Vd1 = Vd2 = +5.0; Vg1, Vg2 = -0.5V (nominal), adjust Vg1 and Vg2 to get Idq1 = 60mA, Idq2 = 340mA and at F = 2.45GHz, at 25°C.
2. Two tone 3rd order Output Intermodulation products (IM3) are measured with total output power level of 25dBm (tone spacing is 1MHz).
3. Vg1, Vg2 tied together. Vd = 5V until Idq total = 45 mA, Pin = -10dBm.

Other Parameters are guaranteed by Design Validation Testing (DVT)

## Application Information

**CAUTION: THIS IS AN ESD SENSITIVE DEVICE.**

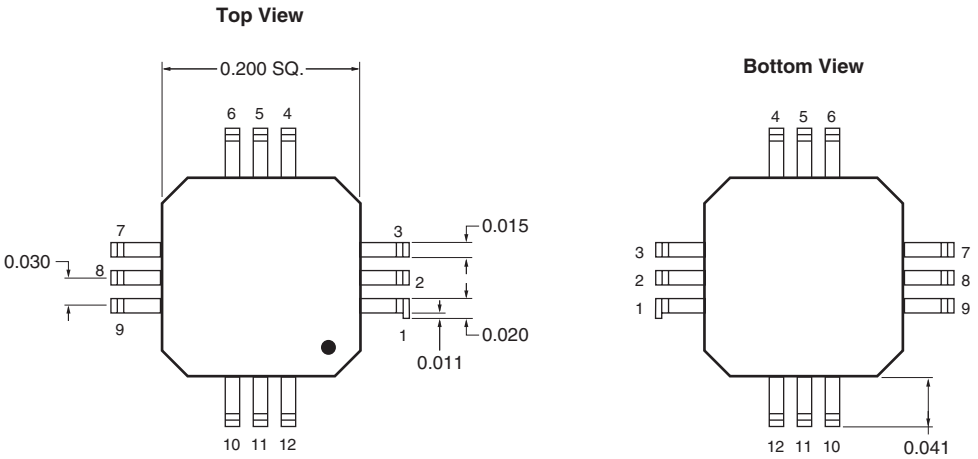
The following describes the procedure for evaluating the RMPA2451, a partially-matched PHEMT monolithic power amplifier which has been designed for wireless applications in the 2.4 - 2.5 GHz ISM band, in a surface mount package. The package outline, along with the pin designations, is provided as Figure 1. The functional block diagram of the packaged product is provided as Figure 2.

It should be noted that the RMPA2451 requires the use of external passive components to form the DC bias and RF output matching circuits. The schematic for a recommended DC bias / RF matching circuit is shown in Figure 3, along with a list of the appropriate components. Figure 4 illustrates the layout of an evaluation board based on this schematic (RMPA2451-TB).

Figures 5 and 6 illustrate typical device performance. This data for various operating parameters was obtained across the design bandwidth over a range of temperatures.

Figure 5 shows the variation in Gain and P1dB with temperature and operating frequency.

Figure 6 shows the 3rd-order intermodulation product measured at different total output power levels.




| Pin | Description |
|---|---|
| 1 | Vd2 + RF Out |
| 2 | Vd2 + RF Out |
| 3 | Vd2 + RF Out |
| 4 | GND |
| 5 | Vd1 |
| 6 | GND |
| 7 | GND |
| 8 | RF IN |
| 9 | GND |
| 10 | Vg1 |
| 11 | Vg2 |
| 12 | GND |
| Base | GND |

Dimensions in inches

**Figure 1. Package Information**

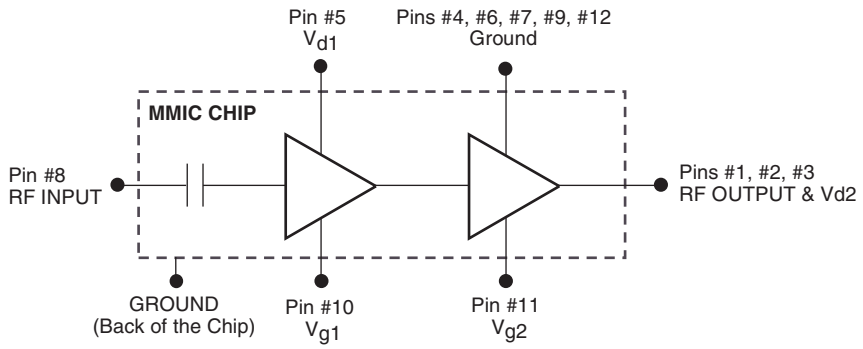



**Figure 2. Functional Block Diagram**

## Test Procedure for the Evaluation Board (RMPA2451-TB)

It is important that the following points be noted prior to testing; Pin designations are as shown in Figure 2 and 4.

- $V_{gg1}$ and $V_{gg2}$ are the negative Gate bias voltages applied at the pins of the evaluation test board.
- $V_{dd1}$ and $V_{dd2}$ are the positive Drain bias voltages applied at the pins of the evaluation test board.
- $V_{g1}$ and $V_{g2}$ are the negative Gate bias voltages applied at the pins of the package.
- $V_{d1}$ and $V_{d2}$ are the positive Drain bias voltages applied at the pins of the package.

**CAUTION: LOSS OF GATE VOLTAGES (VG1, VG2) WHILE DRAIN VOLTAGES (VD1, VD2) ARE PRESENT MAY DAMAGE THE AMPLIFIER.**

The following sequence of procedures must be followed to properly test the amplifier:

**Step 1:** Turn the RF power OFF.

**Step 2:** Use the GND terminals of the evaluation board for the ground of the DC supplies.

**Step 3:** Apply a nominal voltage of approximately - 3.0V to both $V_{gg1}$ and $V_{gg2}$ terminals.

**Step 4:** Apply a nominal voltage of +5.0V to the $V_{dd}$ terminals. Adjust $V_{gg2}$ to provide a second stage quiescent Drain current, $I_{dd2}$, of 340 mA. Adjust $V_{gg1}$ to give a first stage quiescent Drain current, $I_{d1}$ of 60mA.

**Step 5:** Apply an RF signal within the ISM frequency range (2.4 - 2.5 GHz) at an initial input power level of -10 dBm.

**Step 6:** To perform intermodulation product measurements, a second RF signal generator with a frequency difference of 1 MHz is required, along with an appropriate power combiner. The test configuration should allow this additional generator to provide the same input power level as the first generator into the device. Intermodulation readings may then be made at the required total output power levels.

**Step 7:** To operate at lower quiescent Drain currents, increase the magnitudes of $V_{gg1}$ and $V_{gg2}$ as required, alternatively to operate at higher quiescent Drain currents, the magnitudes of $V_{gg1}$ and $V_{gg2}$ should be decreased accordingly.

**Step 8:** When turning the amplifier OFF, the power-up sequence should be reversed.

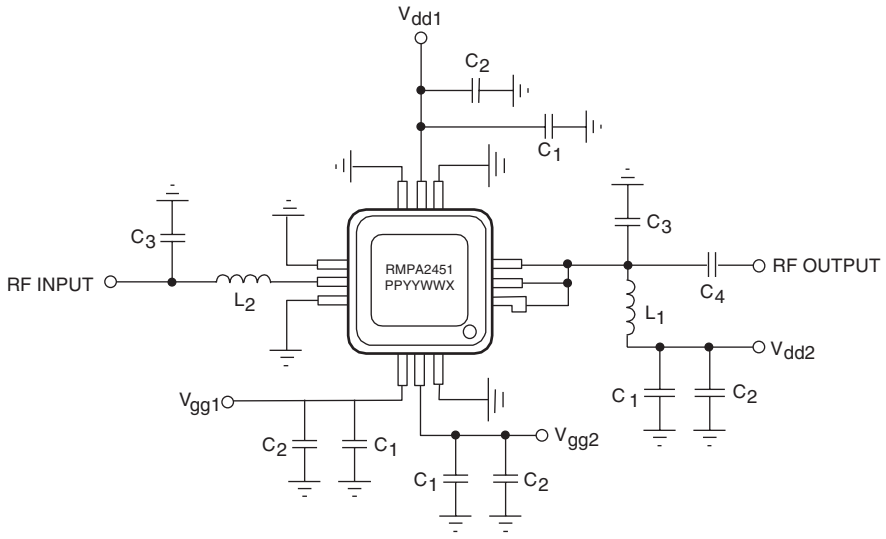
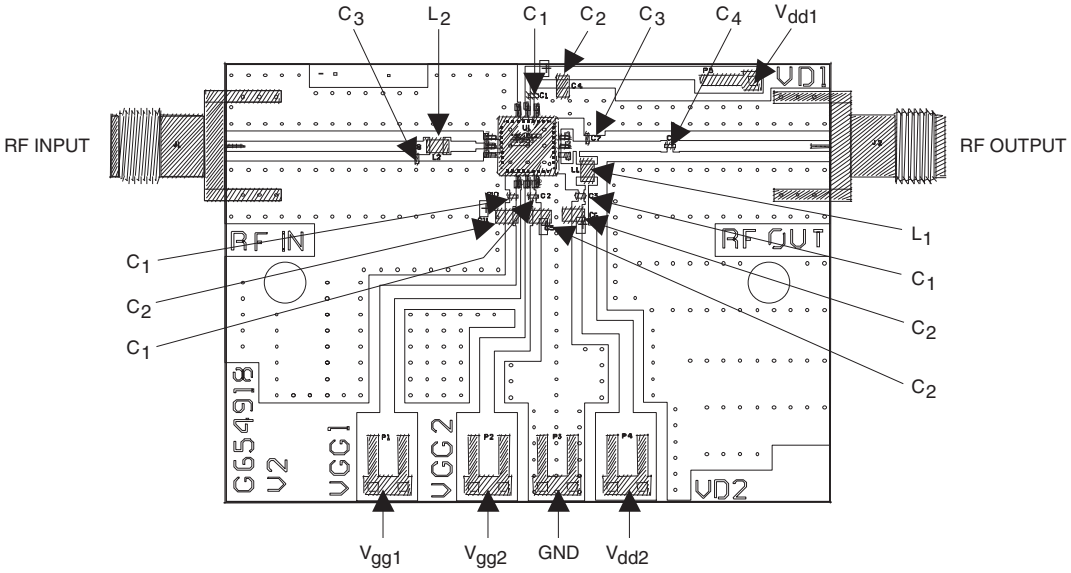



**Figure 3. Schematic of a Recommended DC Bias/RF Matching Circuit**

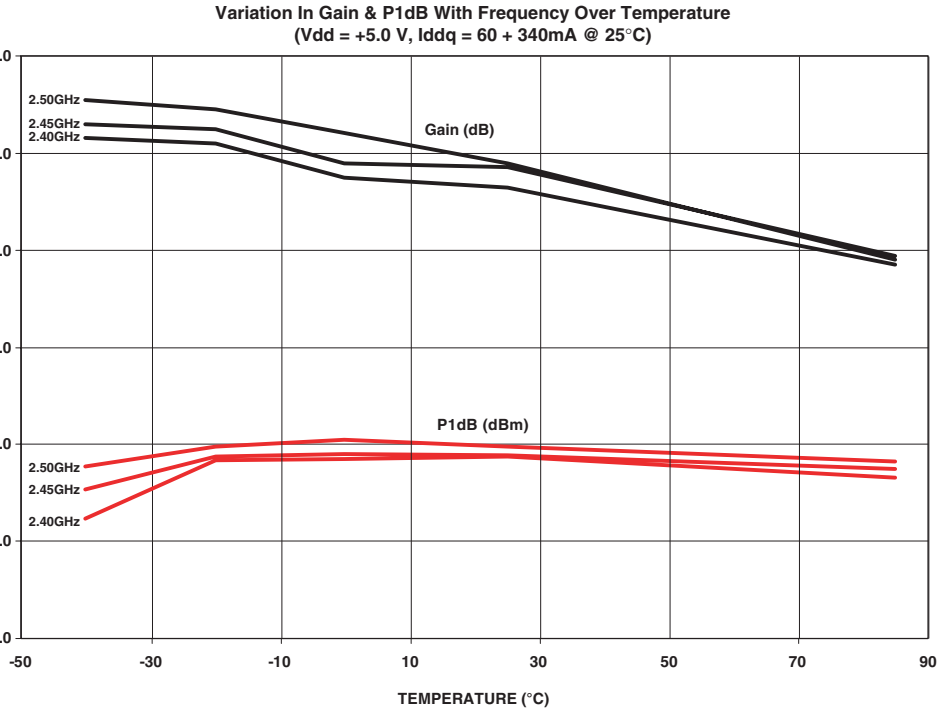



**Parts Lists for Test Evaluation Board**

| Part | Value | Quantity | Supplier | Part Number |
|---|---|---|---|---|
| C1 | 1000pF | 4 | Murata | GRM36X |
| C2 | 2.2µF | 4 | Sprague | 595D225X0016T2T |
| C3 | 1.0pF | 2 | Murata | GRM36COG1R0B050 |
| C4 | 2.0pF | 1 | Murata | GRM36COG2R0B050 |
| L1 | 10.0nH | 1 | Coilcraft | 0805HT10NTKBC |
| L2 | 1.8nH | 1 | Coilcraft | 0805HT1N8TKBC |

**Figure 4. Layout of Evaluation Board (RMPA2451-TB)**

## Typical Characteristics




NB: Gain measured at $P_{in}$ = -10dBm

**Figure 5. Typical Gain and P1dB Performance Across Bandwidth Over Temperature**

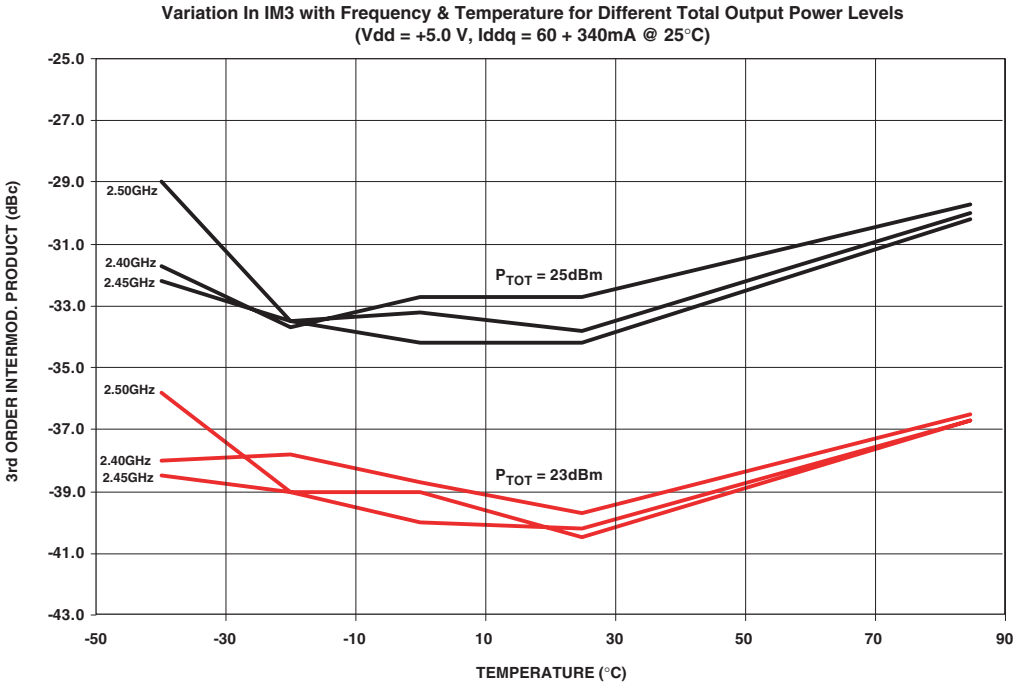



**Figure 6. Typical Third-Order Intermodulation Product Variation Over Temperature**

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