DATA SHEET

SA3601
Low voltage dual-band RF front-end

Preliminary specification

1999 Nov 09

Philips
Semiconductors

PHILIPS

Low voltage dual-band RF front-end SA3601

DESCRIPTION

The SA3601 is an integrated dual-band RF front-end that operates at both cellular (AMPS and TDMA) and PCS (TDMA) frequencies, and is designed in a 20 GHz f_T BiCMOS process—QUBiC2. The low-band (LB) receiver is a combined low-noise amplifier (LNA) and mixer. The LNA has a 1.7 dB noise figure (NF) at 881 MHz with 17 dB of gain and an IIP3 of –7 dBm. The wide-dynamic range mixer has a 9.5 dB NF at 881 MHz with 9.5 dB of gain and an IIP3 of +6 dBm.

The high-band (HB) receiver is a combined low-noise amplifier (LNA) and mixer, with the low-band and high-band mixers sharing the same mixer output. The LNA has a 2.2 dB NF at 1960 MHz with 16 dB of gain and an IIP3 of –5 dBm. The wide-dynamic range mixer has a 8.5 dB NF at 1960 MHz with 8.5 dB of gain and an IIP3 of +5.5 dBm.

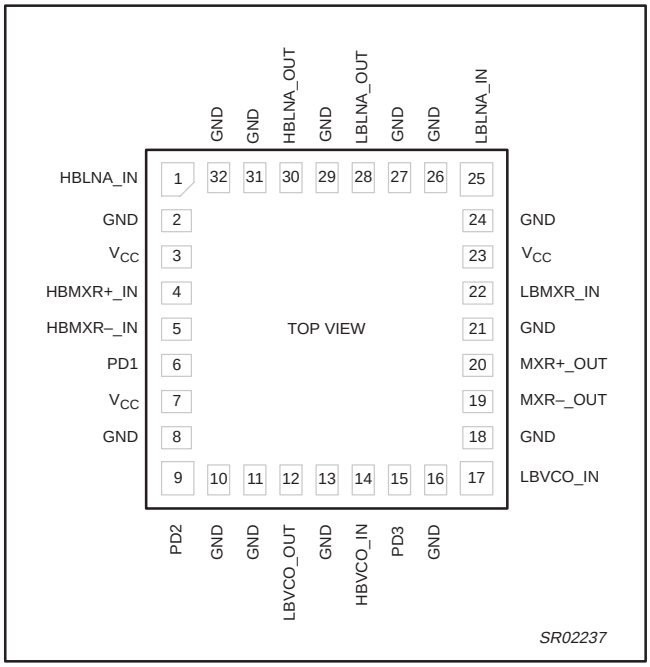
FEATURES

- Low current consumption: LB I_{CC} = 14 mA; HB I_{CC} = 15.5 mA
- Outstanding low- and high-band noise figure
- LNAs with gain control (30 dB gain step)
- LO input and output buffers
- Frequency doubler
- On chip logic for network selection and power down
- Very small outline package

APPLICATIONS

- 800 to 1000 MHz analog and digital receivers
- 1800 to 2000 MHz digital receivers
- Portable radios
- Mobile communications equipment

PIN CONFIGURATION



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA3601	BCC32++	HBCC32: plastic, heatsink bottom chip carrier; 32 terminals; body 5 x 5 x 0.65 mm	SOT560-1

PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	HBLNA_IN	Highband LNA input
2	GND	Ground
3	V_{CC}	Power supply
4	HBMXR+_IN	Highband mixer positive input
5	HBMXR–_IN	Highband mixer negative input
6	PD1	Power down control 1
7	V_{CC}	Power supply
8	GND	Ground
9	PD2	Power down control 2
10	GND	Ground
11	GND	Ground
12	LBVCO_OUT	Lowband VCO buffered output
13	GND	Ground
14	HBVCO_IN	Highband VCO input
15	PD3	Power down control 3
16	GND	Ground

PIN NO.	PIN NAME	DESCRIPTION
17	LBVCO_IN	Lowband VCO input
18	GND	Ground
19	MXR–_OUT	Mixer negative output
20	MXR+_OUT	Mixer positive output
21	GND	Ground
22	LBMXR_IN	Lowband mixer input
23	V_{CC}	Power supply
24	GND	Ground
25	LBLNA_IN	Lowband LNA input
26	GND	Ground
27	GND	Ground
28	LBLNA_OUT	Lowband LNA output
29	GND	Ground
30	HBLNA_OUT	Highband LNA output
31	GND	Ground
32	GND	Ground

BLOCK DIAGRAM

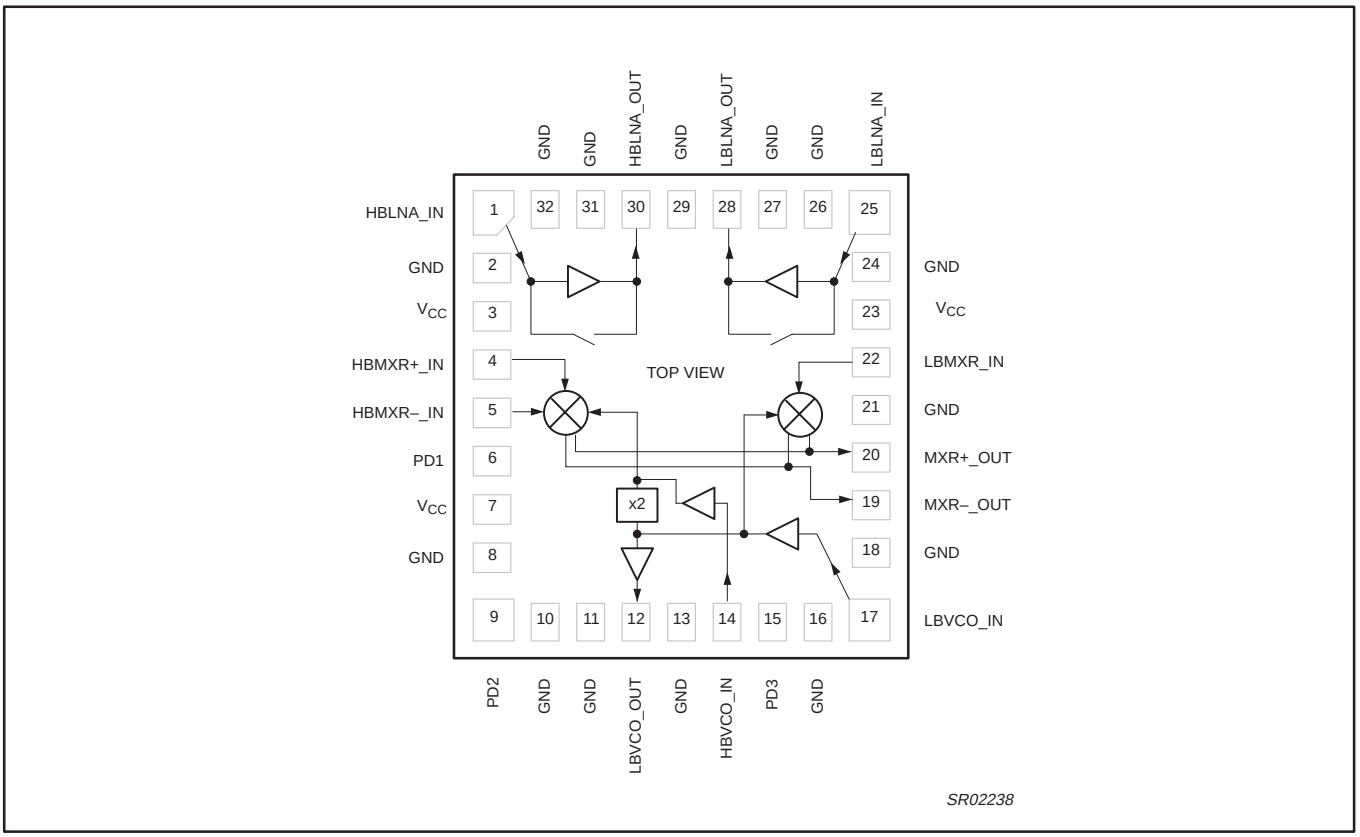


Figure 1. Block Diagram

MODE SELECT LOGIC

PD1	PD2	PD3	OPERATING MODE	Cel LNA	Cel MXR	PCS LNA	PCS MXR	x2 DBL	LB LO O/P	HB LO O/P
0	0	0	Sleep mode	off	off	off	off	off	off	off
0	0	1	Tx mode, LO lowband buffer	off	off	off	off	off	on	off
0	1	0	Rx mode cellular, low gain	off	on	off	off	off	on	off
0	1	1	Rx mode cellular, high gain	on	on	off	off	off	on	off
1	0	0	Rx mode PCS, low gain, x2	off	off	off	on	on	on	off
1	0	1	Rx mode PCS, high gain, x2	off	off	on	on	on	on	off
1	1	0	Rx mode PCS, low gain, no x2	off	off	off	on	off	off	off
1	1	1	Rx mode PCS, high gain, no x2	off	off	on	on	off	off	off

OPERATION

The SA3601 is a highly integrated dual-band radio frequency (RF) front-end integrated circuit (IC) targeted for TDMA applications. This IC is split into separate low-band (LB) and high-band (HB) receivers. The LB receiver contains a low noise amplifier (LNA) and mixer that are designed to operate in the cellular frequency range (869–894MHz). The HB receiver contains an LNA and mixer that are designed to operate in the PCS frequency range (1930–1990 MHz). The SA3601 also contains a frequency doubler that can drive the HB mixer local oscillator (LO) port, allowing a single-band voltage controlled oscillator (VCO) to be used to drive both mixers. Modes for bypassing the doubler are also provided, in the case where a dual-band VCO is used.

The SA3601 has eight modes of operation that control the LNAs, mixers, LO buffers and doubler. The select pins (PD1,2,3) are used to change modes of operation. The internal select logic powers the device down (0,0,0), turns on the LB LO buffer for use in transmit mode (0,0,1), enables cellular receive mode for high and low gain (0,1,X), enables PCS receive mode for high and low gain both without doubler (1,1,X) and with doubler (1,0,X).

Low-Band Receive Section

The LB circuit contains a LNA followed by a wide dynamic range active mixer. In a typical application circuit, the LNA output uses an external pull-up inductor to VCC and is AC coupled. The mixer IF outputs are differential and are combined with the high-band IF mixer outputs thereby eliminating the need for extra output pins. External inductors and capacitors can be used to convert the differential mixer outputs to single-ended. Furthermore, the LNA provides two gain settings: high gain (17dB) and low gain (–15 dB). The desired gain state can be selected by setting the logic pins (PD1,PD2,PD3) appropriately.

High-Band Receive Section

The HB circuit contains a LNA followed by a Gilbert cell mixer with differential inputs. The LNA output uses an internal pull-up inductor to VCC , which eliminates the need for an external pull-up. The mixer IF outputs are differential and are combined with the low-band IF mixer outputs thereby eliminating the need for extra output pins. Similar to the LB LNA, the HB LNA has two gain settings: high gain (16 dB) and low gain (–15 dB).

Control Logic Section

Pins PD1, PD2, and PD3, control the logic functions of the SA3601. The PD1 selects between LB and HB operations. In LB receive mode, the LB LNA is in high gain mode (or on) when PD1,2,3 are (0,1,1). In all other modes, the LB LNA is off. The LB mixer is on when PD1,2,3 are (0,1,X). In all other modes, the LB mixer is off. During transmit mode when PD1,2,3 are (0,0,1), the LB LO buffer is on, enabling use of the LO signal for the transmitter.

In HB receive mode, the HB LNA is in high gain mode (or on) when PD1,2,3 are (1,X,1). In all other modes, the HB LNA is off. The HB mixer is on when PD1,2,3 are (1,X,X), and is off in all other modes. The on-chip frequency doubler (X2) is on in (1,0,X) modes. When the frequency doubler is on, the input signal from the LB LO buffer is doubled in frequency, which can then be used to drive the HB mixer LO port. The frequency doubler can also be bypassed in modes (1,1,X), in which case the HB mixer is driven directly by an external 2 GHz LO signal.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	LIMITS		UNITS
		MIN.	MAX.	
V_{CC}	Supply voltage	–0.3	+4.5	V
V_{IN}	Voltage applied to any other pin	–0.3	V_{CC}+0.3	V
P_D	Power dissipation, T_{amb} = +25 °C (still air)		TBD	mW
$T_{J\ MAX}$	Maximum junction temperature		150	°C
P_{MAX}	Power input/output		+20	dBm
I_{MAX}	DC current into any I/O pin	–10	+10	mA
T_{STG}	Storage temperature range	–65	+150	°C
T_O	Operating temperature	–40	+85	°C

NOTES:
1. IC is protected for ESD voltages up to 500 V (human body model).

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all Input/Output ports are single-ended.

DC PARAMETERS

V_{CC} = +3.0 V, T_{amb} = +25°C; unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS			TESTER LIMITS			UNIT
		PD1	PD2	PD3	MIN	TYP	MAX	
I_{CC}	Sleep mode	0	0	0		0.1	1	µA
	Tx mode, LO lowband buffer	0	0	1		4.3	5.5	mA
	Rx mode cellular, low gain	0	1	0		10.1	12	mA
	Rx mode cellular, high gain	0	1	1		14	16.5	mA
	Rx mode PCS, low gain, x2	1	0	0		17.5	21	mA
	Rx mode PCS, high gain, x2	1	0	1		23.5	28	mA
	Rx mode PCS, low gain, no x2	1	1	0		10	TBD	mA
	Rx mode PCS, high gain, no x2	1	1	1		15.5	TBD	mA
V_{IH}	Input HIGH voltage				0.5xV_{CC}		V_{CC}+0.3	V
V_{IL}	Input LOW voltage				–0.3		0.2xV_{CC}	V
I_{BIAS}	Input bias current	Logic 1 or logic 0			–5		+5	µA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0 V, f_{RF} = 881 MHz, f_{LO} = 963 MHz, T_{amb} = +25°C, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			MIN.	–3 σ	TYP	+3 σ	MAX.	
Cascaded Gain Section								
G_{SYS}	LB LNA + Mixer, High Gain	Filter loss = 3 dB	20.5		23.5		26.5	dB
G_{BYP}	LB LNA + Mixer, Low Gain	Filter loss = 3 dB	–11.5		–8.5		–5.5	dB
Low-band LNA Section								
f_{RF}	RF input frequency range		869				894	MHz
G_{ENA}	Small signal gain ENABLED				17			dB
NF_{ENA}	Noise figure ENABLED				1.7			dB
$IIP3_{ENA}$	Input 3rd order Intercept Point				–7			dBm
$P1dB_{ENA}$	Input 1 dB Compression Point				–20			dBm
G_{BYP}	Small signal gain BYPASSED				–15			dB
NF_{BYP}	Noise figure BYPASSED				15			dB
$IIP3_{BYP}$	Input 3rd order Intercept Point				15			dBm
Z_{IN}	Input return loss	50 Ω system			10			dB
Z_{OUT}	Output return loss	50 Ω system			10			dB
T_{SW}	ENABLE/DISABLE speed[1]						20	µs
Low-band Mixer Section								
f_{RF}	RF input frequency range		869				894	MHz
f_{IF}	IF output frequency range		70				200	MHz
f_{LO}	LO input range		939				1100	MHz
G_{MXR}	Small signal gain	P_{LO} = –5 dBm			9.5			dB
NF_{MXR}	SSB Noise figure	P_{LO} = –5 dBm			9.5			dB
$IIP3_{MXR}$	Input 3rd order Intercept Point	P_{LO} = –5 dBm			6			dBm
$P1dB_{MXR}$	Input 1 dB Compression Point	P_{LO} = –5 dBm			–14			dBm
P_{LO}	LO input power range		–7		–5		–3	dBm
Z_{IN}	Input return loss	50 Ω system			10			dB
Z_{OUT}	Output return loss	50 Ω system			10			dB
2-Tone	Two-tone spurious rejection: $2(f_{RF}–f_{Tx})$, $f_{RF}–f_{Tx}=f_{IF}/2$ $3(f_{RF}–f_{Tx})$, $f_{RF}–f_{Tx}=f_{IF}/3$	P_{LO} = –5 dBm f_{RF}=890.0 MHz @–36 dBm f_{Tx}=848.9 MHz @–20 dBm f_{RF}=876.3 MHz @–36 dBm f_{Tx}=848.9 MHz @–20 dBm			 –110 –110			dBm
RF–LO	RF to LO isolation				25			dB
LO–RF	LO to RF isolation				40			dB
T_{SW}	ENABLE/DISABLE speed[1]						20	µs
Low-band LO Buffer Section								
P_{LO}	LO Input frequency range		939				1100	MHz
P_{IN}	LO Input power	50 Ω matched LB_VCO_IN	–7		–5		–3	dBm
P_{OUT}	LO Output power	50 Ω matched LB_VCO_OUT			–7.5			dBm
Z_{IN}	Input return loss	50 Ω system			10			dB
Z_{OUT}	Output return loss	50 Ω system			10			dB
	Harmonic content	P_{LO} = –5 dBm			–20			dBc
T_{SW}	ENABLE/DISABLE speed[1]						20	µs

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0 V, f_{RF} = 1960 MHz, f_{LO} = 2042 MHz, T_{amb} = +25°C, unless otherwise specified

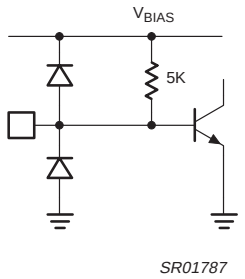
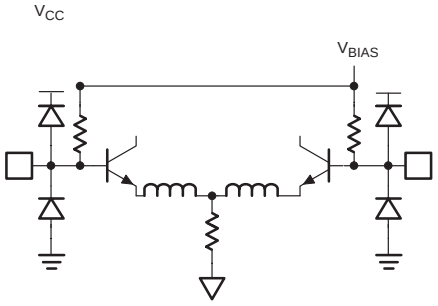
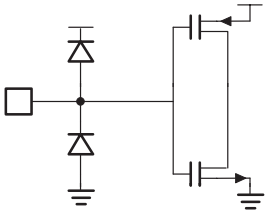
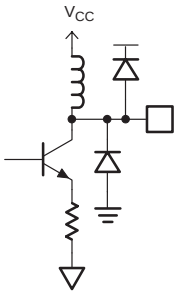
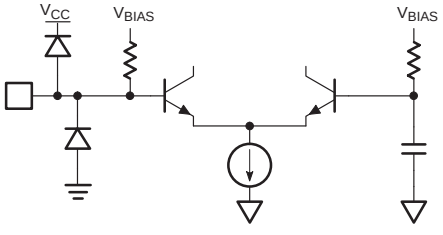
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			MIN.	–3 σ	TYP	+3 σ	MAX.	
Cascaded Gain Section								
G_{SYS}	HB LNA + Mixer, High Gain	Filter loss = 3 dB	18.5		21.5		24.5	dB
G_{BYP}	HB LNA + Mixer, Low Gain	Filter loss = 3 dB	–12.5		–9.5		–6.5	dB
High-band LNA Section								
f_{RF}	RF input frequency range		1930				1990	MHz
G_{ENA}	Small signal gain ENABLED				16			dB
NF_{ENA}	Noise figure ENABLED				2.2			dB
$IIP3_{ENA}$	Input 3rd order Intercept Point				–5			dBm
$P1dB_{ENA}$	Input 1 dB Compression Point				–14			dBm
G_{BYP}	Small signal gain BYPASSED				–15			dB
NF_{BYP}	Noise figure BYPASSED				15			dB
$IIP3_{BYP}$	Input 3rd order Intercept Point				15			dBm
Z_{IN}	Input return loss	50 Ω system, ENA and BYP			10			dB
Z_{OUT}	Output return loss	50 Ω system, ENA and BYP			10			dB
T_{SW}	ENABLE/DISABLE speed[1]						20	µs
High-band Mixer Section								
f_{RF}	RF input frequency range		1930				1990	MHz
f_{IF}	IF output frequency range		70				200	MHz
f_{LO}	LO input range		2000				2190	MHz
G_{MXR}	Small signal gain	P_{LO} = –5 dBm			8.5			dB
NF_{MXR}	SSB Noise figure, doubler off	P_{LO} = –5 dBm			8.5			dB
	SSB Noise figure, doubler on	P_{LO} = –5 dBm			9			dB
$IIP3_{MXR}$	Input 3rd order Intercept Point, doubler off	P_{LO} = –5 dBm			5.5			dBm
	Input 3rd order Intercept Point, doubler on	P_{LO} = –5 dBm			3			dBm
$P1dB_{MXR}$	Input 1 dB Compression Point	P_{LO} = –5 dBm			–14			dBm
IF/2 rej.	Half-IF spurious rejection $2(f_{RF}–f_{LO})$, $f_{RF}–f_{LO}=f_{IF}/2$, doubler off	f_{RF}=1972.0 MHz @–36 dBm f_{LO}=2013.1 MHz @–5 dBm			–90			dBm
	Half-IF spurious rejection $2(f_{RF}–f_{LO})$, $f_{RF}–f_{LO}=f_{IF}/2$, doubler on				–85			
IF/3 rej.	Third-IF spurious rejection $3(f_{RF}–f_{LO})$, $f_{RF}–f_{LO}=f_{IF}/3$	f_{RF}=1985.7 MHz @–36 dBm f_{LO}=2013.1 MHz @–5 dBm			–114			dBm
2-Tone	Two-tone spurious rejection:	P_{LO} = –5 dBm,						dBm
	$f_{RF}–f_{Tx}$, $f_{RF}–f_{Tx}=f_{IF}$	f_{RF}=1933.0 MHz @–36 dBm f_{Tx}=1850.8 MHz @–20 dBm			–70			
	$2(f_{RF}–f_{Tx})$, $f_{RF}–f_{Tx}=f_{IF}/2$	f_{RF}=1951.0 MHz @–36 dBm f_{Tx}=1909.9 MHz @–20 dBm			–115			
	$3(f_{RF}–f_{Tx})$, $f_{RF}–f_{Tx}=f_{IF}/3$	f_{RF}=1937.3 MHz @–36 dBm f_{Tx}=1909.9 MHz @–20 dBm			–125			
P_{LO}	LO input power range		–7		–5		–3	dBm
Z_{IN}	Input return loss	50 Ω system			10			dB
Z_{OUT}	Output return loss	50 Ω system			10			dB
RF–LO	RF to LO isolation				40			dB
LO–RF	LO to RF isolation				30			dB
T_{SW}	ENABLE/DISABLE speed[1]						20	µs

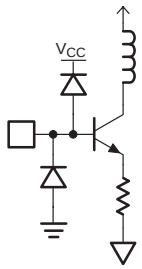
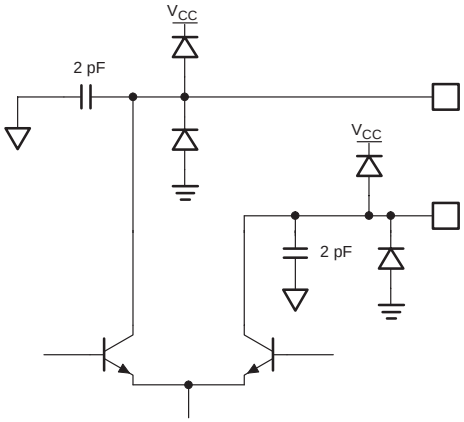
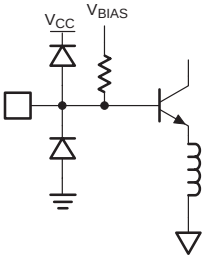
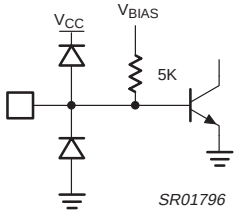
AC ELECTRICAL CHARACTERISTICS

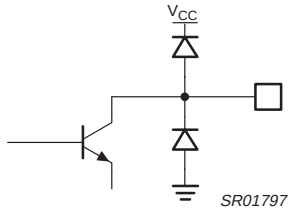
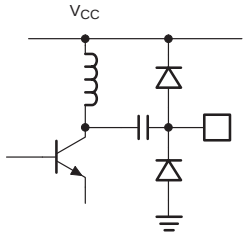
V_{CC} = +3.0 V, T_{amb}= +25°C, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN.	–3 σ	TYP	+3 σ	MAX.	
High-band LO Buffer Section								
P_{LO}	LO Input frequency range		2000				2190	MHz
P_{IN}	LO Input power	50 Ω matched HB_VCO_IN	–7		–5		–3	dBm
P_{OUT}	LO Output power	50 Ω matched HB_VCO_OUT			–8			dBm
Z_{IN}	Input return loss	50 Ω system			10			dB
Z_{OUT}	Output return loss	50 Ω system			10			dB
	Harmonic content	P_{LO} = –5 dBm			–20			dBc
T_{SW}	ENABLE/DISABLE speed[1]						20	µs
x2 LO Doubler Section								
f_{LO}	LO Input frequency		1000				1095	MHz
P_{IN}	LO Input power	50 Ω matched LB_VCO_IN	–7		–5		–3	dBm
Z_{IN}	Input return loss	50 Ω system			10			dB
Z_{OUT}	Output return loss	50 Ω system			10			dB
T_{SW}	ENABLE/DISABLE speed[1]						20	µs

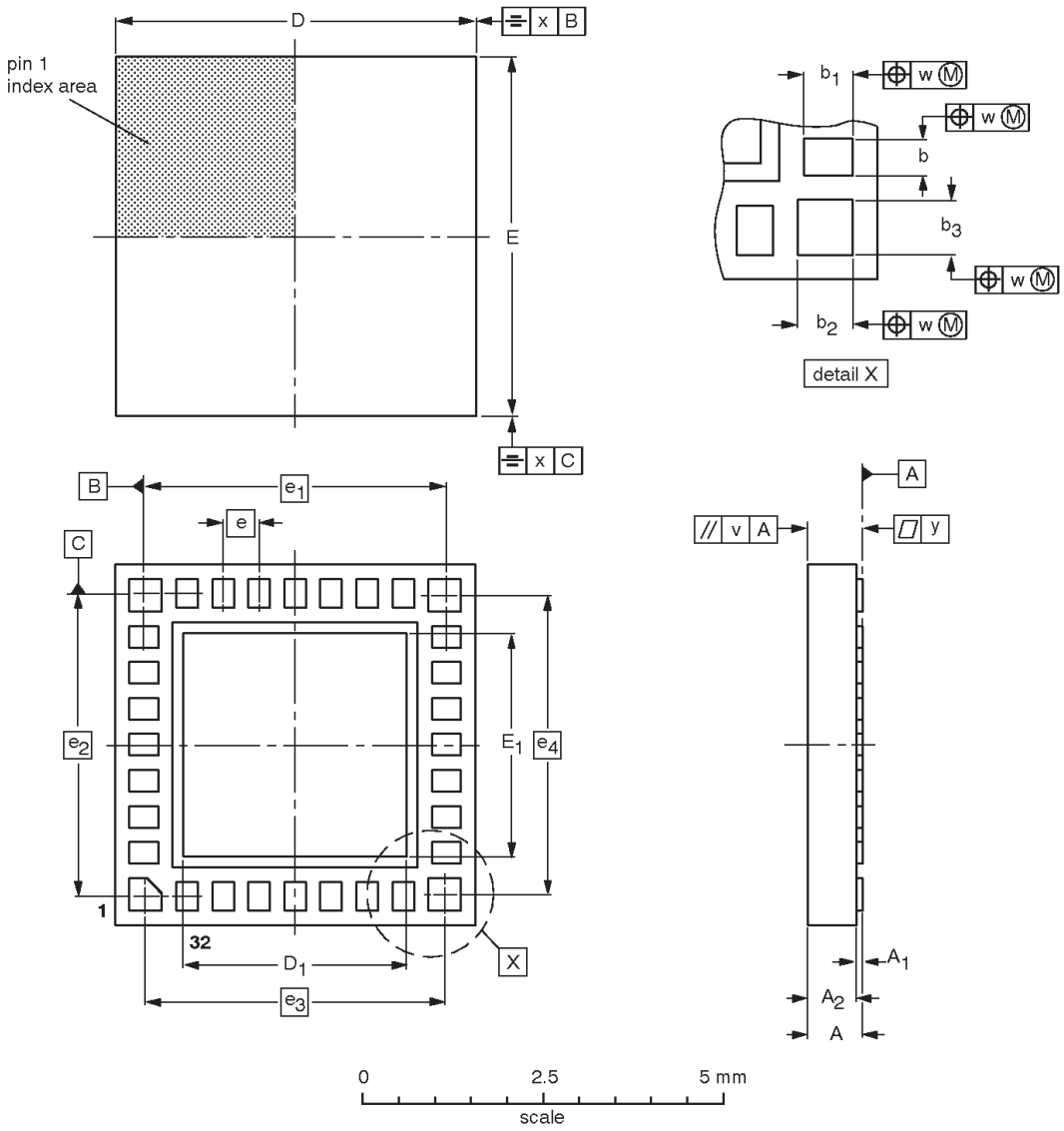
NOTES:
1. Dependent on external components.

PIN NO	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	HB LNA IN	0.8	 SR01787
3, 7, 23	V_{CC}		 SR01788
4	HB MXR+ IN	1.2	
5	HB MXR– IN	1.2	
6	PD1	Apply externally	 SR01789
9	PD2		
15	PD3		
12	LB VCO OUT	V_{CC} – 0.2 V	 SR01791
14	HB VCO IN	1.9	 SR01792

PIN NO	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
17	LB VCO IN	1.0	 *SR01793*
19	MXR– OUT	Pull-up externally to V_{CC}	 *SR01794*
20	MXR+ OUT		
22	LB MXR IN	1.2	 *SR01795*
25	LB LNA IN	0.8	 *SR01796*

PIN NO	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
28	LB LNA OUT	Pull-up externally to V_{CC}	 SR01797
30	HB LNA OUT		 SR01786

HBCC32: plastic, heatsink bottom chip carrier; 32 terminals; body 5 x 5 x 0.65 mm **SOT560-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	b_1	b_2	b_3	D	D_1	E	E_1	e	e_1	e_2	e_3	e_4	v	w	x	y
mm	0.80	0.10 0.05	0.70 0.60	0.35 0.20	0.50 0.30	0.50 0.35	0.50 0.35	5.1 4.9	3.2 3.0	5.1 4.9	3.2 3.0	0.5	4.2	4.2	4.15	4.15	0.2	0.15	0.15	0.05

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT560-1		MO-217				99-09-10

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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