Ordering number : ENA0325

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA75600VA — IF Signal Processing (VIF/SIF) IC for use in TV/VCR Applications

Overview

The LA75600VA is a NTSC intercarrier support VIF/SIF signal-processing IC that makes the minimum number of adjustments possible. The VIF block adopts a technique that makes AFT adjustment unnecessary by adjusting the VCO, thus simplifying the adjustment steps in the manufacturing process. PLL detection is adopted in the FM detector to support multi-format audio detection. A 5V power-supply voltage is used to match that used in most multimedia systems. In addition,these ICs also include a buzz canceller to suppress Nyquist buzz and provide high audio quality.

Functions

- VIF Block :VIF Amplifier, Buzz Canceller, PLL Detector, IF AGC, RF AGC, AFT, Equalizer Amplifier
- SIF Block :Limiter Amplifier, PLL FM detector

Specitications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		6	V
Circuit voltage	V_{13}, V_{17}		V_{CC}	V
Circuit current	I_6		-3	mA
	I_{10}		-10	mA
Allowable dissipation	Pd max	Ta≤70°C *	640	W
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

* Mounted on a board:114.3×76.1×1.6mm^3 glass epoxy board.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5	V
Operating supply voltage	V_{CC} op		4.5 to 5.5	V

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Electrical Characteristics at Ta = 25°C, V_{CC} = 5V, fp = 45.75MHz

Parameter	Symbol	Conditions	No.	Ratings min	Ratings typ	Ratings max	Unit
[VIF block]							
Circuit current	I_5		V1	35	42	52	mA
Maximum RF AGC voltage	$V_{14}H$		V2	V_{CC}-0.5	V_{CC}		V
Minimum RF AGC voltage	$V_{14}L$		V3		0	0.5	V
Input sensitivity	V_i	S1 = OFF	V4	32	38	44	dBμV
AGC range	GR		V5	51	56		dB
Maximum allowable input	V_i max		V6	95	100		dBμV
No-signal video output voltage	V_6		V7	3.1	3.4	3.7	V
Sync. signal tip voltage	V_6tip		V8	0.8	1.1	1.4	V
Video output level	V_O		V9	1.7	2.0	2.3	Vp-p
Black noise threshold voltage	V_{BTH}		V10	0.3	0.5	0.7	V
Black noise clamp voltage	V_{BCL}		V11	1.3	1.6	1.9	V
Video S/N	S/N		V12	48	52		dB
C-S beat	IC-S		V13	38	43		dB
Frequency characteristics	fc	6MHz	V13	-3	-1.5		dB
Differential gain	DG		V15		3.0	6.5	%
Differential phase	DP		V16		3	5	deg
No-signal AFT voltage	V_{13}		V17	2.0	2.5	3.0	V
Maximum AFT voltage	$V_{13}H$		V18	4.0	4.4	5.0	V
Minimum AFT voltage	$V_{13}L$		V19	0	0.18	1.0	V
AFT detection sensitivity	Sf		V20	19	29	38	mV/kHz
VIF input resistance	Ri	45.75MHz	V21		1.5		kΩ
VIF input capacitance	Ci	45.75MHz	V22		3		pF
APC pull-in range (U)	fpu		V23	1.3	2.0		MHz
APC pull-in range (L)	fpl		V24		-2.0	-1.4	MHz
AFT tolerance frequency 1	Δfa1		V25	-150	0	+150	kHz
VCO1 maximum variable range (U)	dfu		V26	1.0	1.5		MHz
VCO1 maximum variable range (L)	dfl		V27		-2.0	-1.5	MHz
VCO control sensitivity	B		V28	1.3	2.7	5.4	kHz/mV
RF AGC input level	V_iRFAGC	R = 5.1kΩ	V29	87	94	101	dBμV
[SIF block]							
Limiting sensitivity	V_{li}(lim)		S1	39	45	51	dBμV
FM detection output voltage	V_O(FM)	4.5MHz ± 25kHz	S2	767	1000	1280	mVrms
AMR	AMR		S3	50	60		dB
Distortion factor	THD	4.5MHz ± 15kHz	S4		0.5	1.0	%
SIF S/N	S/N(FM)		S5	59	64		dB
4.5MHz output level	Vsout	SIF IN 80dBμV	S6	87	94	101	dBμV

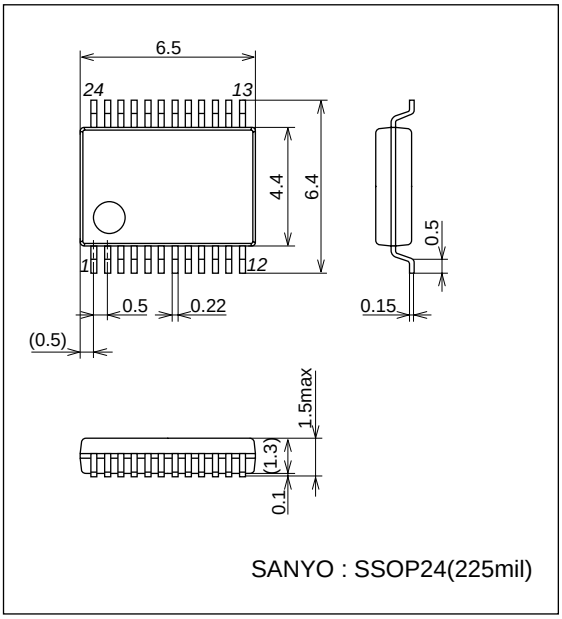
*:If the dynamic range of the FM detection output needs to be widened, connect a resistor and a capacitor in series between pin 23 and GND for level adjustment.

*:The resistor between pin10 and GND must be 470Ω or more.

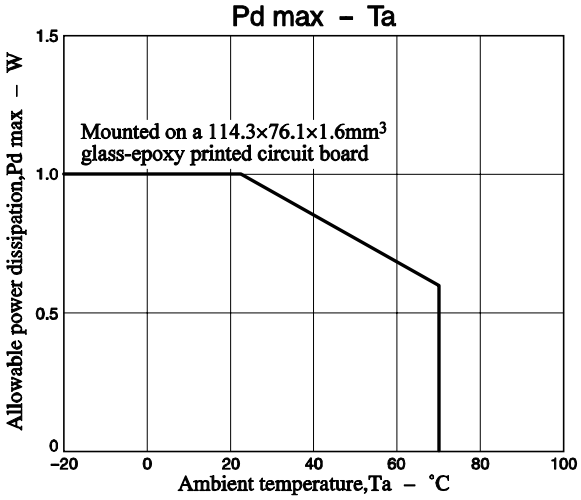
Package Dimensions

unit : mm

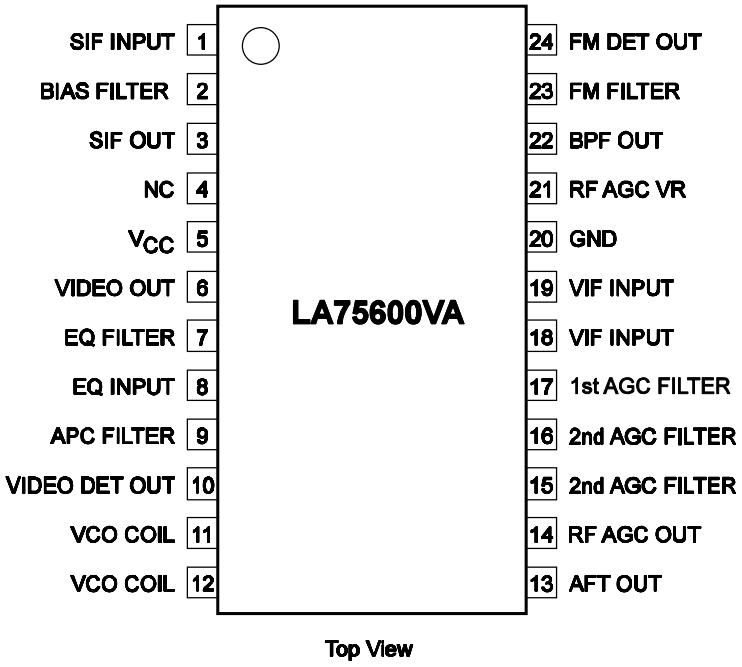
3287



SANYO : SSOP24(225mil)

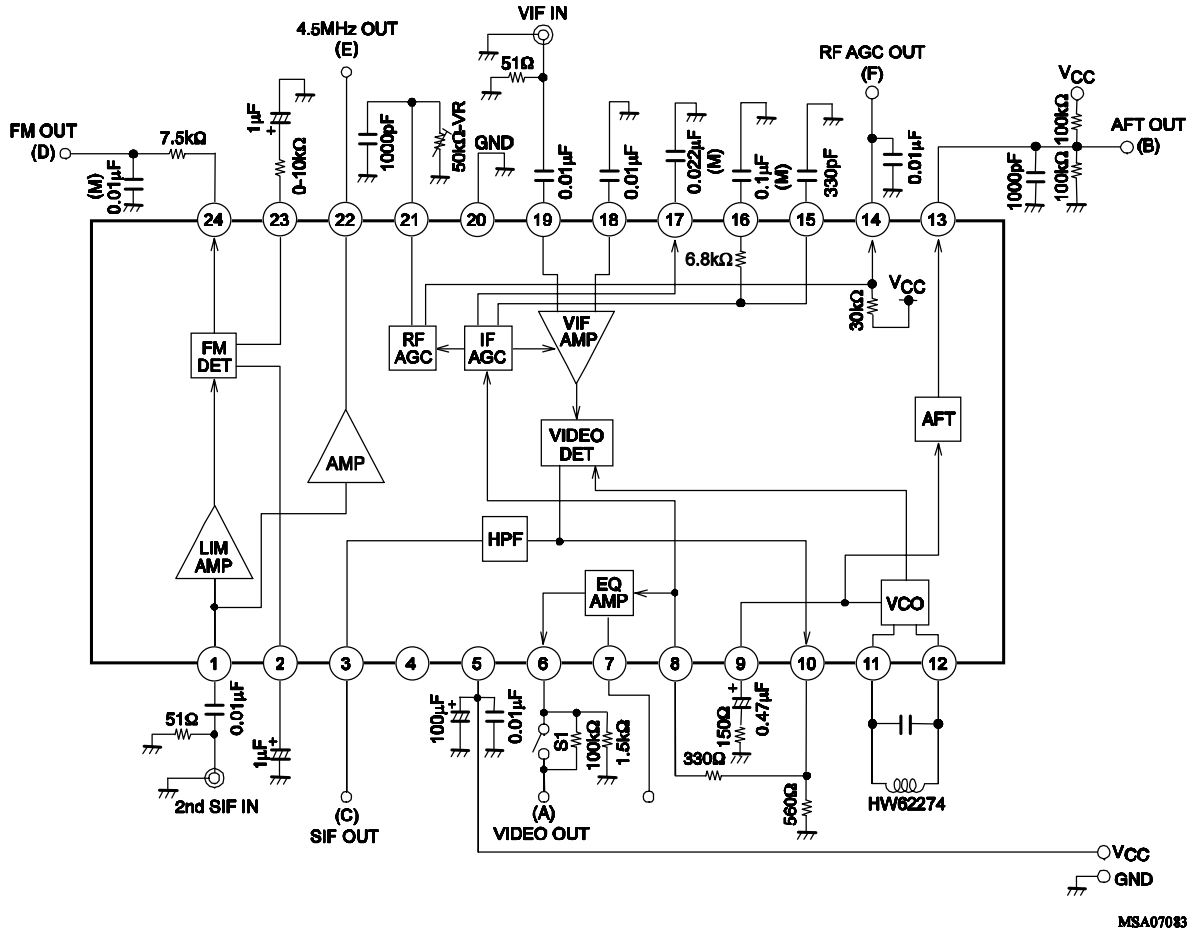


Pin Assignment



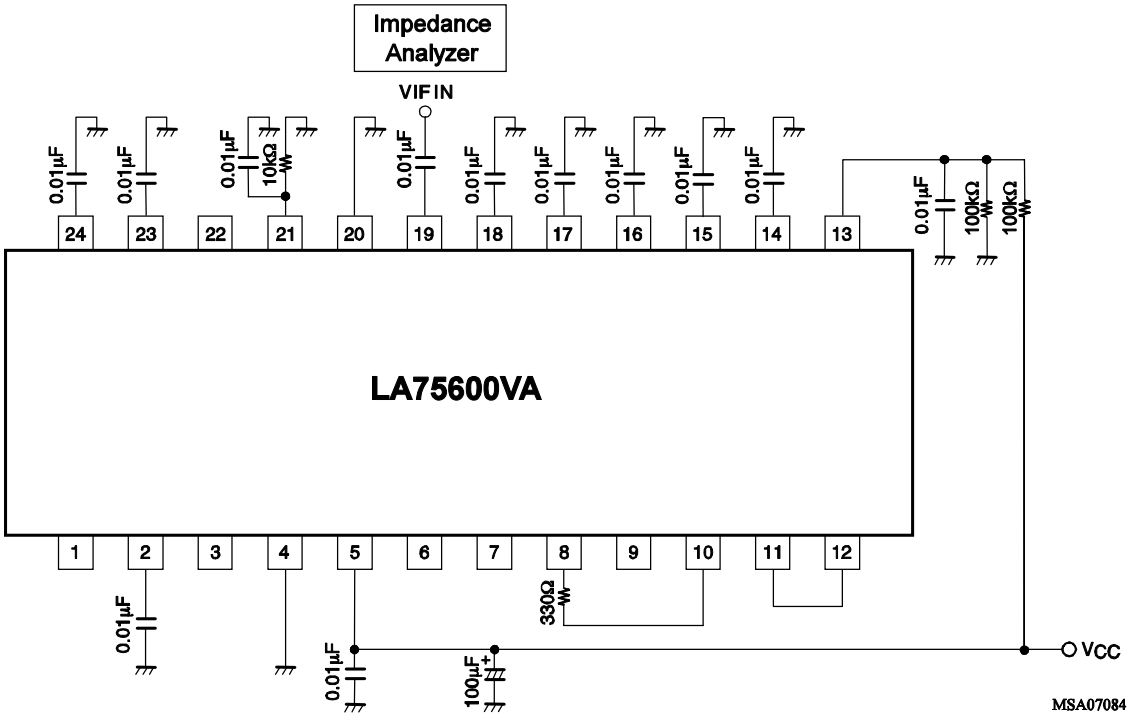
Top View

Block Diagram and AC Characteristics Test Circuit



Test Circuit

Input impedance test circuit (VIF, 1st SIF input impedance)



Test Conditions

V1. Circuit current …… [I_5]

(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) RF AGC Vr MAX
(4) Connect an ammeter to the V_{CC} and measure the incoming current.

V2. V3. Maximum RF AGC voltage, Minimum RF AGC voltage …… [$V_{14}H$, $V1_4L$]

(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) Adjust the RF AGC Vr (resistance value max.) and measure the maximum RF AGC voltage. (F)
(4) Adjust the RF AGC Vr (resistance value min.) and measure the minimum RF AGC voltage. (F)

V4. Input sensitivity …… [V_i]

(1) Internal AGC
(2) fp = 45.75MHz 15kHz 78% AM (VIF input)
(3) Turn off the S1 and put 100kΩ through.
(4) VIF input level at which the 400Hz detection output level at test point A becomes 0.64Vp-p.

V5. AGC range …… [GR]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) In the same manner under the same conditions as for V_4 (input sensitivity), measure the VIF input level at which the detection output level becomes 0.64Vp-p – Vil.

(3) $\mathbf{GR = 20\log \frac{Vil}{Vi}\ dB}$

V6. Maximum allowable input …… [V_i max]

(1) Internal AGC
(2) fp = 45.75MHz 15kHz 78% AM (VIF input)
(3) VIF input level at which the detection output level at test point A becomes video output (V_O) ±1dB.

V7. No-signal video output voltage …… [V_6]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Measure the DC voltage at the VIDEO output (A).

V8. Sync. signal tip voltage …… [V_6tip]

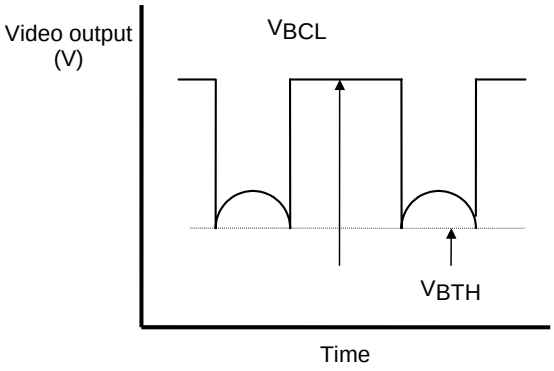
(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) Measure the DC voltage at the VIDEO output (A).

V9. Video output level …… [V_O]

(1) Internal AGC
(2) fp = 45.75MHz 15kHz 78% AM V_i = 10mVrms (VIF input)
(3) Measure the peak value of the detection output level at test point A. (Vp-p)

V10. V11 Black noise threshold level and clamp voltage …… [V_{BTH}, V_{BCL}]

(1) Apply DC voltage to the external AGC, IF AGC (pin 17) and vary it.
(2) fp = 45.75MHz 15kHz 78% AM10mVrms (VIF input)
(3) Adjust the IF AGC (pin 17) voltage to operate the noise canceller.
Measure the VBTH, VBCL at test point A.



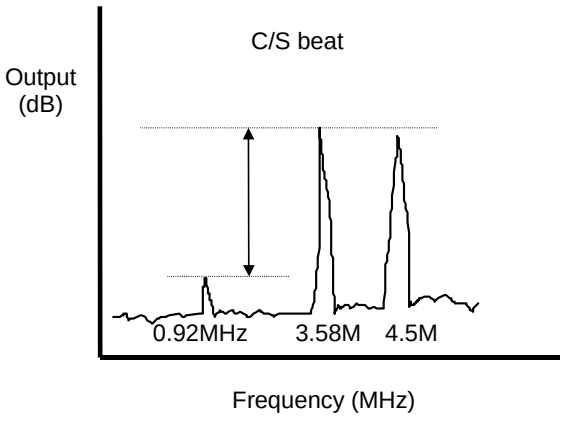
V12. Video S/N …… [S/N]

(1) Internal AGC
(2) fp = 45.75MHz continuous wave = 10mVrms (VIF input)
(3) Measure the noise voltage at test point A in RMS volts through a 10kHz to 4MHz band-pass filter.
……Noise voltage (N)

(4) $S/N = 20\log\frac{\text{Video portion(Vp-p)}}{\text{Nois voltage(Vrms)}} = 20\log\frac{1.12\text{Vp-p}}{\text{Nois voltage}}$ dB

V13. C/S beat …… [IC-S]

(1) Apply DC voltage to the external AGC IF AGC (pin 17) and vary it.
(2) fp = 45.75MHz continuous wave;10mVrms
fc = 42.17MHz continuous wave;10mVrms – 10dB
fs = 41.25MHz continuous wave;10mVrms – 10dB
(3) Adjust the IF AGC (pin 17) voltage so that the output level at test point A becomes 1.3Vp-p.
(4) Measure the difference between the levels for 3.58MHz and 0.92MHz components at test point A.



V14. Frequency characteristics …… [fc]

(1) Apply DC voltage to the external AGC IF AGC (pin 17) and adjust the voltage.
(2) SG1:45.75MHz continuous wave 10mVrms
SG2:45.65MHz to 39.75MHz continuous wave 2mVrms
Add the SG1 and SG2 signals using a T pat and adjust each SG signal level so that the above-mentioned levels are reached, and input the added signals to the VIF IN.
(3) First set the SG2 frequency to 45.65MHz, and then adjust the IF AGC voltage (V17) so that the output level at test point A becomes 0.5Vp-p. ……V1
(4) Set the SG2 frequency to 39.75MHz and measure the output level. ……V2
(5) Calculate as follows: $\mathbf{fc = 20\log\frac{V2}{V1}\ dB}$

V15. V16. Differential gain, Differential phase …… [DG, DP]

(1) Internal AGC
(2) fp = 45.75MHz APL50% 87.5% modulation video signal V_i = 10mVrms
(3) Measure the DG and DP at test point A

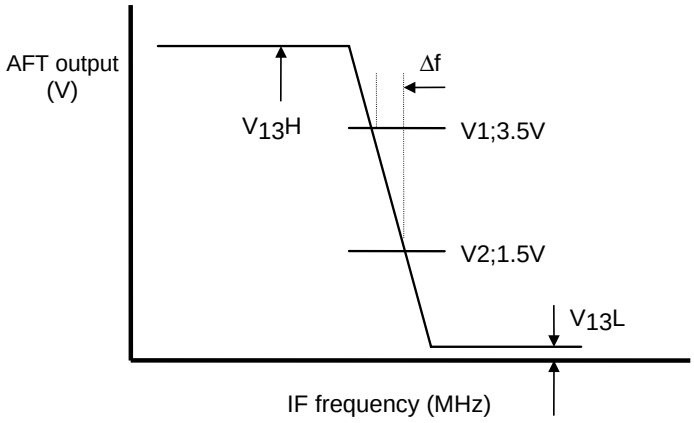
V17. No-signal AFT voltage …… [V_{13}]

(1) Internal AGC
(2) Measure the DC voltage at the AFT output (B).

V18.V19.V20 Maximum minimum AFT output voltage, AFT detection sensitivity …… [V_{13}H, V_{13}L, Sf]

(1) Internal AGC
(2) fp = 45.75MHz ±1.5MHz Sweep = 10mVrms (VIF input)
(3) Maximum voltage …… V10H, minimum voltage …… V10L
(4) Measure the frequency deviation at which the voltage at test point VB changes from V1 to V2 …… Δf

$$\mathbf{Sf = \frac{2000(mV)}{\Delta f(kHz)}\ mV/kHz}$$



V21.V22 VIF input resistance, Input capacitance …… [Ri, Ci]

(1) Referring to the input impedance Test Circuit, measure Ri and Ci with an impedance analyzer.

V23.V24 APC pull-in range …… [fpu, fpl]

(1) Internal AGC
(2) fp = 39MHz to 51MHz continuous wave ; 10mVrms
(3) Adjust the SG signal frequency to be higher than fp = 45.75MHz to bring the PLL to unlocked state.
Note; The PLL is assumed to be in unlocked state when a beat signal appears at test point A.
(4) When the SG signal frequency is lowered, the PLL is brought to locked state again. …… f1
(5) Lower the SG signal frequency to bring the PLL to unlocked state.
(6) When the SG signal frequency is raised, the PLL is brought to locked state again. …… f2
(7) Calculate as follows:

fpu = f1 – 45.75MHz
fpl = f2 – 45.75MHz

V25. AFT tolerance frequency 1 …… [Δfa1]

(1) Internal AGC
(2) SG1:43.75MHz to 47.75MHz variable continuous wave 10mVrmns
(3) Adjust the SG1 signal frequency so that the AFT output DC voltage (test point B) becomes 2.5V; that SG1 signal frequency is f1.
(4) External AGC (Adjust the V_{17}.)
(5) Apply 9V to the IFAGC (pin 17) and then pick up the VCO oscillation frequency from the GND, etc.; that frequency is f2.
(6) Calculate as follows: AFT tolerance frequency Δfa1 = f2 – f1 (kHz)

V26.V27 VCO Maximum variable range (U, L) …… [dfu, dfl]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so that the frequency becomes 45.75MHz.
(3) fl is taken as the frequency when 1V is applied to the APC pin (pin 9). In the same manner, fu is taken as the frequency when 5V is applied to the APC pin (pin 9).

dfu = fu – 45.75MHz
dfl = fl – 45.75MHz

V28. VCO control sensitivity …… [β]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so that the frequency becomes 45.75MHz.
(3) f1 is taken as the frequency when 2.8V is applied to the APC pin (pin 9). In the same manner, f2 is taken as the frequency when 3.0V is applied to the APC pin (pin 9).

$$\beta = \frac{f2 - f1}{400} \text{ kHz/mV}$$

V29. RF AGC input level …… [V_iRFAGC]

(1) Internal AGC.
(2) fp = 45.7MHz continuous wave (VIF input)
(3) Measure the input level at which the pin 14 voltage becomes 2.5V with the RF AGC resistance (pin 21 to GND) being 5.1kΩ.

S1. SIF limiting sensitivity …… [Vi(lim)]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) fs = 4.5MHz fm = 400Hz Δf = ±25kHz (SIF input V_i = 100mVrms)
(3) Set the SIF input level to 100mVrms and measure the level attest point D. ……V_1
(4) Lower the SIF input level and measure the input level that becomes V_1 – 3dB.

S2.S4 FM detection output voltage, Distortion factor …… [V_O(FM), THD]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) fs = 4.5MHz fm = 400Hz Δf = ±25kHz (SIF input)
(3) Measure the FM detection output voltage and the distortion rate at test point D.

S3. AM rejection ratio …… [AMR]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) fs = 4.5MHz fm = 400Hz AM = 30% (SIF input V_i = 100mVrms)
(3) Measure the output level at test point D. ……VAM

(4) $\mathbf{AMR = 20\log \frac{V_{O(DET)}}{VAM}\ dB}$

S5. SIF S/N …… [S/N]

(1) External AGC ($V_{17} = V_{CC}$).
(2) fs = 4.5MHz NO MOD V_i = 100mVrms
(3) Measure the output level at test point D. ……Vn

(4) $\mathbf{S/N = 20\log \frac{V_{O(DET)}}{Vn}\ dB}$

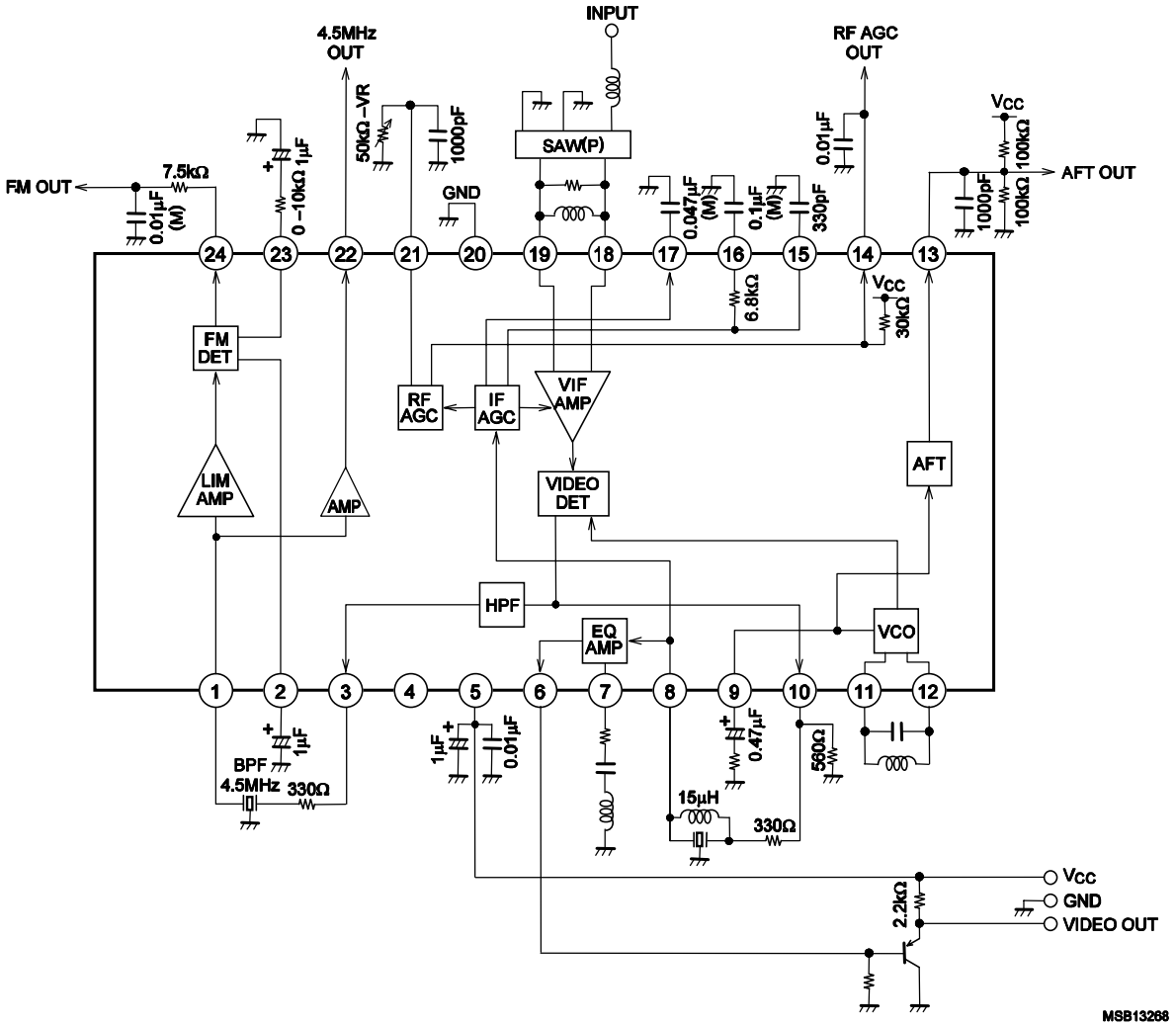
S6. 4.5MHz output level …… [Vsout]

(1) External AGC ($V_{17} = V_{CC}$).
(2) fs = 4.5MHz NO MOD V_i = 10mVrms
(3) Measure the output level at test point E. ……Vsout

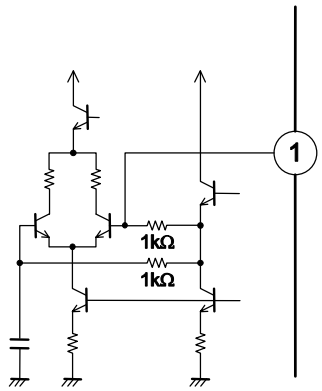
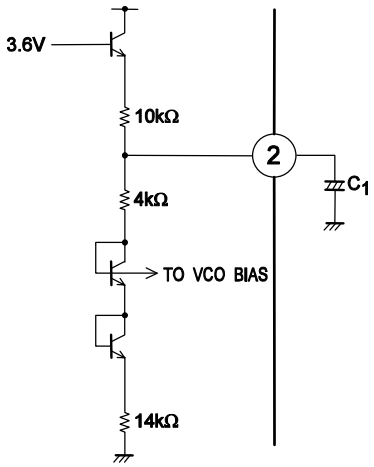
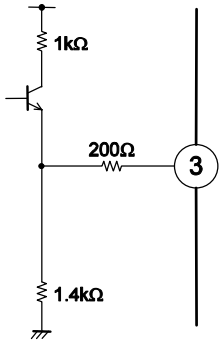
Note 1) Unless otherwise specified for VIF test, apply the V_{CC} voltage to the IF AGC and adjust the VCO coil so that oscillation occurs at 45.75MHz.
Note 2) Unless otherwise specified, turn ON the SW1.

Sample Application Circuit

NT INTER



Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	SIF INPUT	SIF input. The input impedance is about 1kΩ. Since interference signals* entering this input can result in buzzing and beat signals, the pattern layout for the signal input to this pin must be designed carefully. *: Signals that can interfere with audio include video and chrominance signals. Thus the VIF carrier signal can cause interference.	
2	BIAS FILTER	The FM detector signal-to-noise ratio can be improved by inserting a filter in the FM detector bias line. C1 must be 0.47μF or higher, and we recommend 1μF. If the FM detector is not used, a 2 kΩ resistor must be inserted between pin 2 and ground. This stops the FM detector VCO circuit.	
3	SIF OUT	Outputs the intercarrier detector output that has been passed through a high-pass filter. (4.5MHz output)	
4	NC	This pin should be left open.	
5	V_{CC}	Use lines that are as short as possible for V_{CC} / ground decoupling.	

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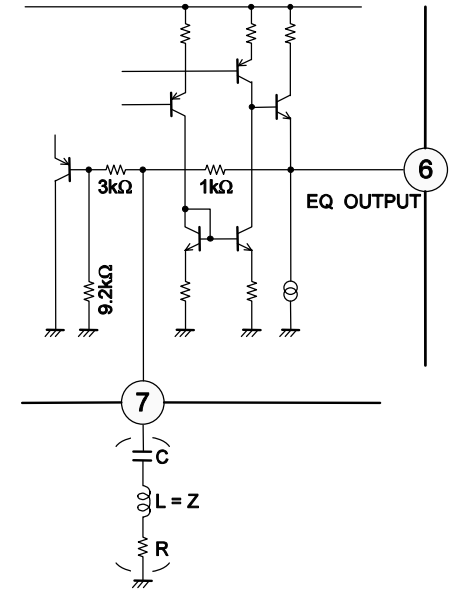
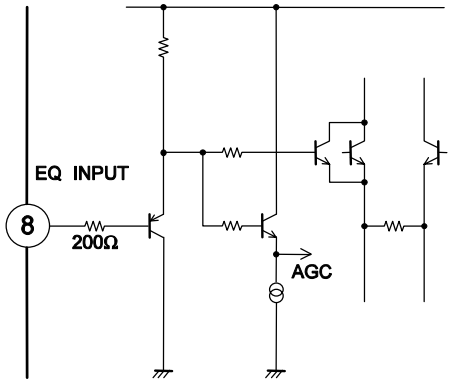
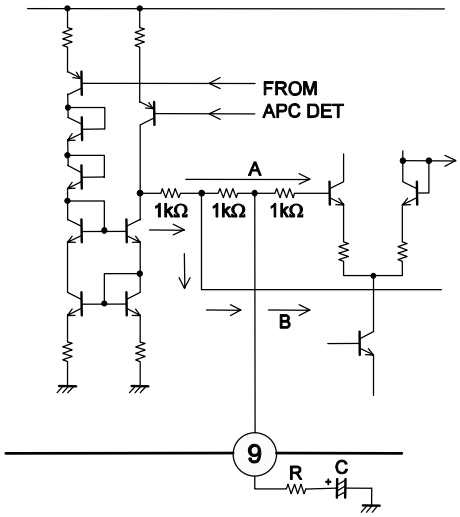
Pin No.	Pin name	Function	Equivalent circuit
6 7 8	VIDEO OUT EQ FILTER EQ INPUT	Equalizer circuit. This circuit corrects the frequency characteristics of the video signal. Pin 8 is the input to the EQ amplifier. The EQ amplifier takes a 1.5Vp-p video signal as its input and amplifies that to a 2.0Vp-p level. • Notes on the equalizer amplifier design. The equalizer amplifier is designed as a voltage follower amplifier with a gain of about 2.3dB. If frequency characteristics correction is required, insert the capacitor, inductor, and resistor between pin 7 and ground in series. • Using the equalizer amplifier. If the input signal is Vi and the output signal Vo, then $\frac{R1}{Z}+1\ (Vi-Vin) = Vo \times G$ G: Gain of the voltage follower amplifier Vin: Imaginary voltage G: About 2.3 dB Assuming Vin ≈ 0, then AV will be: $AV = \frac{Vo \times G}{Z} = \frac{R1}{Z}+1$ R1 is an IC internal 1kΩ resistor. Simply select a value of Z according to the desired characteristics. However, note that the equalizer amplifier gain will be a maximum at the Z resonance, so care is required to prevent distortion from occurring.	 
9	APC FILTER	PLL detector APC filter connection. The APC time constant is switched internally by the IC. When locked, the VCO is controlled by the route A, and the gain is reduced. When unlocked or during weak field reception, the VCO is controlled by the route B, and the gain is increased. We recommend the following values for this APC filter: R = 150 to 390Ω C = 0.47μF	

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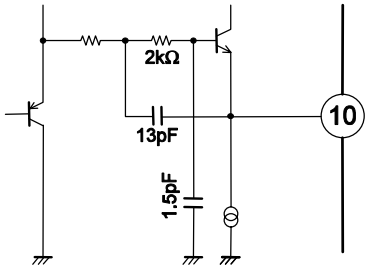
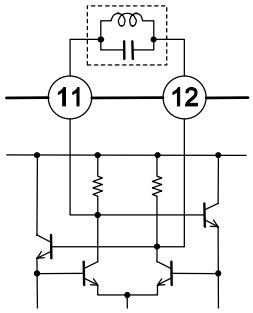
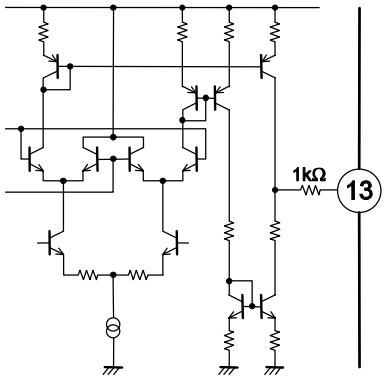
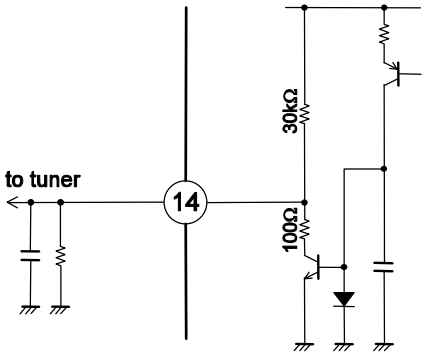
Pin No.	Pin name	Function	Equivalent circuit
10	VIDEO DET OUT	Outputs a video signal that includes the SIF carrier. A resistor must be inserted between pin 10 and ground to acquire adequate drive capability. R ≥ 470Ω	
11 12	VCO COIL VCO COIL	VCO tank circuit for video detection. This VCO is a vector synthesis VCO circuit.	
13	AFT OUT	AFT output. This circuit includes a function that controls the AFT voltage so that it naturally goes to the center voltage during weak field reception.	
14	RF AGC OUT	RF AGC output. This output controls the tuner RF AGC. The internal circuit includes both a 30kΩ pull-up resistor and a 100Ω protective resistor. Determine the value of the external bleeder resistor to match the specifications of the tuner.	

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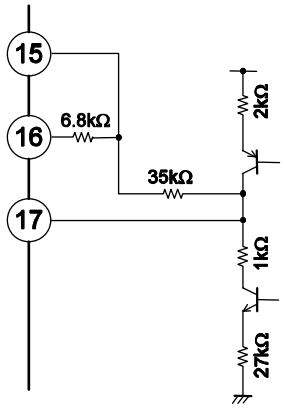
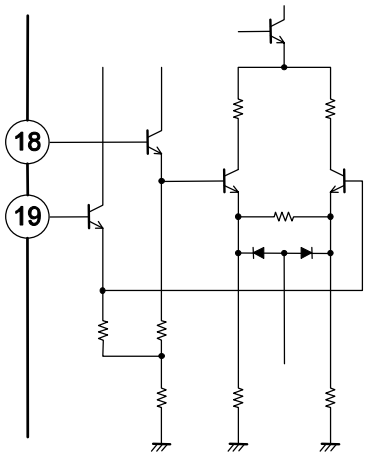
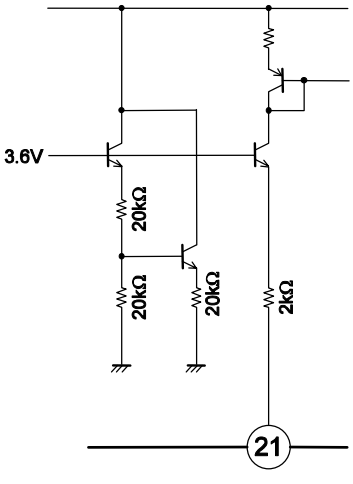
Pin No.	Pin name	Function	Equivalent circuit
15 16 17	2nd AGC FILTER 2nd AGC FILTER 1st AGC FILTER	IF AGC filter connection. The AGC voltage is created by smoothing the signal that results from peak detection by the AGC detector at pins 17 (first AGC), and 15 and 16 (second AGC). The video signal input to this IF AGC detector is a signal that was passed through the audio trap circuit.	
18 19	VIF INPUT VIF INPUT	VIF amplifier input. The input circuit is a balanced input, and its input impedance is due to the following component values. R ≈ 1.5kΩ C ≈ 3pF	
20	GND		
21	RF AGC VR	RF AGC adjustment. This pin sets the tuner's RF AGC operating point. Both the FM output and the video output can be muted by setting this pin to the ground level.	

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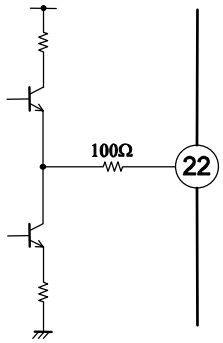
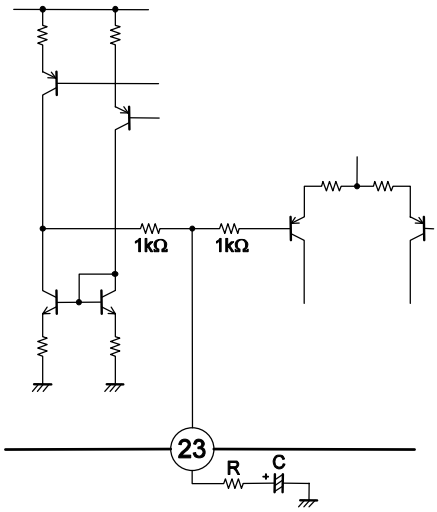
Pin No.	Pin name	Function	Equivalent circuit
22	BPF OUT	Band-pass filter output. The output to the external band-pass filter is passed through an internal amplifier before being output.	
23	FM FILTER	Filter that holds the FM detector output DC voltage fixed. Normally, a 1μF electrolytic capacitor is used. If the low band (around 50Hz) frequency characteristics are of concern, this value should be increased. The FM detection output level can be reduced and the FM dynamic range improved by inserting the resistor R in series with the capacitor between pin 23 and ground.	
24	FM DET OUT	Audio FM detector output. This is an emitter-follower circuit with a 300 Ω resistor inserted in series. • Stereo applications. In some application that provide input to a stereo decoder, the input impedance may be reduced, resulting in distortion in the L-R signal and degraded stereo characteristics. If this problem occurs, add a resistor between pin 24 and ground. R1 ≥ 5.1kΩ • Mono applications. Construct an external de-emphasis circuit. t = C×R2