C9812

Low EMI Clock Generator for Intel® 810E Chipset Systems

Product Features

- Intel's 810E clock solution
- 3 copies of CPU Clock (CPU[0:1] and CPU_ITP)
- 9 copies of SDRAM Clock (SDRAM[0:7] and DCLK)
- 8 copies of PCI Clock
- 2 copies of 3V66 Clock
- 2 copies of APIC Clock, synchronous to PCI Clock
- 1 REF Clock
- 1 USB Clock (Non SSC)
- 1 DOT Clock (Non SSC)
- Power Down Feature
- Spread Spectrum Support
- SMBUS Support for turning off unused clocks

Block Diagram

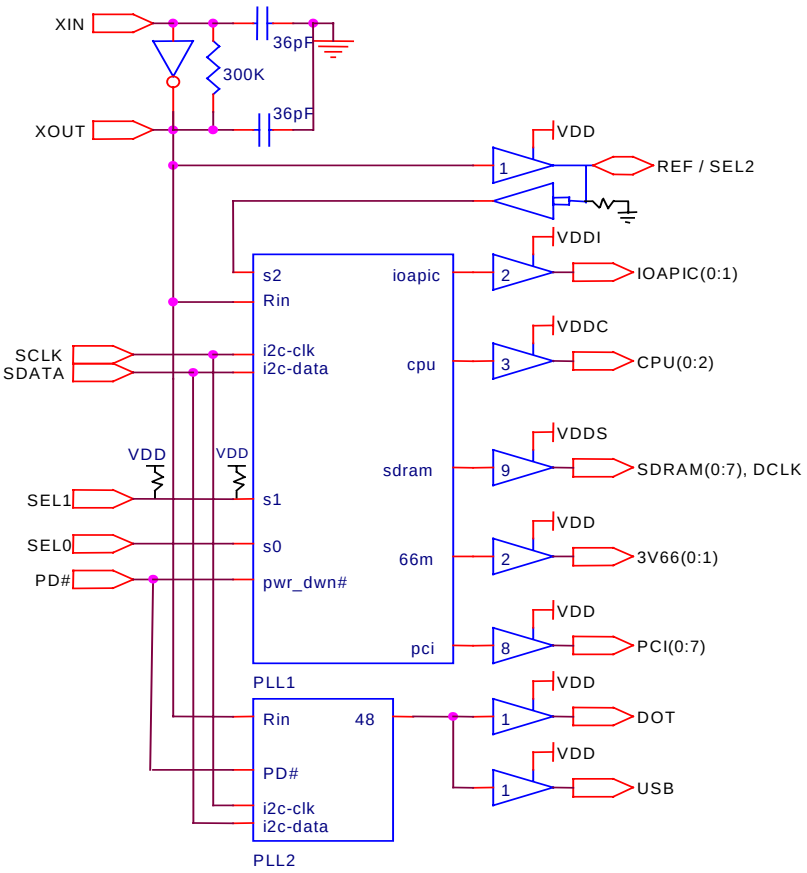


Fig.1

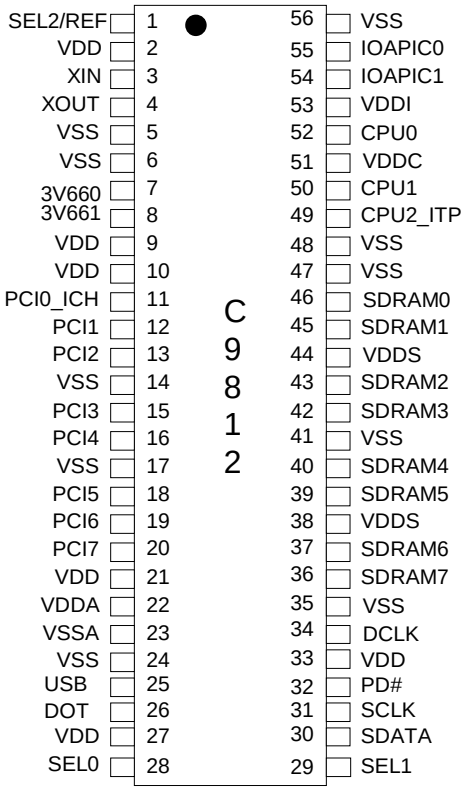
Frequency Table (MHz)

SEL2	SEL1	SEL0	CPU	SDRAM	PCI
X	0	0	Tristate	Tristate	Tristate
X	0	1	Test mode (see table2)		
0	1	0	66.6	100	33.3
0	1	1	100	100	33.3
1	1	X	133.3	100	33.3

Table 1

Note: The following clocks remain fixed frequencies except in Test Mode.
3V66=66.6MHz, USB/DOT=48MHz, REF=14.318MHz and IOAPIC=33.3MHz.

Pin Configuration



Cypress Semiconductor Corporation
525 Los Coches St.
Milpitas, CA 95035. Tel: 408-263-6300, Fax: 408-263-6571
http://www.cypress.com

Pin Description

PIN No.	Pin Name	PWR	I/O	TYPE	Description
1	**SEL2/REF**	VDD	I/O		3.3V 14.318 MHz clock output. This pin also serves as the select strap (associates with SEL0 & 1, see app. note page 5) for clock frequencies during power up. Refer to Table 1 for detail. This pin has an internal pull-down (Typ. 70KΩ).
3	**XIN**	VDD	I	OSC1	14.318MHz Crystal input
4	**XOUT**	VDD	O		14.318MHz Crystal output
11, 12, 13, 15, 16, 18, 19, 20	**PCI0/ICH PCI(1..7)**	VDD	O		3.3V PCI clock outputs
7, 8	**3V66(0,1)**	VDD	O		3.3V Fixed 66.6 MHz clock outputs
25	**USB**	VDD	O		3.3V Fixed 48 MHz clock outputs
26	**DOT**	VDD	O		3.3V Fixed 48 MHz clock outputs
28, 29	**SEL(0,1)**	VDD	I		3.3V LVTTL compatible inputs for logic selection. Has an internal pull-up (Typ. 250KΩ)
30	**SDATA**	VDD	I		I²C compatible SDATA input. Has an internal pull-up (>100KΩ)
31	**SCLK**	VDD	I		I²C compatible SCLK input. Has an internal pull-up (>100KΩ)
32	**PD#**	VDD	I		3.3V LVTTL compatible input. Device enters powerdown mode When held LOW. Has an internal pull-up (>100KΩ)
34	**DCLK**	VDD	O		3.3V output running 100MHz
36, 37, 39, 40, 42, 43, 45, 46	**SDRAM(7..0)**	VDDS	O		3.3V output running 100MHz. All SDRAM outputs can be turned off through SMBUS.
49, 50, 52	**CPU(2)_ITP, CPU(1,0)**	VDDC	O		2.5V Host bus clock outputs. 66, 100 or 133MHz depending on state of SEL(2..0)
54, 55	**IOAPIC(1,0)**	VDDI	O		2.5V clock outputs running rising edge synchronous with the PCI clock.
2, 9, 10, 21, 27, 33	**VDD**	-			3.3V Power Supply
22	**VDDA**	-			Analog circuitry 3.3V Power Supply
23	**VSSA**	-			Analog circuitry power supply Ground pins.
51, 53	**VDDC, VDDI**	-			2.5V Power Supply's
5, 6,14, 17, 24, 35, 41, 47, 48, 56	**VSS**	-		-	Common Ground pins.
38, 44	**VDDS**	-		-	3.3V power support for SDRAM clock output drivers.

A bypass capacitor (0.1μF) should be placed as close as possible to each positive power pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductance of the traces.

Test Mode Function

Test Mode Functionality

SEL2	SEL1	SEL0	CPU	SDRAM	3V66	PCI	48 MHz	REF	IOAPIC
x	0	1	TCLK/2	TCLK/2	TCLK/3	TCLK/6	TCLK/2	TCLK	TCLK/6

Table 2

Note: TCLK is a test clock over driven on the XIN input during test mode.

Power Management Functions

Power Management on this device is controlled by a single pin, PD# (pin32). When PD# is high (default) the device is in running and all signals are active.

When PD# is asserted (forced) low, the device is in shutdown (or in power down) mode and all power supplies (3.3V and 2.5V except for VDDA/pin 27) may be removed. When in power down, all outputs are synchronously stopped in a low state (see Fig.2 below), all PLL's are shut off, and the crystal oscillator is disabled. When the device is shutdown the I²C function is also disabled.

Power Management Timing

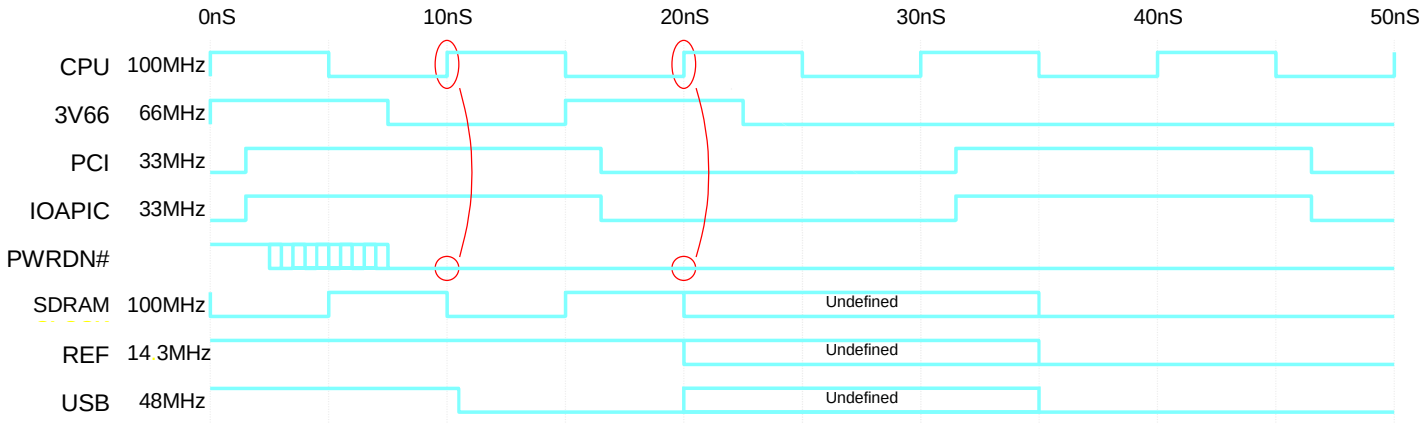


Fig.2

Power Management Current

PD#, **SEL[2..0]** (CPU Clock)	Maximum 2.5 Volt Current Consumption (VDD2.5 =2.625)	Maximum 3.3 Volt Current Consumption (VDD3.3 = 3.465 V)
0XXX (Power down)	100 µA	200 µA
1010 (66MHz)	70 mA	280 mA
1011 (100MHz)	100 mA	280 mA
111X (133MHz)	133 mA	280 mA

Table 3

When exiting the power down mode, the designer must supply power to the VDD pins first, a minimum of 200mS before releasing the PD# pin high.

Clock Synchronization and Phase Alignment

This device incorporates IOAPIC clock synchronization. With this feature, the IOAPIC clocks are derived from the CPU clock. The IOAPIC clock lags the CPU clock by the specified 1.5 to 3.5 nSec. Figure 3 shows the relationship between the CPU and IOAPIC clocks.

Device Clock Phase Relationships

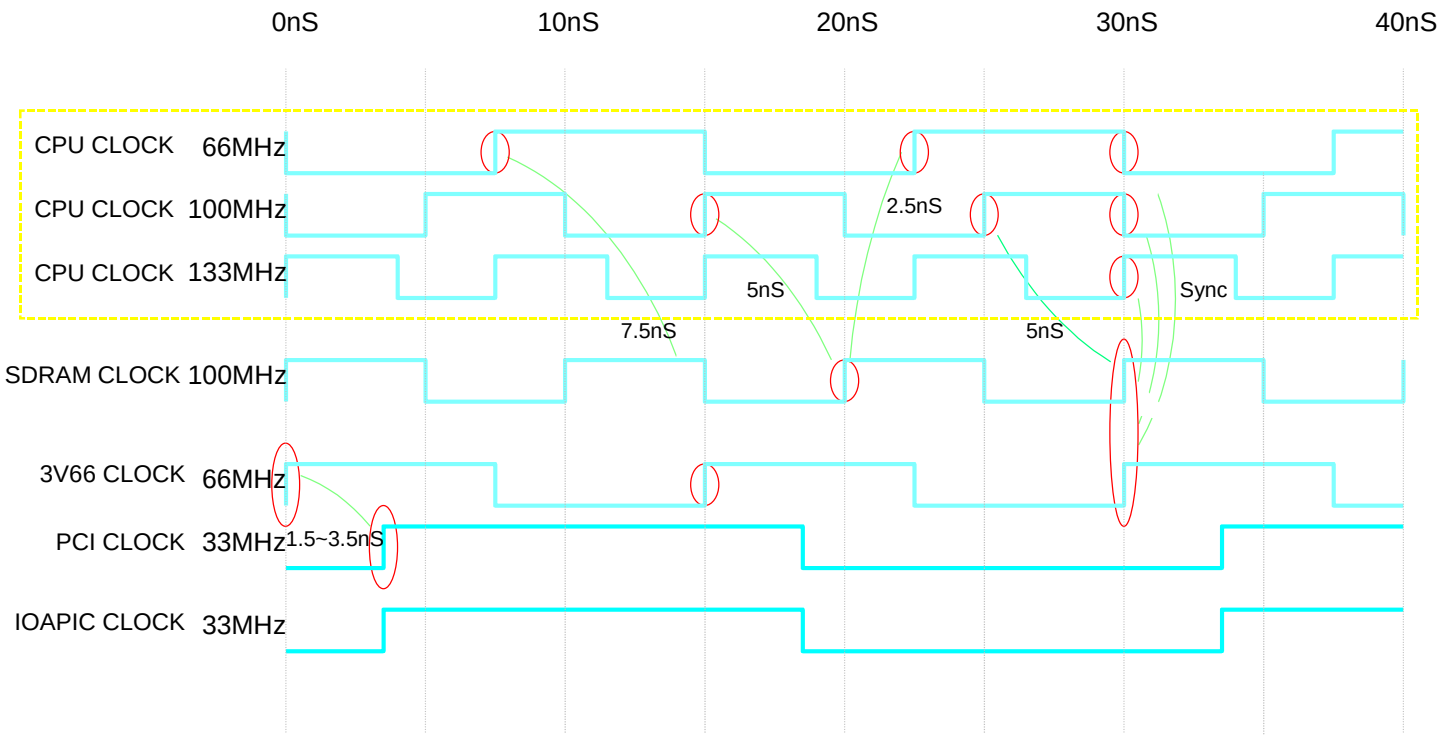


Fig.3

Power on Bi-Directional Pins

Power Up Condition:

Pin1 is a Power up bi-directional pin and is used for selecting the host frequency in page 1, table 1. During power-up of the device, this pin is in input mode (see Fig 4, below), therefore; it is considered an input select pins internal to the IC. After a settling time, the selection data is latch into the internal control register and this pin becomes a clock output.

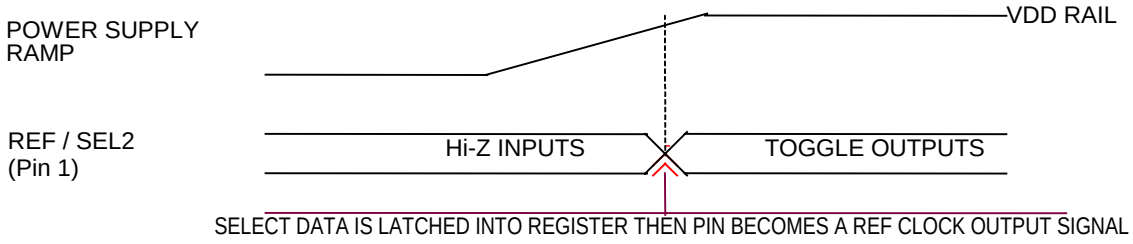


Fig.4

Strapping Resistor Options:

The power up bi-directional pins have a large value pull-down each (70KΩ), therefore, a selection "0" is the default. If the system uses a slow power supply (over 5mS settling time), then **it is recommended** to use an external Pull-down in order to insure a low selection.

Fig. 5 If a selection "0" is desired, then a jumper is placed on JP1 to a 10KΩ resistor as implemented as shown in Fig.5. Please note the selection resistor (Rdn) is placed before the Damping resistor (Rd) close to the pin.

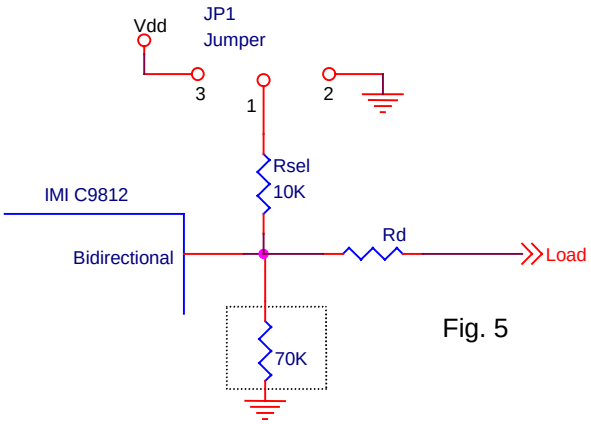


Fig. 5

2-Wire SMBUS Control Interface

The 2-wire control interface implements a write slave only interface according to SMBus specification. (See Fig. 7 / P. 8). The device can be read back by using standard SMBUS command bytes. Sub addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is an 8-bit address. W#=0 in write mode.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. Data is transferred MSB first at a max rate of 100kbits/S. The device will not respond to any other control interface conditions, and previously set control registers are retained.

SMBUS Test Circuitry

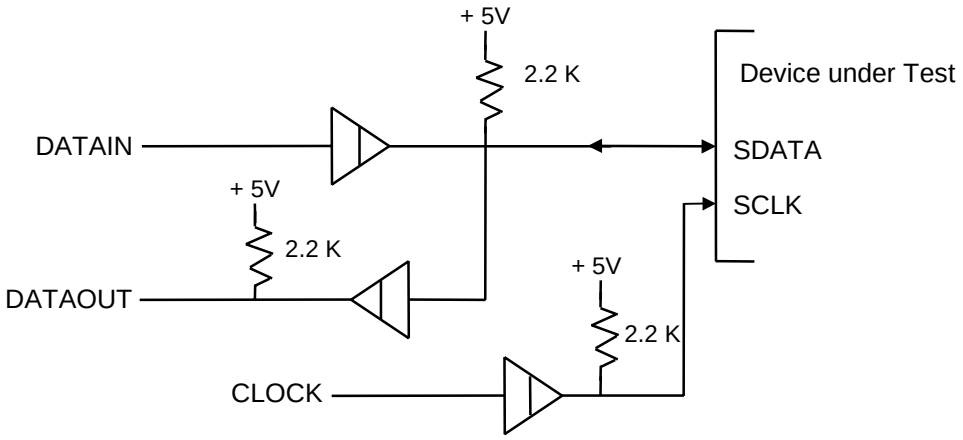


Fig.6

Note: Buffer is 7407 with VCC @ 5.0 V

Serial Control Registers

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up.

Following the acknowledge of the Address Byte, two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care"; they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the below described sequence (Byte 0, Byte 1, and Byte2) will be valid and acknowledged.

Byte 0: CPU Clock Register (1=Enable, 0=Disable, Default=07)

Bit	@Pup	Pin#	Description
7	0	-	Reserved
6	0	-	Reserved
5	0	-	Reserved
4	0	-	Reserved
3	0	-	Spread spectrum mode
2	1	26	DOT
1	1	25	USB
0	1	49	CPU2_ITP

Byte 1: SDRAM Clock Register (1=Enable, 0=Disable, Default=FF)

Bit	@Pup	Pin#	Description
7	1	36	SDRAM7
6	1	37	SDRAM6
5	1	39	SDRAM5
4	1	40	SDRAM4
3	1	42	SDRAM3
2	1	43	SDRAM2
1	1	45	SDRAM1
0	1	46	SDRAM0

Byte 2: PCI Clock Register (1=Enable, 0=Disable, Default=FE)

Bit	@Pup	Pin#	Description
7	1	20	PCI7
6	1	19	PCI6
5	1	18	PCI5
4	1	16	PCI4
3	1	15	PCI3
2	1	13	PCI2
1	1	12	PCI1
0	0	-	Reserved

Byte 3: Reserved Register (Default=00)

Byte 4: Reserved Register (Default=00)

Byte 5: SSCG Control Register (Default=00)

Bit	@Pup	Pin#	Description
7	0	-	Spread Mode (0=down, 1=center)
6	0	-	Ref. Table 4
5	0	-	Ref. Table 4
4	0	-	Reserved
3	0	-	Reserved
2	0	-	Reserved
1	0	-	Reserved
0	0	-	Reserved

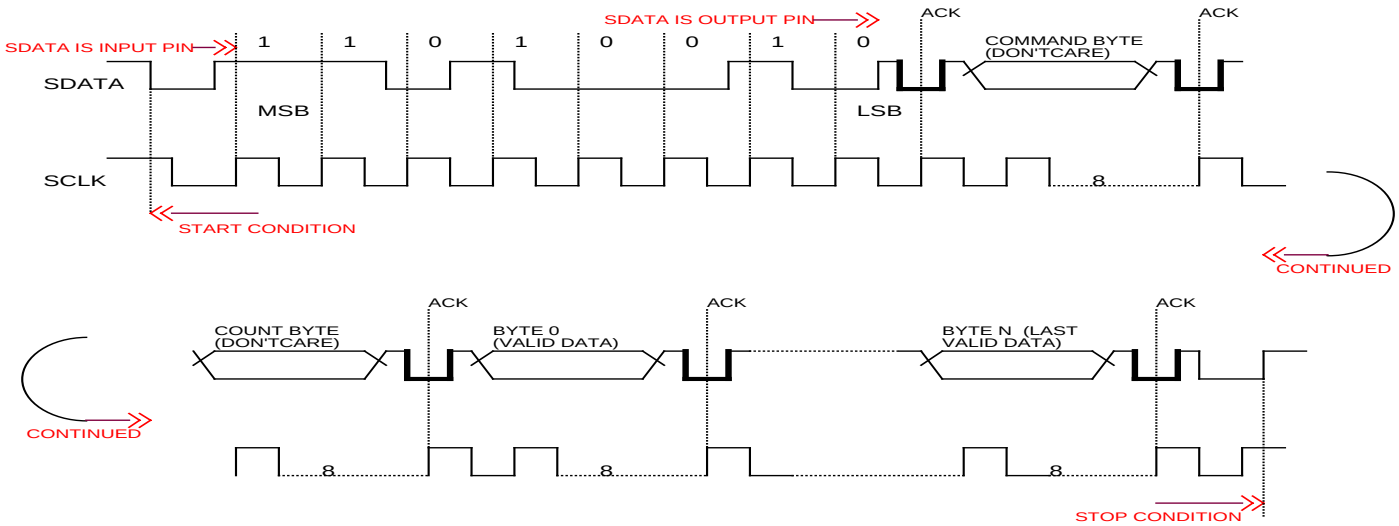
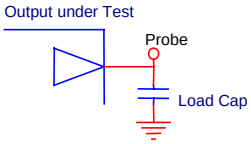
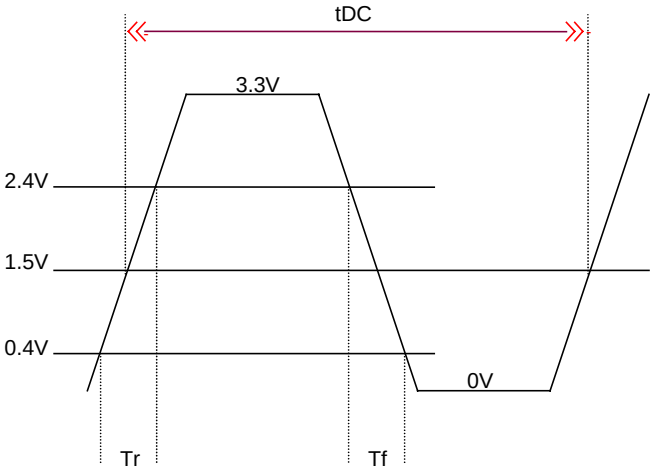


Figure 7
SMBUS Communications Waveforms

Test and Measurement Condition



3.3V signals



2.5V signals

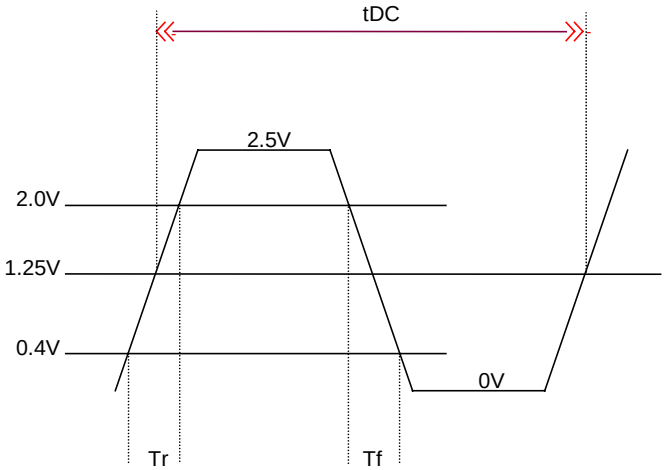


Fig.8

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique applied here for maximum efficiency in minimizing Electro-Magnetic Interference radiation generated from repetitive digital signals mainly clocks. A clock accumulates EM energy at the center frequency it is generating. Spread Spectrum distributes this energy over a small frequency bandwidth therefore spreading the same amount of energy over a spectrum. This technique is achieved by modulating the clock down from (Fig.9A) or around the center (Fig.9B) of its resting frequency by a certain percentage (which also determines the energy distribution bandwidth). In this device, Spread Spectrum is enabled by setting SMBUS byte0, bit3 = 1. The default of the device at power up keeps the Spread Spectrum disabled, it is therefore, important to have SMBUS accessibility to turn-on the Spread Spectrum function. Once the Spread Spectrum is enabled, the spread bandwidth option is selected by SST(0:2) in SMBUS byte 5, bits 5, 6 & 7 following tables 4A, and 4B below.

In Down Spread mode the center frequency is shifted down from its rested (non-spread) value by ½ of the total spread %. (eg.: assuming the center frequency is 100MHz in non-spread mode; when down spread of –0.5% is enabled, the center frequency shifts to 99.75MHz.).

In Center Spread mode, the Center frequency remains the same as in the non-spread mode.

Down Spread

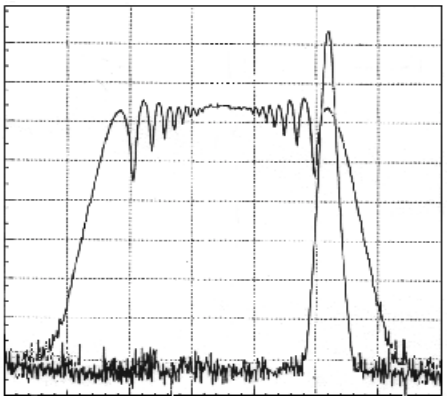


Fig.9A

Center Spread

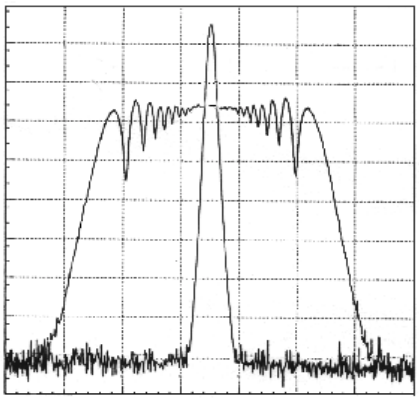


Fig.9B

Spread Spectrum Selection Tables

I²C BYTE5 Bit[7:5]	Center Frequency (MHz)	Spread %
100	66/100/133.3	± 0.25
101	66/100/133.3	± 0.35
110	66/100/133.3	± 0.5
111	66/100/133.3	± 0.7

Table 4A

I²C BYTE5 Bit[7:5]	Down Frequency (MHz)	Spread %
000	66/100/133.3	- 0.5
001	66/100/133.3	- 0.7
010	66/100/133.3	- 1.0
011	66/100/133.3	- 1.5

Table 4B

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V
Maximum Input Voltage Relative to VDD: VDD + 0.3V
Storage Temperature: -65ºC to + 150ºC
Operating Temperature: 0ºC to +70ºC
Maximum ESD protection 2KV
Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL1	-	-	1.0	Vdc	Note 1
Input High Voltage	VIH1	2.0	-	-	Vdc	
Input Low Voltage	VIL2	-	-	1.0	Vdc	Note 2
Input High Voltage	VIH2	2.2	-	-	Vdc	
Input Low Current (@VIL = VSS)	IIL	-66		-5	µA	For internal Pull up resistors, Notes 1,3
Input High Current (@VIL =VDD)	IIH			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd3.3V	-	-	280	mA	Sel2 = Sel1 = Sel0 = 1, Note 4
Dynamic Supply Current	Idd2.5V	-	-	100	mA	Sel2 = Sel1 = Sel0 = 1, Note 4
Static Supply Current	Isdd	-	-	300	µA	Sel2 = Sel1 = Sel0 = x, Note 4
Input pin capacitance	Cin	-	-	5	pF	
Output pin capacitance	Cout	-	-	6	pF	
Pin capacitance	Lpin	-	-	7	nH	
Clock Stablization Time	tstab	3	-	-	mSec	Measured from VDD – 3.15 volts
Crystal pin capacitance	Cxtal	32	34	38	pF	Measured from Pin to Ground. Note 5
Crystal DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Crystal Startup time	Txs	-	-	40	µS	From Stable 3.3V power supply.
VDD=VDDS = 3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0º to +70ºC						

Note1: Applicable to input signals: Sel(0:1), PD#
Note2: Applicable to Sdata, and Sclk.
Note3: Although internal pull-up resistors have a typical value of 250K, this value may vary between 200K and 500K. Internal Pull-down resisters are typically 70K in value.
Note4: All outputs loaded as per table below.
Note5: Although the device will reliably interface with crystals of a 17pF – 20pF C_L range, it is optimized to interface with a typical C_L = 18pF crystal specifications.

Clock Name	Max Load (in pF)
CPU, IOAPIC, REF, USB	20
PCI, SDRAM, 3V66(0,1)	30
DOT	15

Table 5.

AC Parameters

Symbol	Parameter	133 MHz Host		100 MHz Host		Units	Notes
		Min	Max	Min	Max		
TPeriod	CPU(0:1) period	7.5	8.0	10.0	10.5	nS	5, 6, 8
THIGH	CPU(0:1) high time	1.87	-	3.0	-	nS	6,10
TLOW	CPU(0:1) low time	1.67	-	2.8	-	nS	6, 11
Tr / Tf	CPU(0:1) rise and fall times	0.4	1.6	0.4	1.6	nS	6, 7
TSKEW	CPU0 to CPU1 Skew time	-	175	-	175	pS	6, 8, 9
TCCJ	CPU(0:1) Cycle to Cycle Jitter	-	250	-	250	pS	6, 8, 9
TPeriod	APIC(0:1) period	60.0	-	60.0	-	nS	5, 6, 8
THIGH	APIC(0:1) high time	25.5	-	25.5	-	nS	6,10
TLOW	APIC(0:1) low time	25.3	-	25.3	N/S	nS	6, 11
Tr / Tf	APIC(0:1) rise and fall times	0.4	1.6	0.4	1.6	nS	6, 7
TCCJ	APIC(0:1) Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	3V66-(0:1) period	15.0	16.0	15.0	16.0	nS	5, 6, 8
THIGH	3V66-(0:1) high time	5.25	-	5.25	-	nS	6,10
TLOW	3V66-(0:1) low time	5.05	-	5.05	-	nS	6, 11
Tr / Tf	3V66-(0:1) rise and fall times	0.4	1.6	0.4	1.6	nS	6, 7
TSKEW	3V66-0 to 3V66-1 Skew time	-	250	-	250	pS	6, 8, 9
TCCJ	3V66-(0:1) Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	PCI(0:7) period	30.0	-	30.0	-	nS	5, 6, 8
THIGH	PCI(0:7) period	12.0	-	12.0	-	nS	6,10
TLOW	PCI(0:7) low time	12.0	-	12.0	-	nS	6, 11
Tr / Tf	PCI(0:7) rise and fall times	0.5	2.0	0.5	2.0	nS	6, 7
TSKEW	(Any PCI clock) to (Any PCI clock) Skew time	-	500	-	500	pS	6, 8, 9
TCCJ	PCI(0:7) Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	48MHz period (conforms to +167ppm max)	20.8299	20.8333	20.8299	20.8333	nS	5, 6, 8
Tr / Tf	48MHz rise and fall times	1.0	4.0	1.0	4.0	nS	6, 7
TCCJ	48MHz Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	REF period	69.8413	71.0	69.8413	71.0	nS	5, 6, 8
Tr / Tf	REF rise and fall times	1.0	4.0	1.0	4.0	nS	6, 7
TCCJ	REF Cycle to Cycle Jitter	-	1000	-	1000	pS	6, 8
tpZL, tpZH	Output enable delay (all outputs)	1.0	10.0	1.0	10.0	nS	13
tpLZ, tpZH	Output disable delay (all outputs)	1.0	10.0	1.0	10.0	nS	13
tstable	All clock Stabilization from power-up		3		3	mS	12

Switching Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Duty Cycle	-	45	50	55	%	Note 6
CPU to SDRAM	TPD1	-	-	500	pS	CPU = 133.3MHz, Notes 6, 7
CPU to 3V66	TPD2	-	-	500	pS	CPU = 133.3MHz, Notes 6, 7
SDRAM to 3V66	TPD3	-	-	500	pS	CPU = 66.6/100/133.3MHz Notes 6, 7
3V66 to PCI	tPD	1.5	-	-	nS	CPU = 66.6/100/133.3MHz Notes 6, 7
PCI to IOAPIC	tPD	-	0	1	nS	CPU = 66.6/100/133.3MHz Notes 6, 7
Skew (CPU0-CPU1)	tSKEW1	-	-	175	pS	see Notes 6, 7
Skew (SDRAM-SDRAM)	tSKEW2	-	-	250	pS	see Notes 6, 7
Skew (APIC-APIC)	tSKEW3	-	-	250	pS	
Skew (3V66-3V66)	tSKEW4	-	-	175	pS	
Skew (PCI – PCI)	TSKEW5	-	-	500	pS	
Cycle to Cycle Jitter	ΔP1	-	-	250	pS	CPU, and SDRAM, Notes 6 & 7
Cycle to Cycle Jitter	ΔP2	-	-	500	pS	IOAPIC, USB, DOT, 3V66, PCI, Notes 6, 7
Cycle to Cycle Jitter	ΔP3	-	-	1,000	pS	REF, Notes 6& 7
VDD=VDDS=3.3V ±5%, VDDC=VDDI=2.5±5%, TA=0 to 70ºC						

Note 6: All outputs loaded as per table 5 below. Probes are placed on the pins and taken at 1.5V levels for 3.3V signals and at 1.25V for 2.5V signals.

Note 7: This measurement is applicable with Spread Spectrum ON or OFF.

Output Buffer Characteristics

Buffer Characteristics for CPU

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-28	-61	-107	mA	Vout =VDDC - 0.4V
Pull-Up Current	IOH_2	-26	-58	-101	mA	Vout = 1.2 V
Pull-Down Current	IOL_1	12	24	40	mA	Vout = 0.4 V
Pull-Down Current	IOL_1	27	56	93	mA	Vout = 1.2 V
Dynamic Output Impedance	Z0	13.5		45	Ω	
Rise Time Min Between 0.4 and 2.0 V	Tr	0.4	-	1.6	nS	20pF Load
Fall Time Max Between 0.4 and 2.0 V	Tf	0.4	-	1.6	nS	20pF Load

Output Buffer Characteristics (Cont.)

Buffer Characteristics for PCI, 3V66 and DOT

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-33	-58	-194	mA	Vout =VDDC - 1.0 V
Pull-Up Current	IOH_2	-30	-54	-184	mA	Vout = 1. 5 V
Pull-Down Current	IOL_1	9.4	18	38	mA	Vout = 0.4 V
Pull-Down Current	IOL_1	28	55	148	mA	Vout = 1.5 V
Dynamic Output Impedance	Z0	12		55	Ω	
Rise Time Min Between 0.4 and 2.4 V	Tr	0.5	-	2.0	nS	30pF Load
Fall Time Max Between 0.4 and 2.4 V	Tf	0.5	-	2.0	nS	30pF Load

Buffer Characteristics for USB and REF

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-29	-46	-99	mA	Vout =VDD - 1.0 V
Pull-Up Current	IOH_2	-27	-43	-92	mA	Vout = 1. 5 V
Pull-Down Current	IOL_1	9	13	27	mA	Vout = 0.4 V
Pull-Down Current	IOL_1	26	39	79	mA	Vout = 1.5 V
Dynamic Output Impedance	Z0	20		60	Ω	
Rise Time Min Between 0.4 and 2.4 V	Tr	1.0	-	4.0	nS	20pF Load
Fall Time Max Between 0.4 and 2.4 V	Tf	1.0	-	4.0	nS	20pF Load

Buffer Characteristics for IOAPIC

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-28	-61	-107	mA	Vout =VDDI - 0.5V
Pull-Up Current	IOH_2	-26	-58	-107	mA	Vout = 1. 0 V
Pull-Down Current	IOL_1	12	24	40	mA	Vout = 0.4 V
Pull-Down Current	IOL_1	28	60	100	mA	Vout = 1.4 V
Dynamic Output Impedance	Z0	13.5		45	Ω	
Rise Time Min Between 0.4 and 2.0 V	Tr	0.4	-	1.6	nS	20pF Load
Fall Time Max Between 0.4 and 2.0 V	Tf	0.4	-	1.6	nS	20pF Load

Output Buffer Characteristics (Cont.)

Buffer Characteristics for SDRAM

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-72	-116	-198	mA	Vout =VDD - 1. 0 V
Pull-Up Current	IOH_2	-68	-110	-188	mA	Vout = 1. 4 V
Pull-Down Current	IOL_1	23	34	53	mA	Vout = 0.4 V
Pull-Down Current	IOL_1	64	98	159	mA	Vout = 1.5 V
Dynamic Output Impedance	Z0	10		24	Ω	
Rise Time Min Between 0.4 and 2.4 V	Tr	0.4	-	1.6	nS	30pF Load
Fall Time Max Between 0.4 and 2.4 V	Tf	0.4	-	1.6	nS	30pF Load
VDD=VDDS=3.3V ±5%, VDDC=VDDI=2.5±5%, TA=0 to 70ºC						

Suggested Crystal Oscillator Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	TC	-	-	+/-100	PPM	Note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) Note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) Note 1
Mode	OM	-	-	-		Parallel Resonant, Note 1
Load Capacitance	CL	-	18	-	pF	The crystal's rated load. Note 1
Effective Series resistance (ESR)	R1	-	40	-	Ohms	Note 1
Power Dissipation	DL	-	-	0.10	mW	Note 1
Shunt Capacitance	CO	-	--	8	pF	Crystal's internal package capacitance (total)

Note1: For best performance and accurate Center frequencies of this device, It is recommended but not mandatory that the chosen crystal meets these specifications

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.
Budgeting Calculations
Device pin capacitance: Cxtal = 34pF
In order to meet the specification for CL = 18pF following the formula:

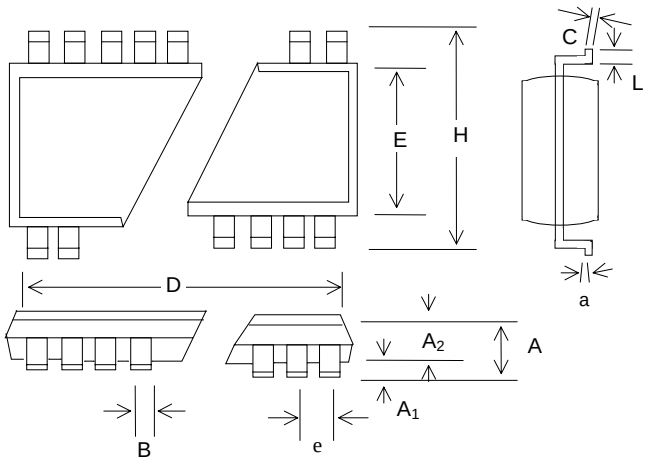
$$C_L = \frac{C_{XIN} x C_{XOUT}}{C_{XIN} + C_{XOUT}}$$

Then the board trace capacitance between Xin and the crystal should be no more than 2pF. (same is applicable to the trace between Xout and the crystal)

In this case the total capacitance from the crystal to Xin will be 36pF. Similarly the total capacitance between the crystal and Xout will be 36pF. Hence using the above formula:

$$C_L = \frac{36\,pF x 36\,pF}{36\,pF + 36\,pF} = 18\,pF$$

Package Drawing and Dimensions



56 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.088	0.090	0.092	2.24	2.29	2.34
B	0.008	0.010	0.0135	0.203	0.254	0.343
C	0.005	-	0.010	0.127	-	0.254
D	.720	.725	.730	18.29	18.42	18.54
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.025 BSC			0.635 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
L	0.024	0.032	0.040	0.61	0.81	1.02
a	0º	5º	8º	0º	5º	8º
X	0.085	0.093	0.100	2.16	2.36	2.54

Ordering Information

Part Number	Package Type	Production Flow
C9812DYB	56 PIN SSOP	Commercial, 0 to 70ºC

Marking: Example: Cypress
C9812
Date Code, Lot #

C9812DYB

Flow
B = Commercial, 0 to 70ºC

Package
Y = SSOP

Revision

Device Number

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