FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27701-4E

ASSP For Power Management Applications (Secondary battery)

DC/DC Converter IC for Charging

MB3832A

■ DESCRIPTION

The MB3832A is a pulse width modulation (PWM) DC/DC converter IC, incorporating a current detector amplifier and error amplifiers (2 circuits) to control the output voltage and current independently. It is suitable for down-conversion.

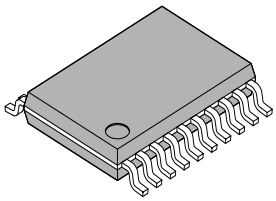
With an on-chip reference voltage generator, the MB3832A is best suited for use in applications such as lithium-ion battery (1-cell to 3-cell) chargers.

■ FEATURES

- High precision reference voltage source: 2.5 V ± 0.5% (+25°C)
  : 2.5 V ± 1.0% (–10°C to +85°C)
- High frequency operating capability: 500 kHz Max.
- Wide operating supply voltage range: 3.6 V to 18 V
- On-chip current detector amplifier with wide in-phase input voltage range: 0 V to V_{CC}
- On-chip standby function
- On-chip triangular waveform oscillator capable of operating in external synchronization
- On-chip, timer-latch short-circuit protection circuit
- Internal totem-pole output stage supporting P-channel MOS FETs and PNP transistors

■ PACKAGE

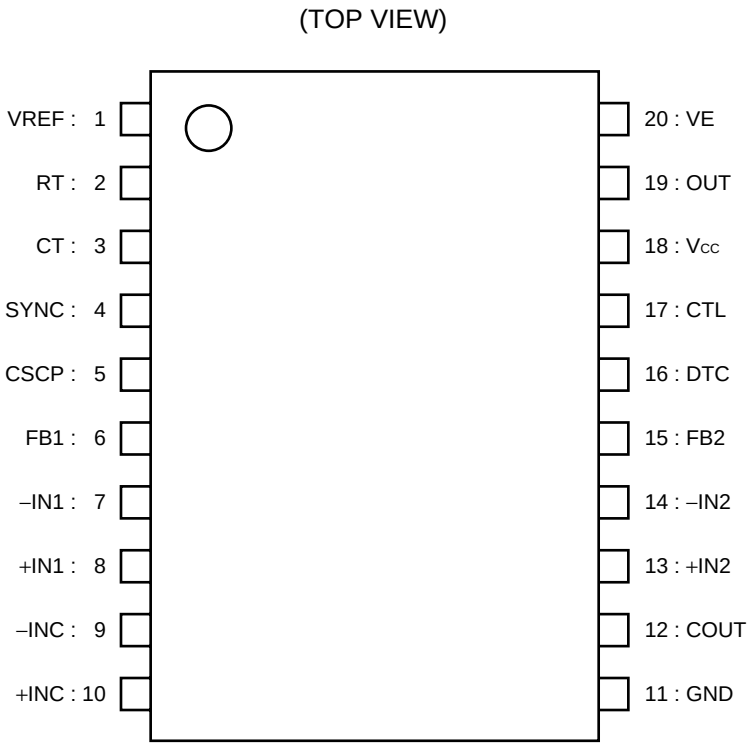
20-pin plastic SSOP



(FPT-20P-M03)

FUJITSU

■ PIN ASSIGNMENT



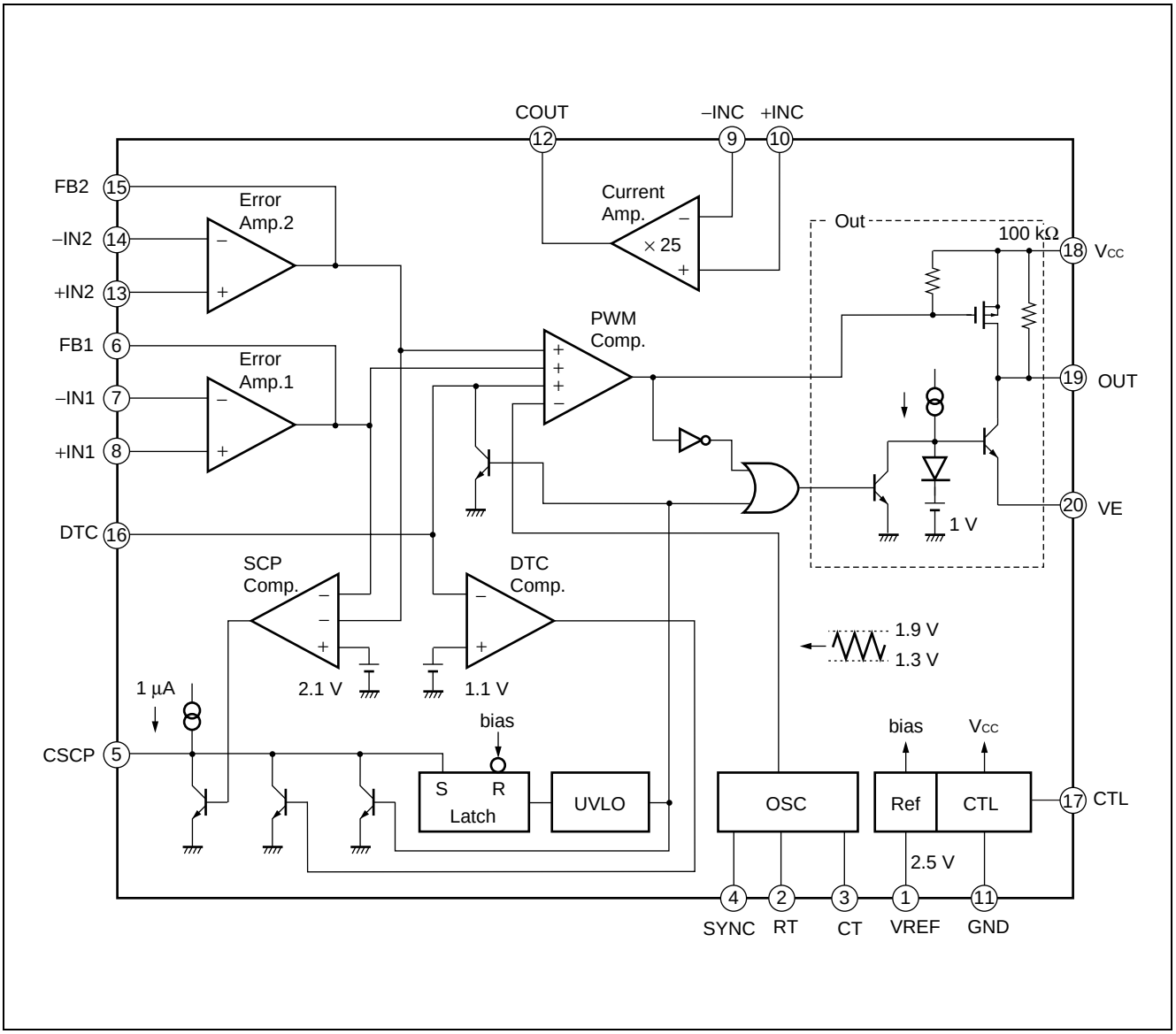
(FPT-20P-M03)

■ PIN DESCRIPTION

Pin no.	Pin name	I/O	Descriptions
1	VREF	O	Reference voltage output terminal
2	RT	—	Connection terminal for triangular wave frequency setting resistor
3	CT	—	Connection terminal for triangular wave frequency setting capacitor
4	SYNC	I	External synchronous signal input terminal
5	CSCP	—	Connection terminal for time constant setting capacitor for timer-latch short-circuit protection circuit
6	FBI	O	Error amplifier 1 output terminal
7	–IN1	I	Error amplifier 1 inverted input terminal
8	+IN1	I	Error amplifier 1 non-inverted input terminal
9	–INC	I	Current detector amplifier inverted input terminal
10	+INC	I	Current detector amplifier non-inverted input terminal
11	GND	—	Ground terminal
12	COUT	O	Current detector amplifier output terminal
13	+IN2	I	Error amplifier 2 non-inverted input terminal
14	–IN2	I	Error amplifier 2 inverted input terminal
15	FB2	O	Error amplifier 2 output terminal
16	DTC	I	Connection terminal for dead time/soft start time setting resistor/capacitor
17	CTL	I	Power supply control input terminal “H” level: Active state “L” level: Standby state
18	V_{CC}	—	Power supply terminal
19	OUT	O	Totem-pole output terminal
20	VE	—	Connector terminal for output sink current setting resistor

I: Input pin, O: Output pin

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	—	—	20	V
Control input voltage	V_{CTL}	—	—	20	V
Output current	I_O	OUT terminal, DC	—	50	mA
Peak output current	I_O	OUT terminal, Duty ≦ 5%	—	600	mA
Allowable dissipation	P_D	Ta ≦ +25°C	—	540*	mW
Storage temperature	Tstg	—	–55	+125	°C

*: When mounted on a 10 cm-square dual-sided epoxy base board

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{CC}	—	3.6	16	18	V
Reference voltage output current	I_{OR}	—	–1	—	0	mA
Input voltage	V_{IN}	+IN1, –IN1, +IN2, –IN2 terminal	0	—	V_{CC} – 0.9	V
		+INC, –INC terminal	0	—	V_{CC}	V
Control input voltage	V_{CTL}	CTL terminal	0	—	18	V
SYNC input voltage	V_{SYNC}	SYNC terminal	0	—	V_{CC}	V
Output current	I_O	OUT terminal, DC	—	—	30	mA
Oscillator frequency	f_{OSC}	—	10	200	500	kHz
Timing capacitance	C_T	—	100	390	2200	pF
Timing resistance	R_T	—	8.2	12	51	kΩ
Short detection capacitance	C_{SCP}	—	—	0.1	1.0	µF
Operating temperature	Ta	—	–30	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 16 V, Ta = +25°C)

Parameter		Symbol	Pin no.	Condition	Value			Unit
					Min	Typ	Max	
Reference voltage block (Ref)	Output voltage	V_{REF}	1	Ta = +25°C	2.4875	2.50	2.5125	V
				Ta = –10°C to +85°C	2.475	2.50	2.525	V
				Ta = +25°C to +85°C	2.480	2.50	2.520	V
	Input stability	Line	1	V_{CC} = 3.6 V to 18 V	—	1	10	mV
	Load stability	Load	1	I_{REF} = 0 mA to –1 mA	—	3	10	mV
	Short circuit output current	I_{OS}	1	V_{REF} = 0 V	–36	–16	–7	mA
Under voltage lockout circuit block (UVLO)	Threshold voltage	V_{TH}	16	V_{CC} terminal	—	2.8	3.1	V
		V_{TL}	16	V_{CC} terminal	2.3	2.6	—	V
	Hysteresis width	V_H	16	V_{CC} terminal	80	200	—	mV
	Reset voltage	V_{RST}	19	V_{CC} terminal	1.7	2.1	—	V
Short detection block (SCP Comp, S-R Latch)	Detection voltage	V_{TH}	5	FB terminal	2.0	2.1	2.2	V
	Threshold voltage	V_{TH}	5	CSCP terminal	0.65	0.70	0.75	V
	Input standby voltage	V_{STB}	5	CSCP terminal	—	50	100	mV
	Input latch voltage	V_I	5	CSCP terminal	—	50	100	mV
	Input source current	I_{CSCP}	5	CSCP terminal	–1.4	–1.0	–0.6	µA
Triangular wave oscillator block (OSC)	Oscillator frequency	f_{OSC}	19	C_T = 330 pF, R_T = 12 kΩ	190	200	210	kHz
	Frequency input stability	Δf/f	19	V_{CC} = 3.6 V to 18 V	—	1	5	%
	SYNC input condition	V_{IH}	19	Input “H” level	2.0	—	—	V
		V_{IL}	19	Input “L” level	0	—	0.8	V
	Input current	I_{SYNC}	4	V_{SYNC} = 5 V	—	50	100	µA
Error amplifier (Error Amp.1, 2)	Input offset voltage	V_{IO}	8, 7, 13, 14	V_{FB} = 1.6 V	–3	—	3	mV
	Input bias current	I_B	8, 7, 13, 14	V_{FB} = 1.6 V	–200	–50	—	nA
	Common mode input voltage range	V_{CM}	8, 7, 13, 14	—	0	—	V_{CC} – 0.9	V
	Common mode rejection ratio	CMRR	6, 15	—	60	100	—	dB
	Voltage gain	A_V	6, 15	DC	60	100	—	dB
	Frequency bandwidth	BW	6, 15	A_V = 0 dB	—	750*	—	kHz
	Maximum output voltage width	V_{OM}^+	6, 15	—	2.5	2.7	—	V
		V_{OM}^-	6, 15	—	—	0.8	1.0	V
	Output source current	I_{OM}^-	6, 15	V_{FB} = 1.6 V	—	–120	–60	µA
	Output sink current	I_{OM}^+	6, 15	V_{FB} = 1.6 V	0.6	2.0	—	mA

*: Standard design value

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(V_{CC} = 16 V, Ta = +25°C)

Parameter		Symbol	Pin no.	Condition	Value			Unit
					Min	Typ	Max	
Current detector amplifier block (Current Amp.)	Input offset voltage	V_{IO}	10, 9	V_{+INC}, V_{-INC} = 2.4 V to 12.6 V	–2	—	2	mV
	Input bias current	I_{+INC}	10	V_{+INC} = 12.7 V, V_{-INC} = 12.6 V	—	1	2	µA
		I_{-INC}	9	V_{+INC} = 0.1 V, V_{-INC} = 0 V	–2	–1	—	µA
	Output voltage	V_{O1}	12	V_{+INC} = 12.7 V, V_{-INC} = 12.6 V	2.25	2.5	2.75	V
		V_{O2}	12	V_{+INC} = 12.8 V, V_{-INC} = 12.6 V	4.5	5.0	5.5	V
		V_{O3}	12	V_{+INC} = 0.1 V, V_{-INC} = 0 V	2.25	2.5	2.75	V
		V_{O4}	12	V_{+INC} = 0.2 V, V_{-INC} = 0 V	4.5	5.0	5.5	V
	Common mode input voltage range	V_{CM}	10, 9	—	0	—	V_{CC}	V
	Common mode rejection ratio	CMRR	12	V_{+INC}, V_{-INC} = 2.4 V to 12.6 V	60	90	—	dB
	Voltage gain	A_V	12	V_{-INC} = 12.6 V	22.5	25	27.5	V/V
	Frequency bandwidth	BW	12	A_V = 0 dB	—	500*	—	kHz
	Output resistance	R_O	12	f = 10 kHz	—	20*	—	Ω
	Maximum output voltage width	V_{OM^+}	12	—	V_{CC} – 2.0	V_{CC} – 1.6	—	V
		V_{OM^-}	12	—	—	50	200	mV
	Output source current	I_{OM^-}	12	V_{COUT} = 2.5 V	—	–7	–2	mA
	Output sink current	I_{OM^+}	12	V_{COUT} = 2.5 V	60	170	—	µA
PWM comparator block (PWM Comp.)	Threshold voltage	V_{T0}	19	Duty cycle = 0 %	1.2	1.3	—	V
		V_{T100}	19	Duty cycle = 100 %	—	1.9	2.0	V
	Input bias current	I_{DTC}	16	V_{DTC} = 0.4 V	–1.0	–0.2	—	µA
	Latch mode input current	I_{DTC}	16	V_{DTC} = 2.5 V	270	900	—	µA
	Input latch voltage	V_{DTC}	16	I_{DTC} = 100 µA	—	0.15	0.3	V
	ON duty cycle	Dtr	19	V_{DTC} = V_{REF}/1.56	43	48	53	%

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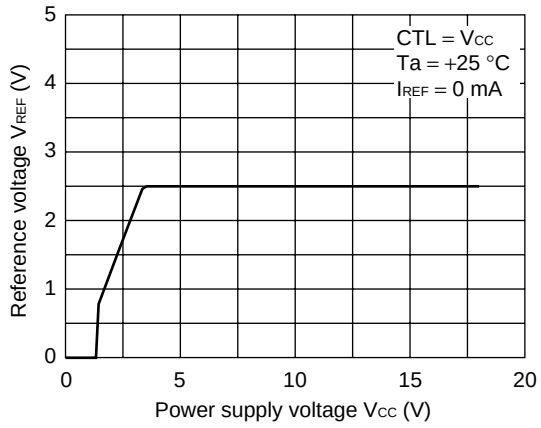
(V_{CC} = 16 V, Ta = +25°C)

Parameter		Symbol	Pin no.	Condition	Value			Unit
					Min	Typ	Max	
Output block (OUT)	Output on resistance	R_{ON}	19	I_O = –50 mA	—	5	8	Ω
	Output sink current	I_O	19	R_E = 33 Ω	18	30	42	mA
	Output voltage	V_{OH}	19	I_O = –300 mA	12.5	14	—	V
		V_{OL}	19	I_O = 300 mA	—	1.2	1.8	V
	Control-off output resistance	R_{OUT1}	19	V_{CTL} = 0 V, V_{REF} = 2.5 V, I_O = –50 mA	—	5	8	Ω
		R_{OUT2}	19	V_{CTL} = 0 V, V_{REF} = 0 V, I_O = –10 µA	70	100	130	kΩ
Control block (CTL)	CTL input condition	V_{ON}	1	IC is active state	2.0	—	18	V
		V_{OFF}	1	IC is standby state	0	—	0.8	V
	Input current	I_{IH}	17	V_{CTL} = 5 V	—	100	200	µA
		I_{IL}	17	V_{CTL} = 0 V	–1	0	—	µA
General	Standby current	I_{CCS}	18	V_{CTL} = 0 V	—	—	10	µA
	Power supply current	I_{CC}	18	Output “H”	—	4.6	7.0	mA

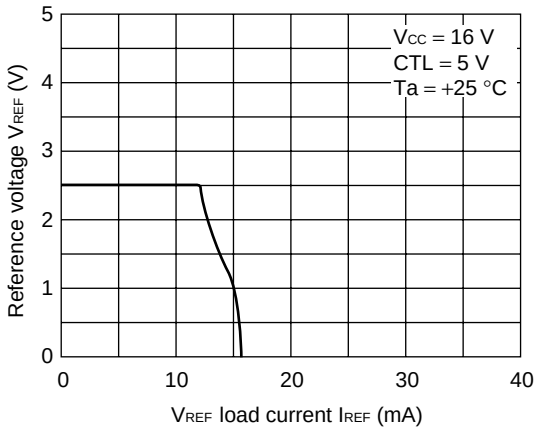
*: Standard design value

■ TYPICAL CHARACTERISTICS

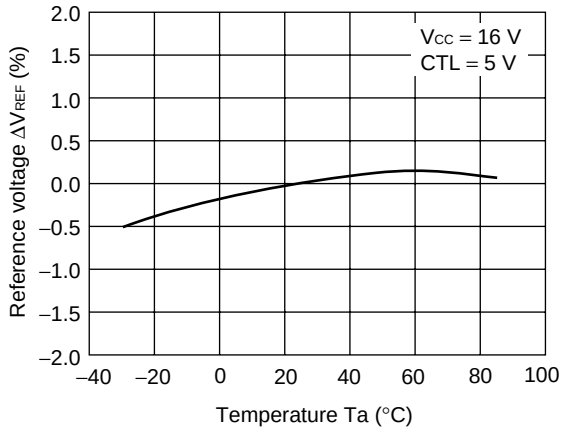
Reference voltage vs. power supply voltage characteristics



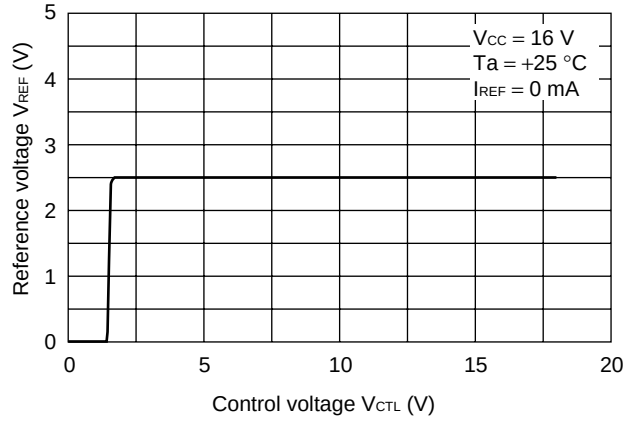
Reference voltage vs. V_{REF} load current characteristics



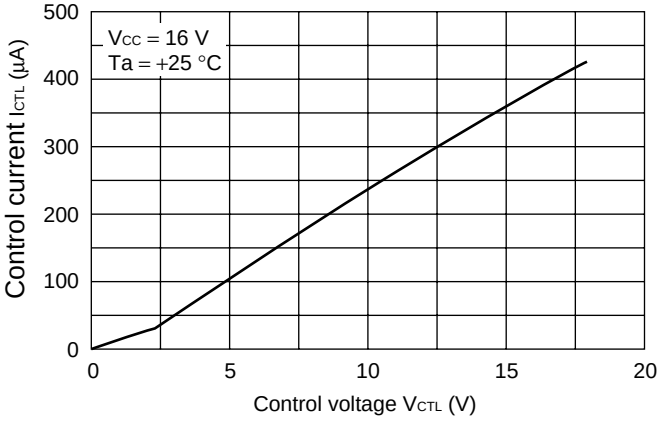
Reference voltage vs. temperature characteristics



Reference voltage vs. control voltage characteristics



Control current vs. control voltage characteristics



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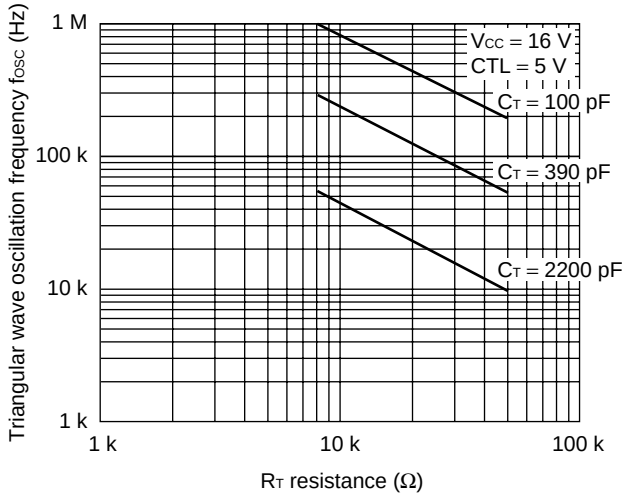
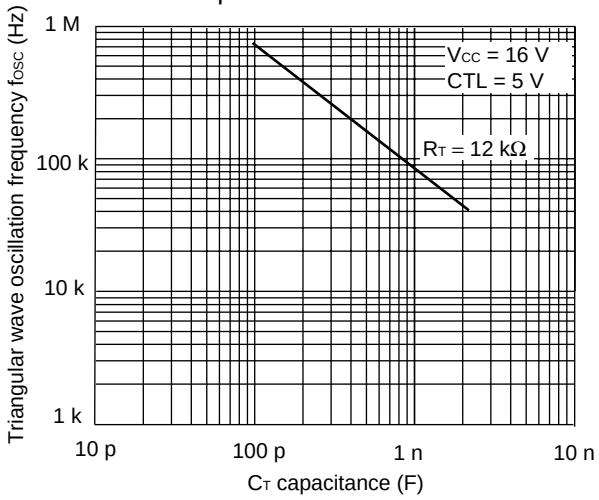
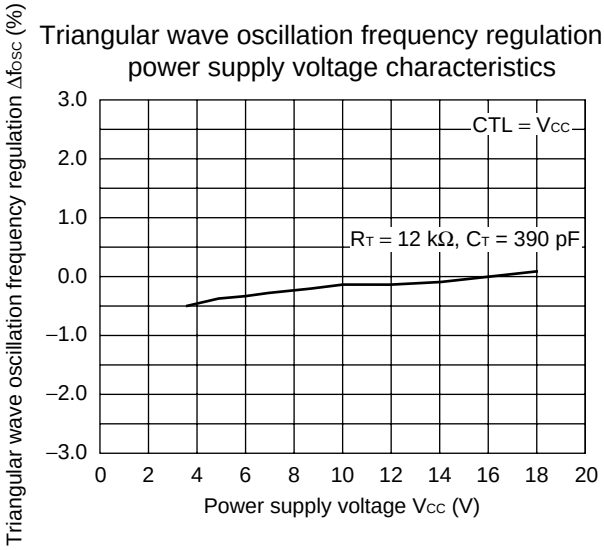
Triangular wave oscillation frequency vs. R_T resistance characteristics



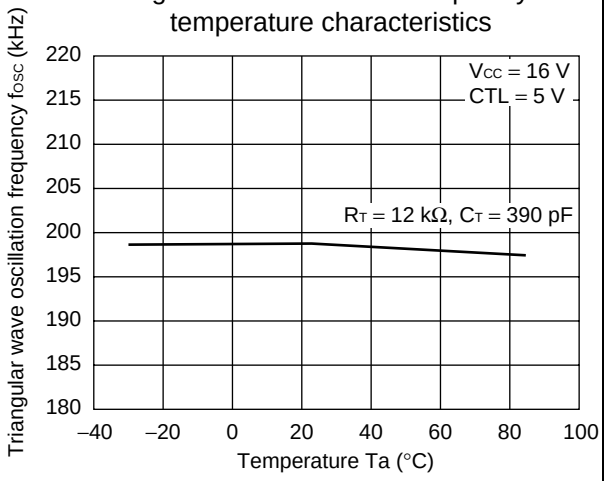
Triangular wave oscillation frequency vs. C_T capacitance characteristics



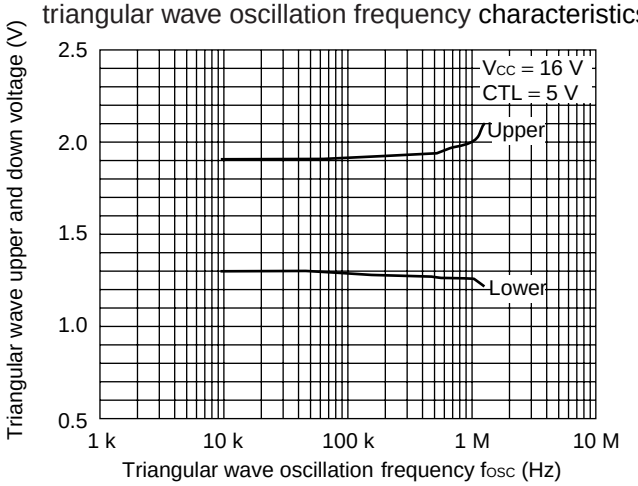
Triangular wave oscillation frequency regulation vs. power supply voltage characteristics



Triangular wave oscillation frequency vs. temperature characteristics



Triangular wave maximum/minimum voltages vs. triangular wave oscillation frequency characteristics



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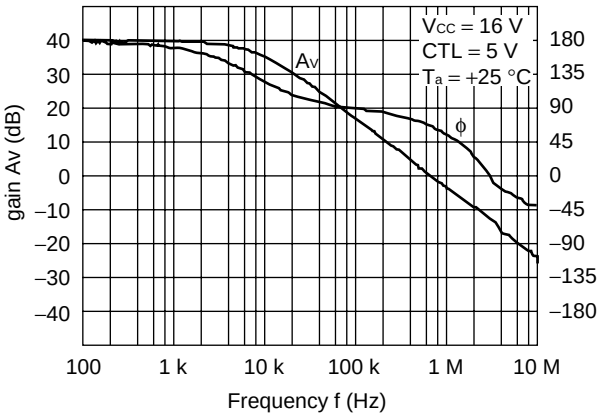
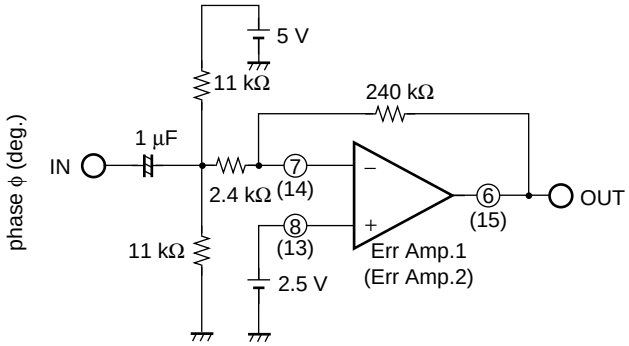
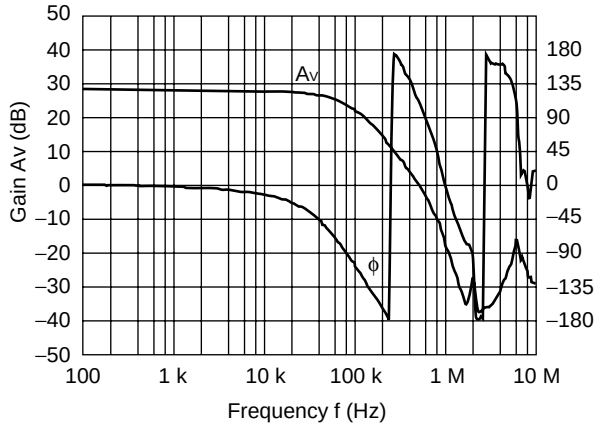
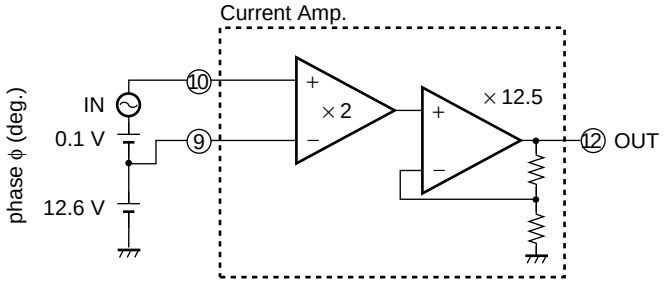
Error amp. gain, phase vs. frequency characteristics



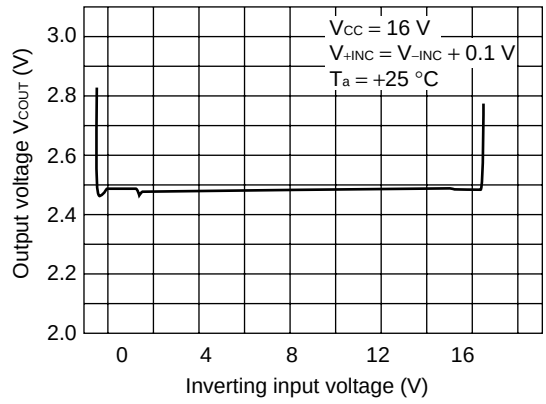


Current detector amp. gain, phase vs. frequency characteristics





Current detector amp. output voltage vs. input voltage characteristics



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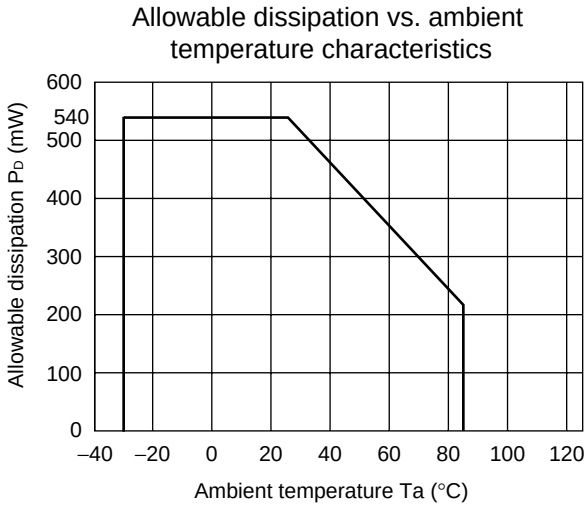

Allowable dissipation vs. ambient temperature characteristics
Allowable dissipation P_D (mW)
600
540
500
400
300
200
100
0
–40
–20
0
20
40
60
80
100
120
Ambient temperature Ta (°C)

■ FUNCTIONAL DESCRIPTION

1. Switching Regulator Functions

(1) Reference voltage circuit (Ref)

The reference voltage generator uses the voltage supplied from the V_{CC} terminal (pin 18) to generate a temperature-compensated, stable voltage (about 2.50 V) as the reference supply voltage for the IC's internal circuitry.

The reference voltage can be output, up to 1 mA, to an external device through the VREF terminal (pin 1).

(2) Triangular wave oscillator (OSC)

The triangular wave oscillator generates a triangular waveform with a timing capacitor and a timing resistor respectively connected to the CT terminal (pin 3) and RT terminal (pin 2).

The triangular wave is input to the PWM comparator in the IC while it can also be supplied to an external device through the CT terminal. In addition, the oscillator can be used for external synchronization, where it generates a triangular wave synchronous to the input signal from the SYNC terminal (pin 4).

(3) Error amplifiers (Error Amp. 1, 2)

The error amplifiers detect the output voltage from the switching regulator and outputs the PWM control signal. It supports a wide range of in-phase inputs from 0 V to "V_{CC} – 0.9 V". An arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the FB1 terminal (pin 6) [FB2 terminal (pin 15)] to the –IN1 terminal (pin 7) [–IN2 terminal (pin 14)] of the error amplifier, enabling stable phase compensation to the system.

(4) Current detector amplifier (Current Amp.)

The current detector amplifier provides 25 × amplification of the voltage drop between the two ends of the output sensor resistor (RS) in the switching regulator, that occurs due to the flow of the charging current. At the same time, the amplifier converts the voltage to the GND-reference voltage level and outputs it to the COUT terminal (pin 12). It can also control the charging current in combination with the error amplifier circuit.

(5) Power control circuit (CTL)

The power control circuit can control turning on and off the power supply through the CTL terminal (pin 17). (Supply current in standby mode: About 0 μA)

Depending on the voltage level of the PWM Comp. input terminal, the OUT terminal (pin 19) may become "L" level during discharging of the V_{REF} voltage after the CTL terminal is turned off with a capacitor connected to the V_{REF} terminal. The power control circuit contains a function for fixing the OUT output terminal to the "H" level when CTL = "L" and VREF = "H", preventing inadvertent "L" level output after turning the CTL terminal off.

(6) PWM comparator circuit (PWM Comp.)

The PWM comparator circuit is a voltage-pulse width converter for controlling the output duty of the error amplifiers (Error Amp. 1, 2) depending on their output voltage.

The PWM comparator circuit turns on the external output transistor during the interval in which the triangular wave voltage level is lower than the voltage level at both of the error amplifier output terminals (FB1 terminal (pin 6), FB2 terminal (pin 15)) and the DTC terminal (pin 16).

(7) Output circuit (Out)

The output circuit uses a totem-pole configuration, capable of driving an external P-channel MOS FET and PNP transistor. It can also control the output sink current with a resistor connected between the VE terminal (pin 20) and the GND terminal (pin 11).

2. Protection Functions

(1) Low input voltage malfunction preventive circuit (ULVO)

The transient state or a momentary decrease in supply voltage, which occurs when the power supply is turned on, may cause errors in the control IC, resulting in breakdown or degradation of the system. The low input voltage malfunction preventive circuit detects the internal reference voltage level according to the supply voltage and turn off the external output transistor to make dead time 100%. The circuit restores voltage supply when the supply voltage reaches its threshold voltage.

(2) Timer-latch short-circuit protection circuit (SCP Comp., SR Latch)

The latch circuit detects the output voltage levels of the error amplifiers. When the output voltage levels of the two error amplifiers reach about 2.1 V at the same time, the timer circuit is actuated to start charging the external capacitor connected to the CSCP terminal (pin 5). If the error amplifier outputs are not restored to the normal voltage range before the capacitor voltage reaches about 0.7 V, the latch circuit is actuated to fix the output terminals (OUT) at the “H” level. To reset the actuated protection circuit, turn the power supply on back.

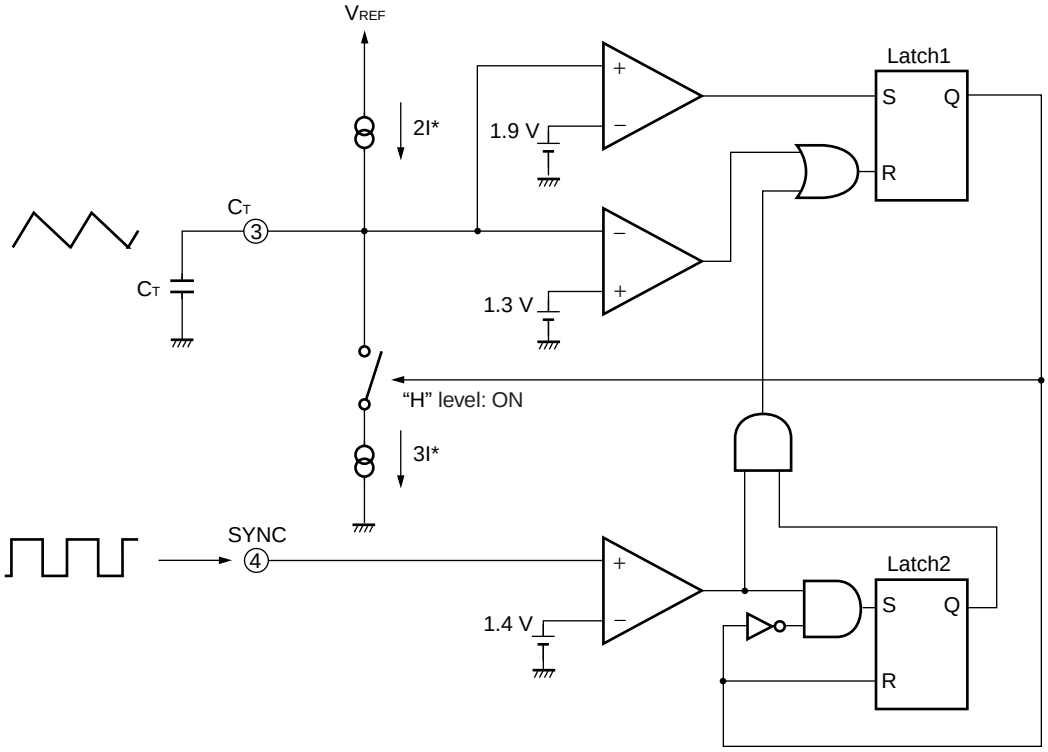
■ METHOD OF SETTING FOR EXTERNAL SYNCHRONOUS OSCILLATION

For external synchronous oscillation, connect a timing capacitor (C_T), a timing resistor (R_T), and an external sync signal to the CT, RT, and SYNC terminals, respectively.

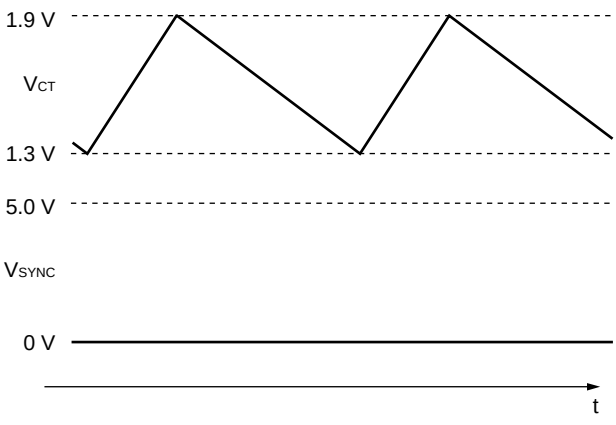
In this case, select the C_T and R_T so that the oscillation frequency is 5% to 10% lower than the frequency of the external synchronous signal excluding the setting error of the oscillation frequency.

The duty cycle (t1/ t) of the external sync signal must be set within a range from 10% to 90%.

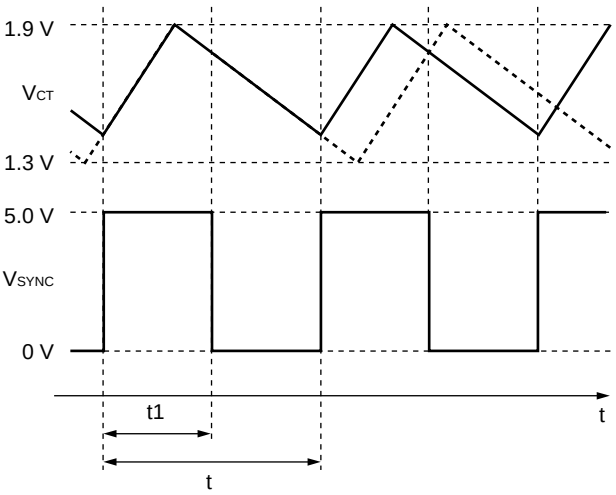
<Triangular wave oscillator (OSC) equivalent circuit>



<Free-run oscillation>



<External synchronous oscillation>

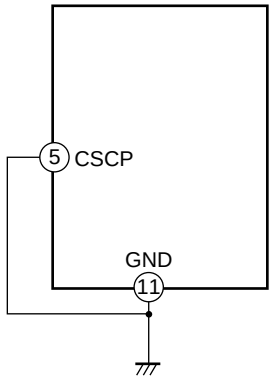


*: | = VRT/R_T, VRT (pin voltage at pin 2) = 1.0 V (typical)

■ TREATMENT OF UNUSED CSCP PIN

When the timer-latch short-circuit protection circuit is not used, connect the CSCP terminal (pin 5) to the GND at the shortest distance.

Treatment of the CSCP terminal when not used



■ OSCILLATOR FREQUENCY SETTING

The oscillator frequency can be set by connecting a timing capacitor (C_T) to the CT terminal (pin 3) and a timing resistor (R_T) to the RT terminal (pin 2).

Oscillator frequency: fosc

$$\text{fosc (kHz)} \fallingdotseq \frac{936000}{C_T\text{(pF)} \cdot R_T\text{(k}\Omega\text{)}}$$

■ METHODS OF SETTING THE DEAD TIME

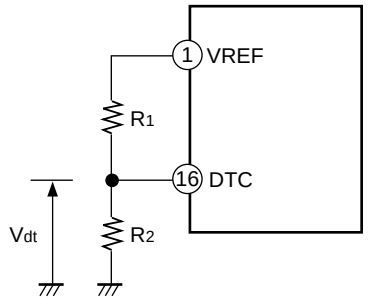
When the device is set for step-up inverted output based on the flyback method, the output transistor is fixed to a full-ON state (ON duty = 100%) when the power supply is turned on. To prevent this problem, you may determine the voltage at the DTC terminal (pin 16) from the V_{REF} voltage so you can set the output transistor's dead time (maximum ON-duty period) as shown in Figure a below.

When the voltage at the DTC terminal (pin 16) is higher than the triangular wave output voltage from the oscillator, the output transistor is turned off. The dead time calculation formula assuming that triangular wave amplitude ≒ 0.6 V and triangular wave minimum voltage ≒ 1.3 V is given below.

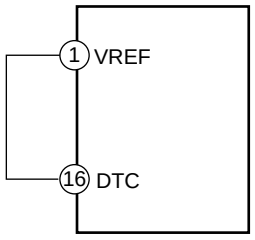
$$\text{Duty (ON)} \fallingdotseq \frac{V_{dt} - 1.3\ V}{0.6\ V} \times 100\ [\%],\ V_{dt} = \frac{R_2}{R_1 + R_2} \times V_{REF}$$

When the DTC terminal is not used, connect it directly to the VREF terminal.

- **Figure a Setting the dead time**



- **Figure b Not setting the dead time**



■ METHODS OF SETTING THE SOFT START TIME

To prevent surge currents when the IC is turned on, you can set a soft start using the DTC terminal (pin 16).

When power is switched on, the current begins charging the capacitor (Cdt) connected the DTC terminal. The soft start process operates by comparing the soft start setting voltage, which is proportional to the DTC terminal voltage, with the triangular waveform, and varying the ON-duty of the OUT terminal (pin 19).

The soft start time until the ON duty reaches 50 % is determined by the following equation:

For figure c

Soft start time (time until output ON duty = 50%)

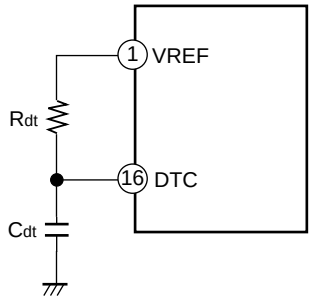
$$ts\ (s) = C_{dt}\ (F) \times R_{dt}\ (\Omega) \times \ln(1 - 1.6/2.5) \fallingdotseq 1.022 \times C_{dt}\ (F) \times R_{dt}\ (\Omega)$$

For figure d

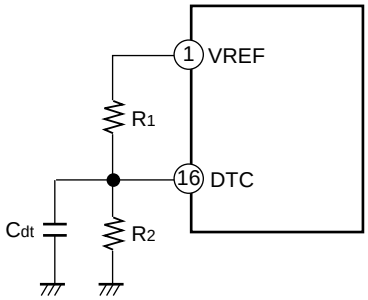
Soft start time (time until output ON duty = 50%)

$$ts\ (s) = -\frac{C_{dt}\ (F) \times R_1\ (\Omega) \times R_2\ (\Omega)}{R_1\ (\Omega) + R_2\ (\Omega)} \times \ln\left(1 - \frac{1.6\ (R_1\ (\Omega) + R_2\ (\Omega))}{2.5 R_2\ (\Omega)}\right)$$

- **Figure c Setting a soft start**

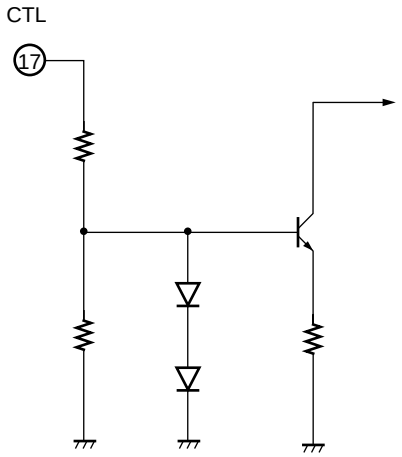


- **Figure d Setting the dead time and a soft start**

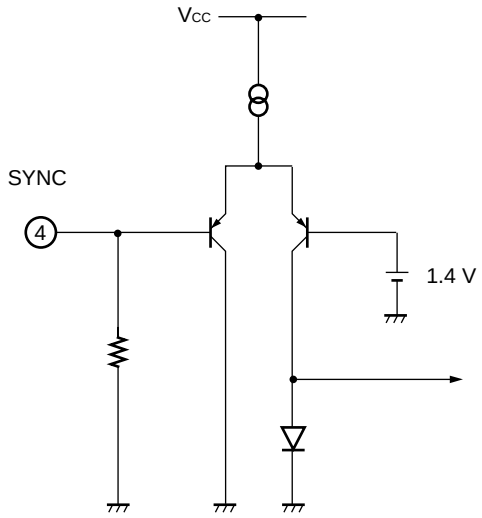


■ EQUIVALE CIRCUIT (CTL, SYNC terminal)

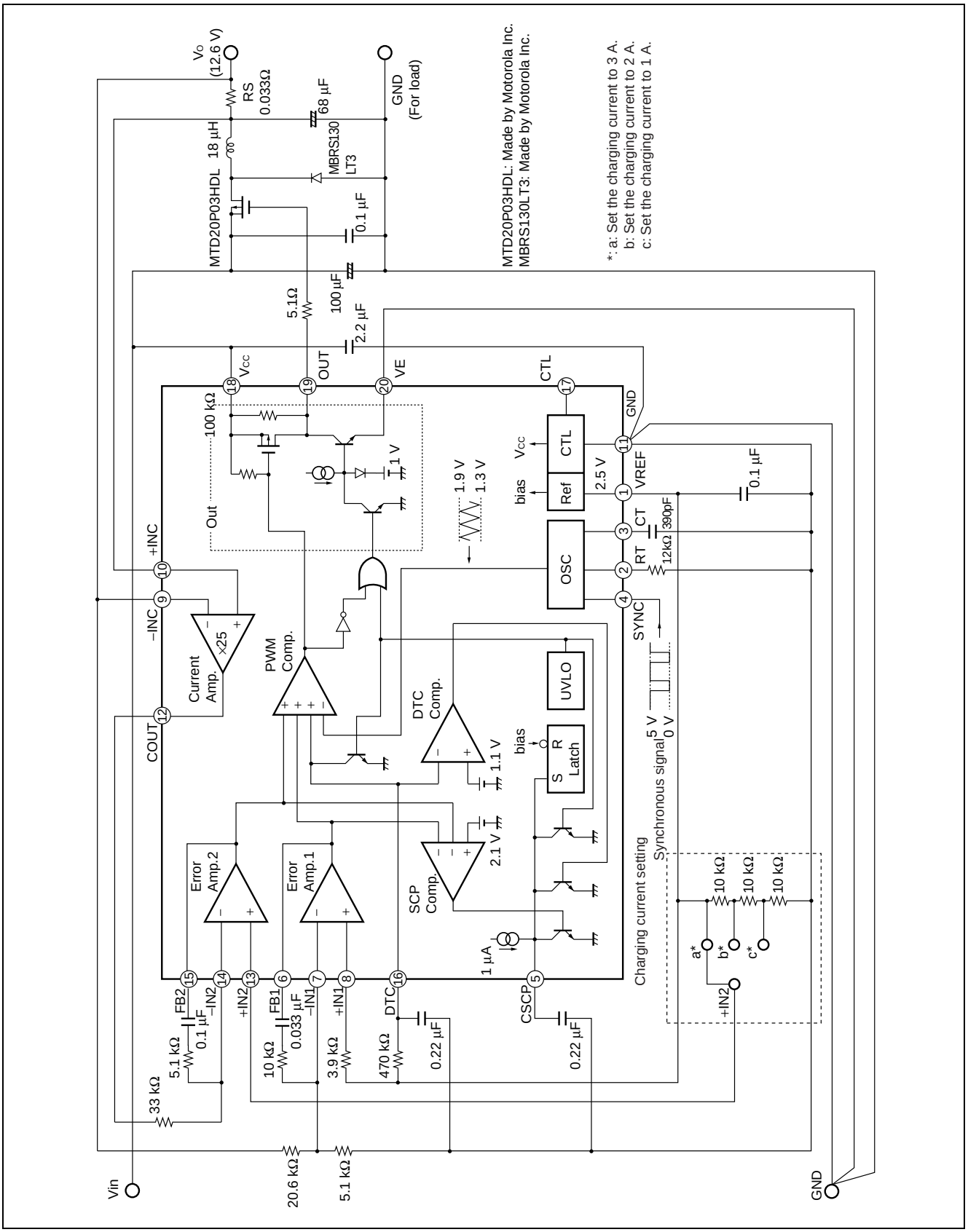
- **CTL terminal**



- **SYNC terminal**

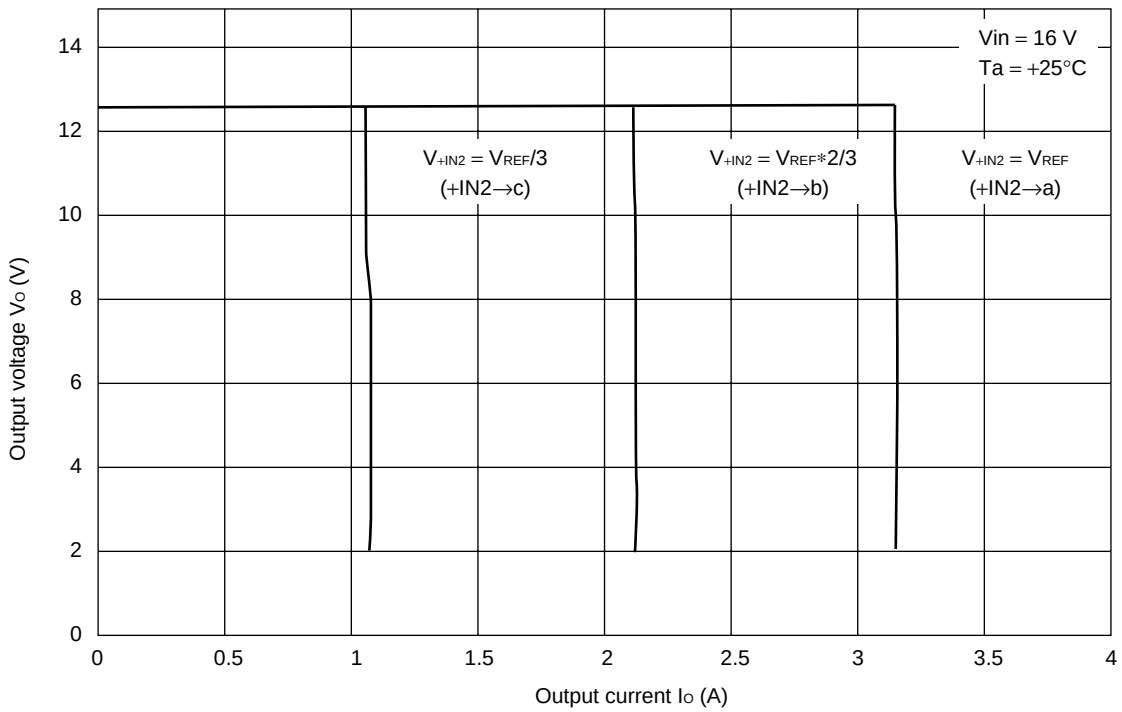


■ APPLICATION EXAMPLE (Step-down scheme)

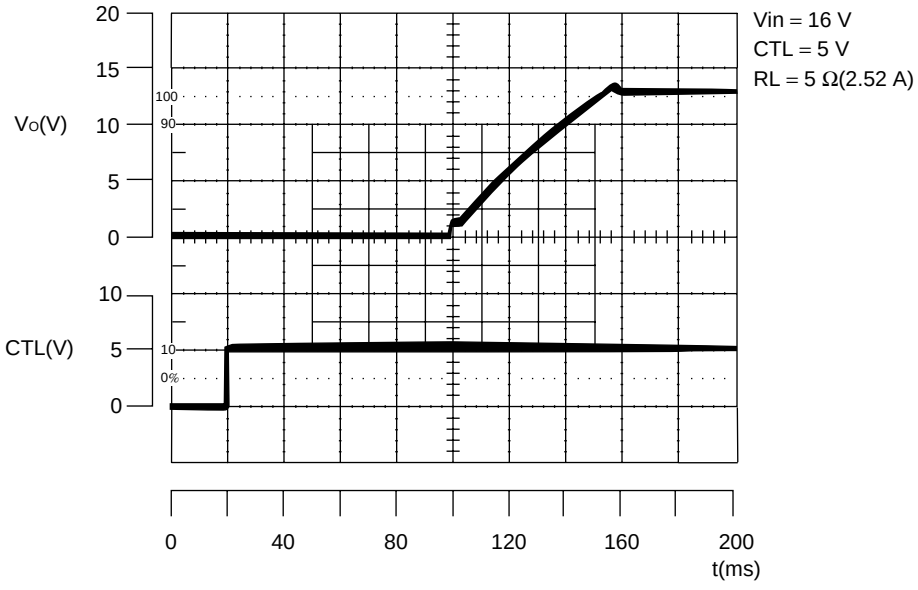


■ REFERENCE DATA

Output voltage vs. output current characteristics



Soft start operation waveforms



■ NOTES ON USE

- Take account of common impedance when designing the earth line on a printed wiring board.

- Take measures against static electricity.
  - For semiconductors, use antistatic or conductive containers.
  - When storing or carrying a printed circuit board after chip mounting, put it in a conductive bag or container.
  - The work table, tools and measuring instruments must be grounded.
  - The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.

- Do not apply a negative voltage
  - Applying a negative voltage of –0.3 V or less to an LSI may generate a parasitic transistor, resulting in malfunction.

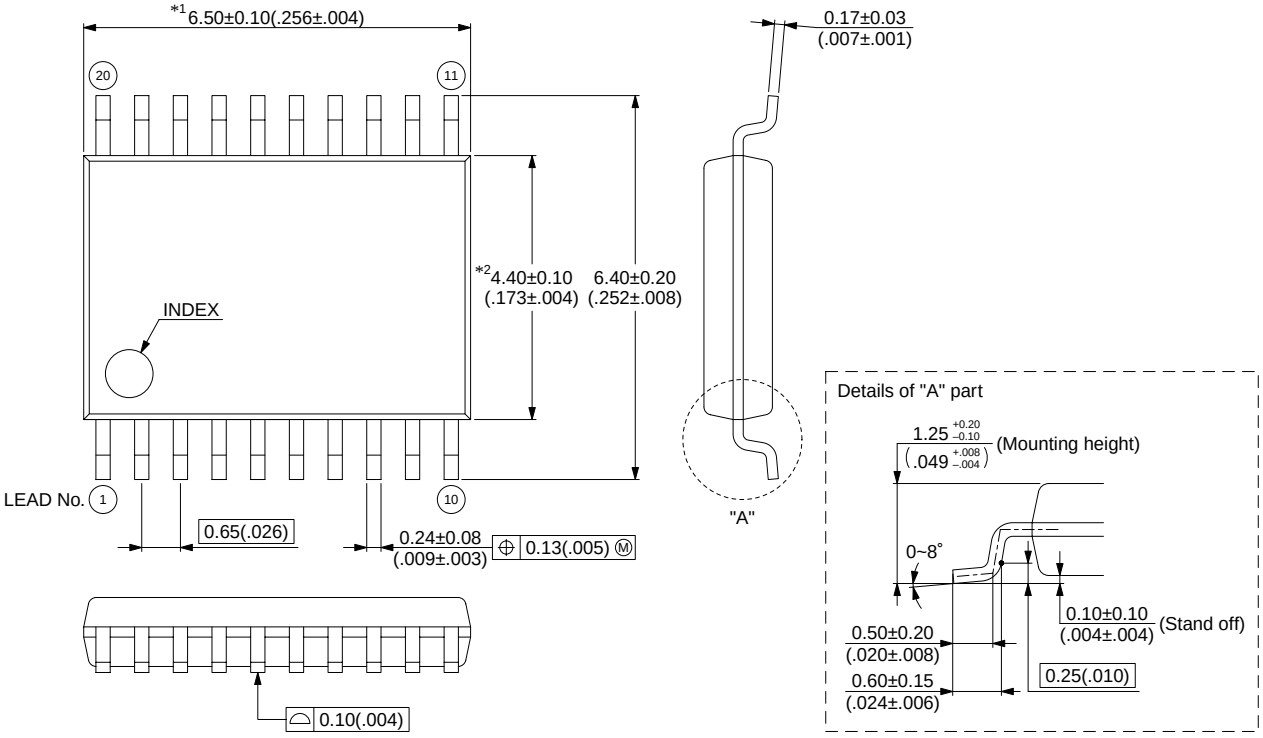
■ ORDERING INFORMATION

Part number	Package	Remarks
MB3832APFV	20-pin Plastic SSOP (FPT-20P-M03)	

■ PACKAGE DIMENSION

20-pin Plastic SSOP
(FPT-20P-M03)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max) .
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

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