3.3V Zero-Delay Buffer

Features

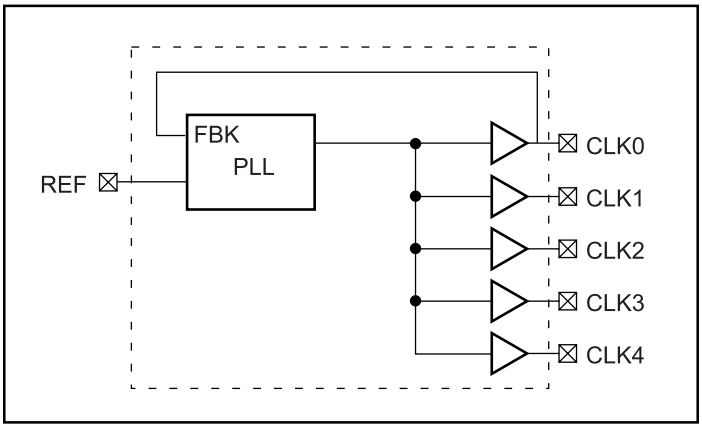
- Zero-input-output propagation delay
- 350ps phase error
- Multiple low-skew outputs
  - Output-output skew less than 250ps
  - Device-device skew less than 700ps
- 10 MHz to 100 MHz operating range
- Low Jitter <200ps
- High drive option (PI6C2305-1H)
- 3.3V operation
- Commercial Operation: 0°C to +70°C
- Industrial Operation: –40°C to +85°C
- Package: Space-saving 8-pin, 150-mil SOIC package (W)

Description

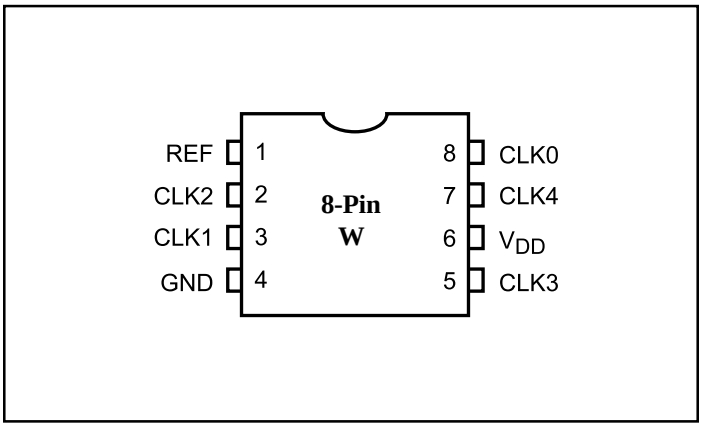
Providing five low-skew clocks, the PI6C2305-1 is a 3.3V zero-delay buffer designed to distribute clock signals in applications including PC, workstation, datacom, telecom, and high-performance systems.

The PI6C2305-1 provides 5 copies of clocks that have less than 350ps propagation delay compared to a reference clock. The skew among the output clock signals for PI6C2305-1 is less than 250ps. When there are no rising edges on the REF input, the PI6C2305-1 enters a power-down state. In this mode, the PLL is off and all outputs are three-stated. This results in less than 50µA of current draw. Featuring faster rise and fall times, the PI6C2305-1H is the high-drive version of the PI6C2305-1.

Block Diagram



Pin Configuration



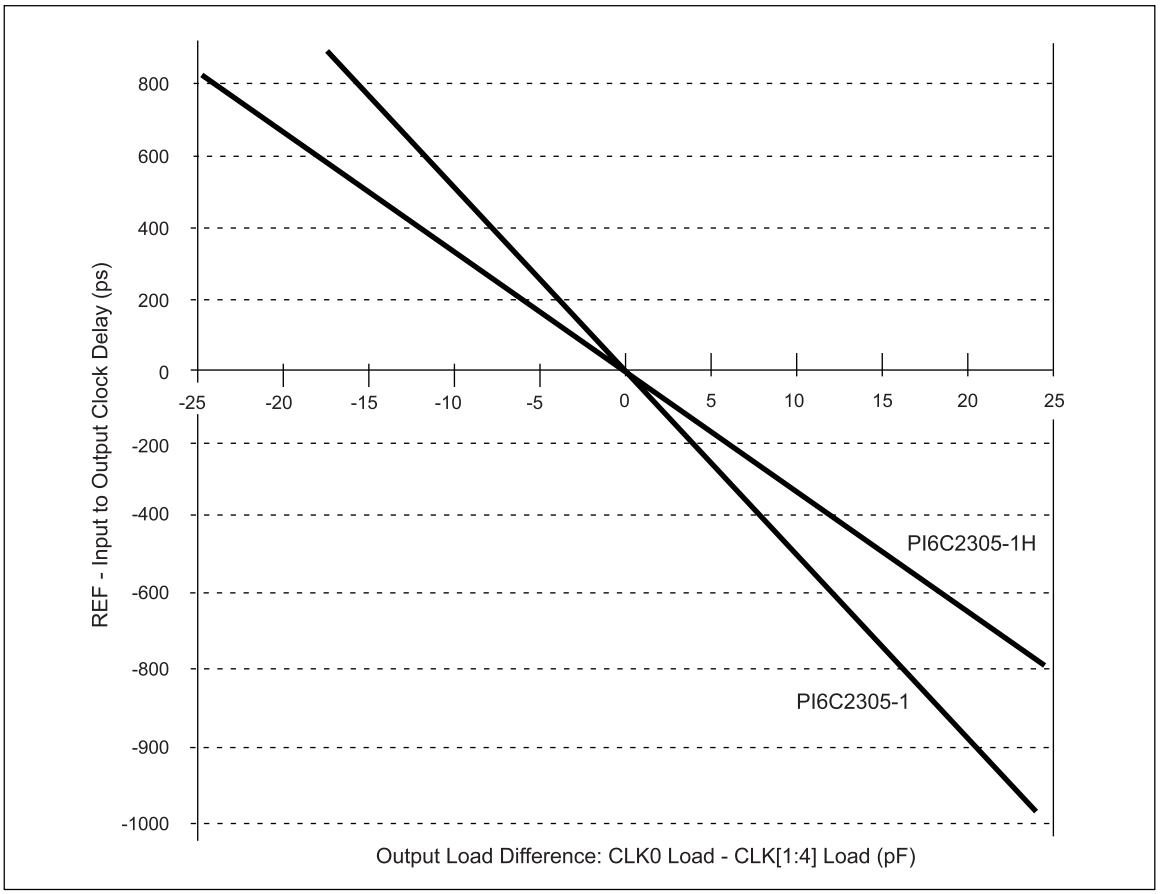
Pin Description

Pin	Signal	Description
1	REF(1)	Input reference frequency, 5V Tolerant input
2	CLK2(2)	Buffered Clock output
3	CLK1(2)	Buffered Clock output
4	GND	Ground
5	CLK3(2)	Buffered Clock output
6	V_{DD}	3.3V Supply
7	CLK4(2)	Buffered Clock output
8	CLK0(2)	Buffered Clock output, internal feedback on this pin

Notes:
1. Weak pull-down.
2. Weak pull-down on all outputs.

Zero-Delay and Skew Control

REF. Input to CLK[1:4] Delay vs. Difference in Loading between CLK[0] pin and CLK[1:4] pins.



To achieve a Zero Delay between the input and output, all outputs should be uniformly loaded. The relative loading of CLK0 (with respect to the remaining outputs) can adjust the input-output delay. This is shown in the graph above.

For applications requiring zero input-output delay, all outputs including CLK0 should be equally loaded. Even if CLK0 is not used, it must have a capacitive load that is equal to that on every other output. If input-output delay adjustments are required, use the above graph to calculate loading differences between the feedback output and remaining outputs.

Maximum Ratings

Supply Voltage to Ground Potential	–0.5V to +7.0V
DC Input Voltage (Except REF)	–0.5V to V_{DD} +0.5V
DC Input Voltage REF	–0.5 to 7V
Storage Temperature	–65° C to +150°C
Maximum Soldering Temperature (10 seconds)	260°C
Junction Temperature	150°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2000V

Operating Conditions

Parameter	Description	Min.	Max.	Units
V_{DD}	Supply Voltage	3	3.6	V
T_A (2305, 2305-1H)	Commercial Temperature (Ambient)	0	70	°C
T_A (2305I-2305-1HI)	Industrial Temperature (Ambient)	–40	85	
C_L	Load Capacitance	—	30	pF
C_{IN}	Input Capacitance	—	7	

Electrical Characteristics (Over operating conditions)

Parameter	Description	Test Conditions	Min.	Max.	Units
V_{IL}	Input LOW Voltage[3]	—	—	0.8	V
V_{IH}	Input HIGH Voltage[3]	—	2.0	—	
I_{IL}	Input LOW Current	V_{IN} = 0V	—	50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	—	200.0	
V_{OL}	Output LOW Voltage[4]	I_{OL} = 8mA (2305-1) I_{OL} = 12mA (2305-1H)	—	0.4	V
V_{OH}	Output HIGH Voltage[4]	I_{OH} = –8mA (2305-1) I_{OH} = –12mA (2305-1H)	2.4	—	
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz	—	50.0	µA
I_{DD}	Supply Current	Unloaded outputs, 66.66 MHz,	—	50.0	mA

Notes:
3. REF and CLK0 inputs have a threshhold voltage of $V_{DD}/2$.
4. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics[4, 5] (Over operating conditions)

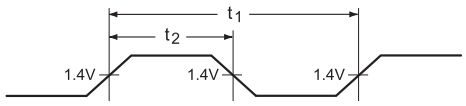
Parameters	Name	Test Conditions	Min.	Typ.	Max.	Units
F_{CLK}	Output Frequency	30pF load	10		100	MHz
	Duty Cycle[4] = $t_2 \div t_1$	Measured at $V_{DD}/2$, F_{OUT} < 66.66 MHz	45	50	55	%
	Duty Cycle[4] = $t_2 \div t_1$	Measured at 1.4V, $F_{OUT} \leq 45$ MHz	40	50	60	
t_3	Rise Time[4] @30pF	Measured between 0.8V and 2.0V			2.5	ns
t_3	Rise Time[4]@30pF (H)				1.5	
t_4	Fall Time[4] @30pF				2.5	
t_4	Fall Time[4]@30pF (H)				1.5	
t_5	Output to Output Skew[4]	All outputs equally loaded			250	ps
t_6	Delay, REF Rising Edge to CLK0 Rising Edge[4]	Measured at $V_{DD}/2$		0	±350	
t_7	Device to Device Skew[4]	Measured at $V_{DD}/2$ on the output pins of devices		0	700	
t_8	Output Slew Rate[4]	Measured between 0.8V and 2.0V on -H device using Test Circuit #2	1			V/ns
t_J	Cycle to Cycle Jitter[4]	Measured at 66.67 MHz, loaded outputs			200	ps
t_{LOCK}	PLL Lock Time[4]	Stable power supply, valid clocks presented on REFpins			1.0	ms

Notes:

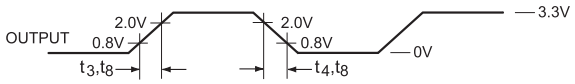
4. Parameter is guaranteed by design and characterization. Not 100% tested in production.
5. For definition of t_{1-8}, see Switching Waveforms on page 5.

Switching Waveforms

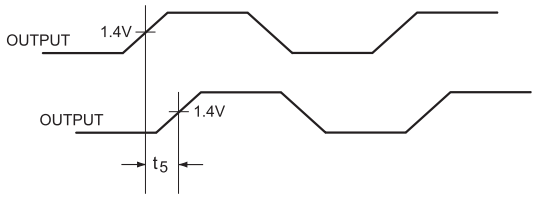
Duty Cycle Timing



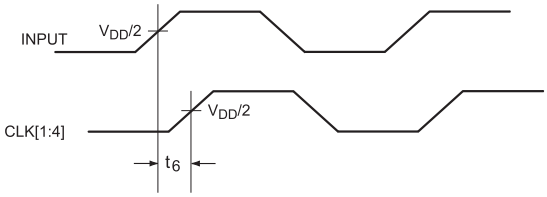
All Outputs Rise/Fall Time



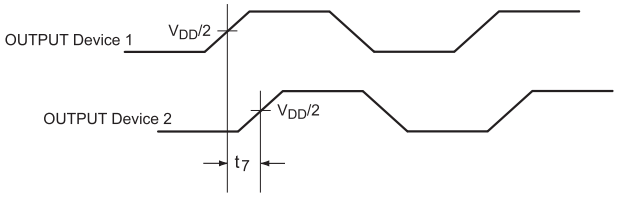
Output-Output Skew



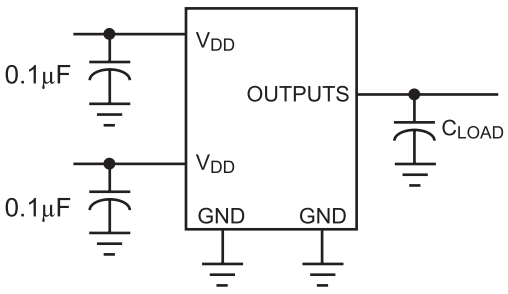
Input-Output Propagation Delay



Device-Device Skew

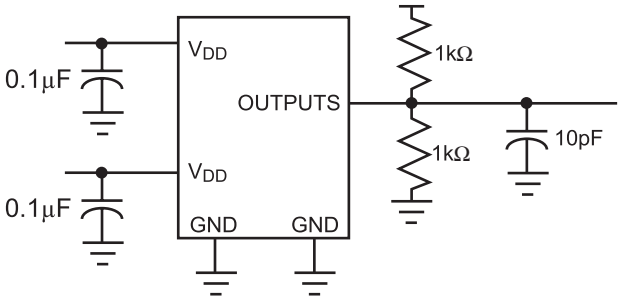


Test Circuit #1



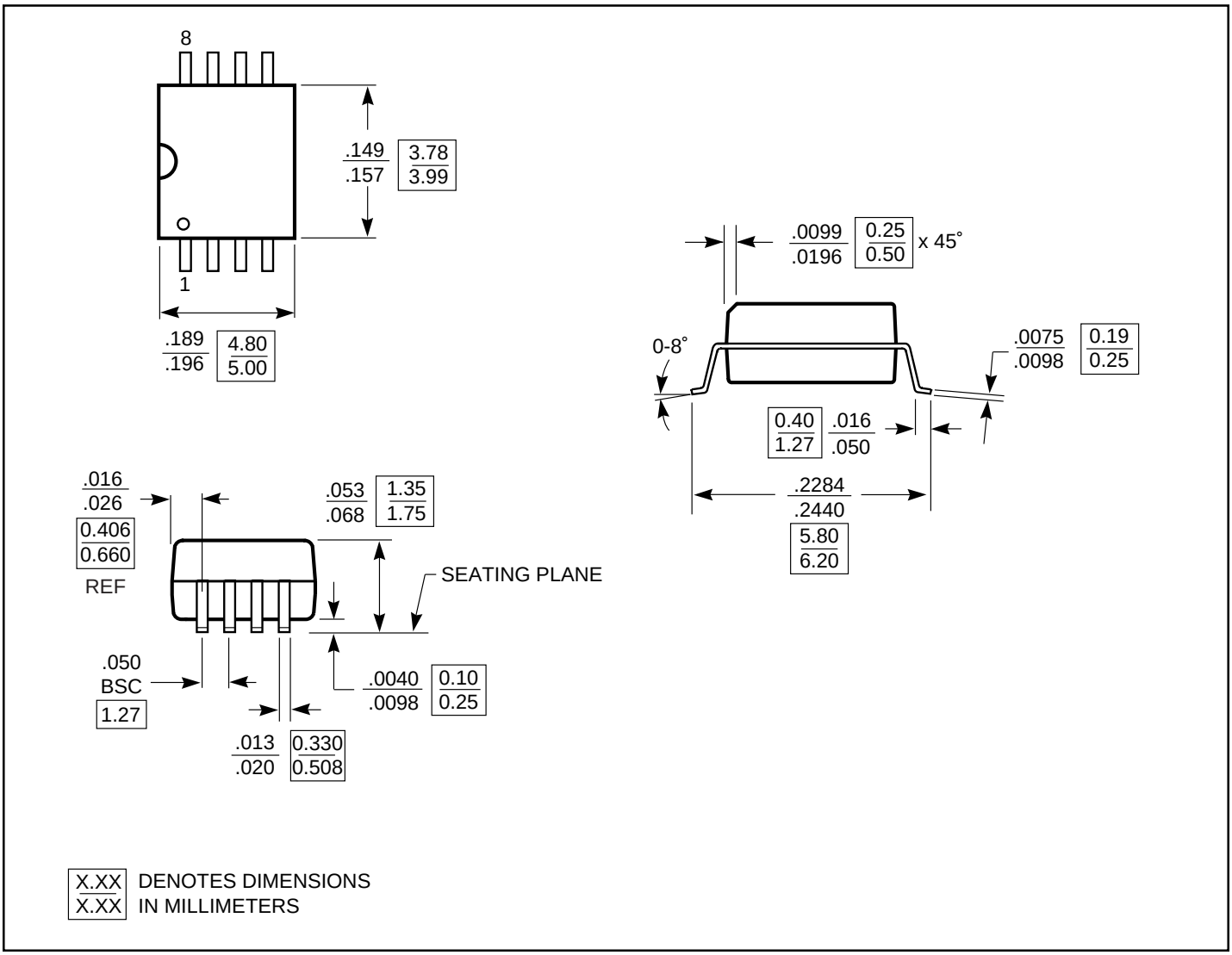
Test Circuit for all parameters except t_8

Test Circuit #2



Test Circuit for t_8 ,Output slew rate on PI6C2305-1H device

8-Pin SOIC Package Mechanical (W)



Ordering Information

Ordering Code	Description	Package Type	Operating Range
PI6C2305-1W	Normal Drive	8-pin 150-mil SOIC	Commercial
PI6C2305-1HW	High Drive		
PI6C2305-1WI	Normal Drive	8-pin 150-mil SOIC	Industrial
PI6C2305-1HWI	High Drive		