Z84C01 Z80® CPU with Clock Generator/Controller

FEATURES:

- Commands compatible with the Zilog Z80 MPU
- Low power consumption
  - 40mA Typ (5V, 10 MHz under RUN mode)
  - 2mA Typ (5V, 10 MHz under IDLE1 mode)
  - 10mA Typ (5V, 10 MHz under IDLE2 mode)
  - 5 µA Typ (5V under STOP mode)
- DC to 10 MHz operation (at 5V±10%)
- Single 5V power supply (at 5V±10%)
- Operating temperature (0° C to 70° C)
- On-chip clock generator

  In the HALT state, the following 4 modes are selectable:
  - RUN mode
  - IDLE 1 mode
  - IDLE 2 mode
  - STOP mode
- Powerful set of 158 instructions
- Powerful interrupt function
  - Non-maskable interrupt terminal ($\overline{NMI}$)
  - Maskable interrrupt terminal ($\overline{INT}$)

  The following three modes are selectable:
  - 8080 compatible interrupt mode (interrupt by Non-Z80 family peripheral LSI) (Mode 0)
  - Restart interrupt (Mode 1)
  - Daisy-chain structure interrupt using Z80 family peripheral LSI (Mode 2)
- An auxiliary register provided to each of general purpose registers.
- 2 index registers

  10 addressing modes
- Built-in refresh circuit for dynamic memory
- 44-Pin PLCC or QFP Package

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GENERAL DESCRIPTION:

The Z84C01 is an 8-bit microprocessor (hereinafter referred to as MPU) with a built-in clock generator/controller, which provides low power operation and high performance.

Built into the Z84C01 is a control function and clock generator for the standby function in addition to: six paired general purpose registers, accumulator, flag registers, an arithmetic-and-logic unit, bus control, memory control and timing control circuits.

The Z84C01 is fabricated with Zilog CMOS technology and molded in a 44-pin PLCC or QFP packages.

Further, in the following text and explanations for charts and tables, hexadecimal numbers are directly used without giving an identification to explanation of address, etc. so as not to cause confusions.

PIN CONNECTIONS AND PIN FUNCTIONS:

The pin connections and I/O pin names and brief functions of the Z84C01 are shown below.

Pin Connections. The pin connections of the Z84C01 are as shown in Fig. 1.

Pin Names and Functions. I/O pin names and functions are as shown in Table 1.

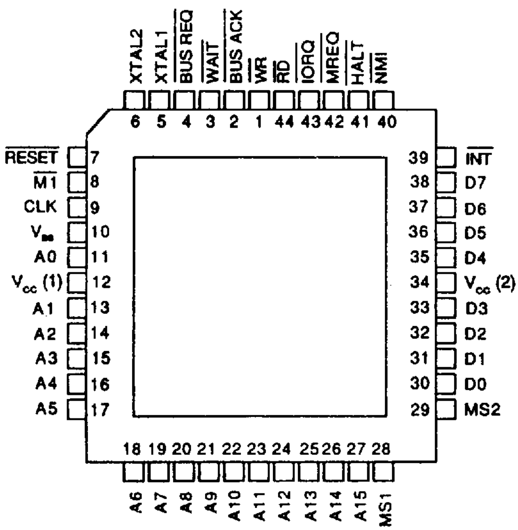

Figure 1. Pin Connections (Top View)

Table 1 Pin Names and Functions

Pin Name	Number of Pin	Input/Output 3-state	Function
A0 - A15	16	Output 3-state	16-bit address bus. Specify addresses of memories and I/O to be accessed. During the refresh period, addresses for refreshing are output.
MS1, MS2	2	Input	Mode selection input. One of 4 modes (Run, IDLE1/2, STOP) is selected according to the state of these 2 pins.
D0 - D7	8	I/O 3-state	8-bit bidirectional data bus.
INT	1	Input	Maskable interrupt request signal. Interrupt is generated by peripheral LSI. This signal is accepted if the interrupt enable flip-flop (IFF) is set at "1". INT is normally wired-OR and requires an external pull up for these applications.

Table 1 Pin Names and Functions (continued)

Pin Name	Number of Pin	Input/Output 3-state	Function
$\overline{NMI}$	1	Input	Non-maskable interrupt request signal. This interrupt request has the higher priority than the maskable interrupt request and does not rely upon the state of the interrupt enable flip-flop (IFF).
$\overline{HALT}$	1	Output	Halt signal. Indicates that the CPU has executed a Halt instruction.
$\overline{MREQ}$	1	Output 3-state	Memory request signal. When an effective address for memory access is on the address bus, "0" is output.
$\overline{IORQ}$	1	Output 3-state	I/O request signal. When addresses for I/O are on lower 8 bits (A0 - A7) of the address bus in the I/O operation, "0" is output. In addition, $\overline{IORQ}$ signal is output together with $\overline{M1}$ signal at time of interrupt acknowledge cycle to inform peripheral LSI of the state that the interrupt response vector may be put on the data bus.
$\overline{RD}$	1	Output 3-state	Read signal. "0" signal is output for a period when MPU can receive data from a memory or peripheral LSI. It is possible to put data from a specified peripheral LSI or mamory on the MPU data bus after gating by this signal.
$\overline{WR}$	1	Output 3-state	Write signal. This signal is output when data to be stored in a specified memory or peripheral LSI is on the MPU data bus.
$\overline{BUSACK}$	1	Output	Bus acknowledge signal. In response to $\overline{BUSREQ}$ signal, this signal informs a peripheral LSI of the fact that the address bus, data bus, MREQ, IORQ, RD and WR signals have been placed in the high impedance state.
$\overline{WAIT}$	1	Input	Wait signal. $\overline{WAIT}$ signal is a signal to inform MPU of specified memory or peripheral LSI which is not ready for data transfer. As long as WAIT signal as at "0" level, MPU is continuously kept in the wait state.
$\overline{BUSREQ}$	1	Input	Bus request signal. $\overline{BUSREQ}$ signal is a signal requesting placement of the address bus, data bus, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$ signals in the high impedance state. $\overline{BUSREQ}$ signal is normally wired-OR. In this case, a pull-up resistor is externally connected.

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Table 1 Pin Names and Functions (continued)

Pin Name	Number of Pin	Input/Output 3-state	Function
$\overline{RESET}$	1	Input	Reset signal. $\overline{RESET}$ signal is used for initializing MPU and must be kept in active state ("0") for a period of at least 3 clocks.
$\overline{M1}$	1	Output	Signal showing machine cycle 1. "0" is output together with $\overline{MREQ}$ signal in the operation code fetch cycle. This signal is output for every opcode fetch when 2 byte opcode is executed. In the maskable interrupt acknowledge cycle, this signal is output together with IORQ signal.
XTAL 1 (XIN) XTAL 2 (XOUT)	2	Input Output	Crystal oscillator connecting terminal.
CLK	1	Output	Single-phase clock output. Clock polarity is in-phase with OSC-IN (XTAL 1) so that Z80 users could use OSC-IN as clock input without needing extra inverter on the board. When the HALT in struction in STOP Mode is executed, MPU stops its operation and holds clock output at "0" level.
VCC (1), (2)	2	Power supply	+5V Connect pin 34 and pin 12 externally.
VSS	1	Power supply	0V

FUNCTIONAL DESCRIPTION:

The system configuration, functions and basic operation of the Z84C01 are described here.

Block Diagram. The block diagram of the internal configuration is shown in Fig. 2.

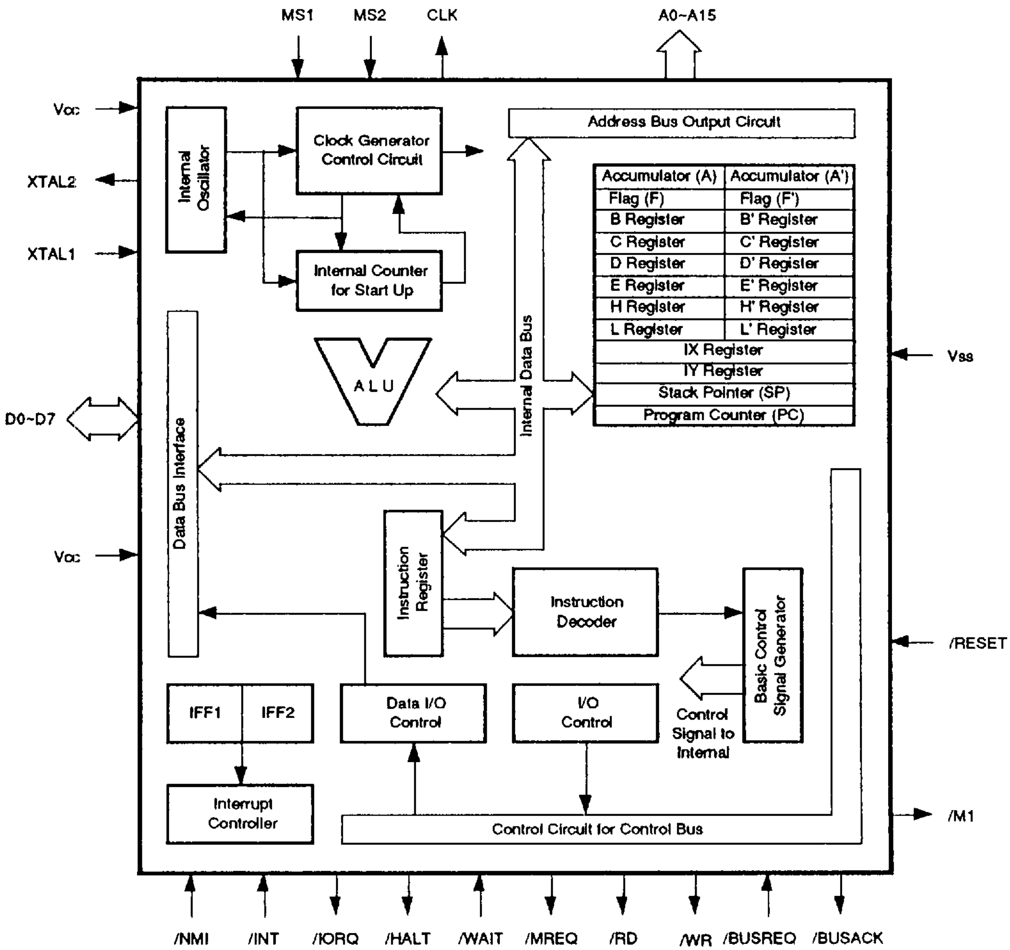

Figure 2. Block Diagram

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System Configuration. The Z84C01 has a built-in system clock generator for CMOS Z80 in addition to the standard functions of the Z84C00 MPU. The explanation is provided here with emphasis placed on the halt function relative to the clock generator, which is an additional function. The internal register group, reset and interrupt function are identical to those of the Z84C00. For details, please refer to the data sheet for the Z84C00.

In this section, the following principal components and functions will be described:

(1) Generation of clock
(2) Operation mode
(3) Start-up time at time of restart

Generating the System Clock. The Z84C01 has a built-in oscillation circuit and required clock can be easily generated by connecting an oscillator to the external terminals (XTAL1, XTAL2). Clock in the same frequency as input oscillation frequency is generated.
Examples of oscillator connection are shown in Figures 3a, 3b.

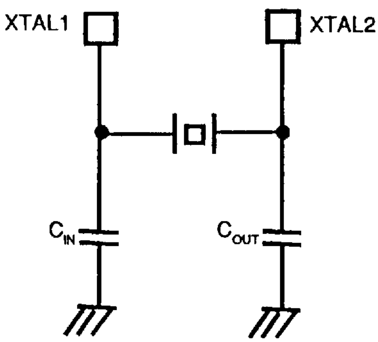

Figure 3a Example of Oscillator Connection and Constant

C_{IN}	C_{OUT}
22_{PF}	33_{PF}

Figure 3b Example of Oscillator Connection and Constant

Operation Modes. There are four kinds of operation modes available for the Z84C01 in connection with generation of clock; RUN Mode, IDLE1/2 Modes and STOP Mode. One of these modes is selected by the mode select inputs (MS1, MS2).

The operation mode is effective when the halt instruction is executed. Restart of MPU from the stopped state under IDLE1/2 Mode or STOP Mode is effected by inputting either RESET signal or interrupt signal (INT or NMI).

Operations of these modes in the halt state are shown in Table 2.

Table 2 Clock Generating Operation Mode

Operation Mode	MS1	MS2	Description at HALT State
RUN Mode	1	1	MPU continues the operation and supplies clock to the outside continuously.
IDLE 1 Mode	0	0	The internal oscillator's operation is continued. Clock (CLK) output as well as internal operations are stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.
IDLE 2 Mode	0	1	The internal oscillator's operation and clock (CLK) output are continued but the internal operations are stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.
STOP Mode	1	0	All operations of the internal oscillator, clock (CLK) output, and internal operation are stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.

Start-up Time at Time of Restart (STOP Mode). When MPU is released from the halt state by accepting an interrupt request, MPU, then will execute an interrupt service routine. Therefore, when an interrupt request is accepted, MPU starts generation of internal system clock and clock output after a start-up time by the internal counter (2^{14}+2.5) TcC (TcC: Clock Cycle) to obtain a stabilized oscillation for MPU operation.

Further, in case of the restart by $\overline{\text{RESET}}$ signal, the internal counter does not operate for a quick operation at time of power ON.

Status Change Flowchart and Basic Timing. In this section, the status change and basic timing when the Z84C01 is operating are explained.

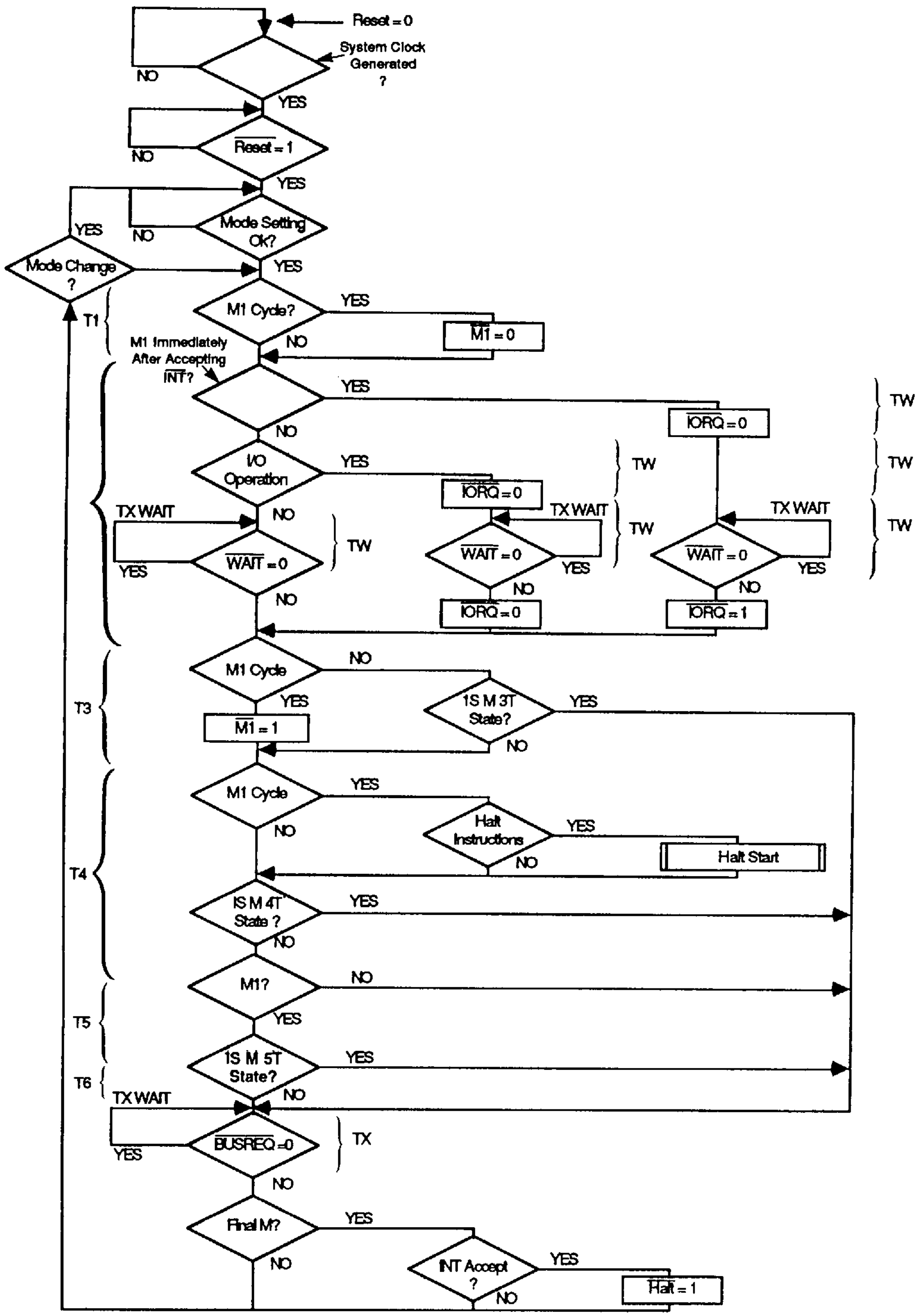

Figure 4 (a) Status Change Flowchart

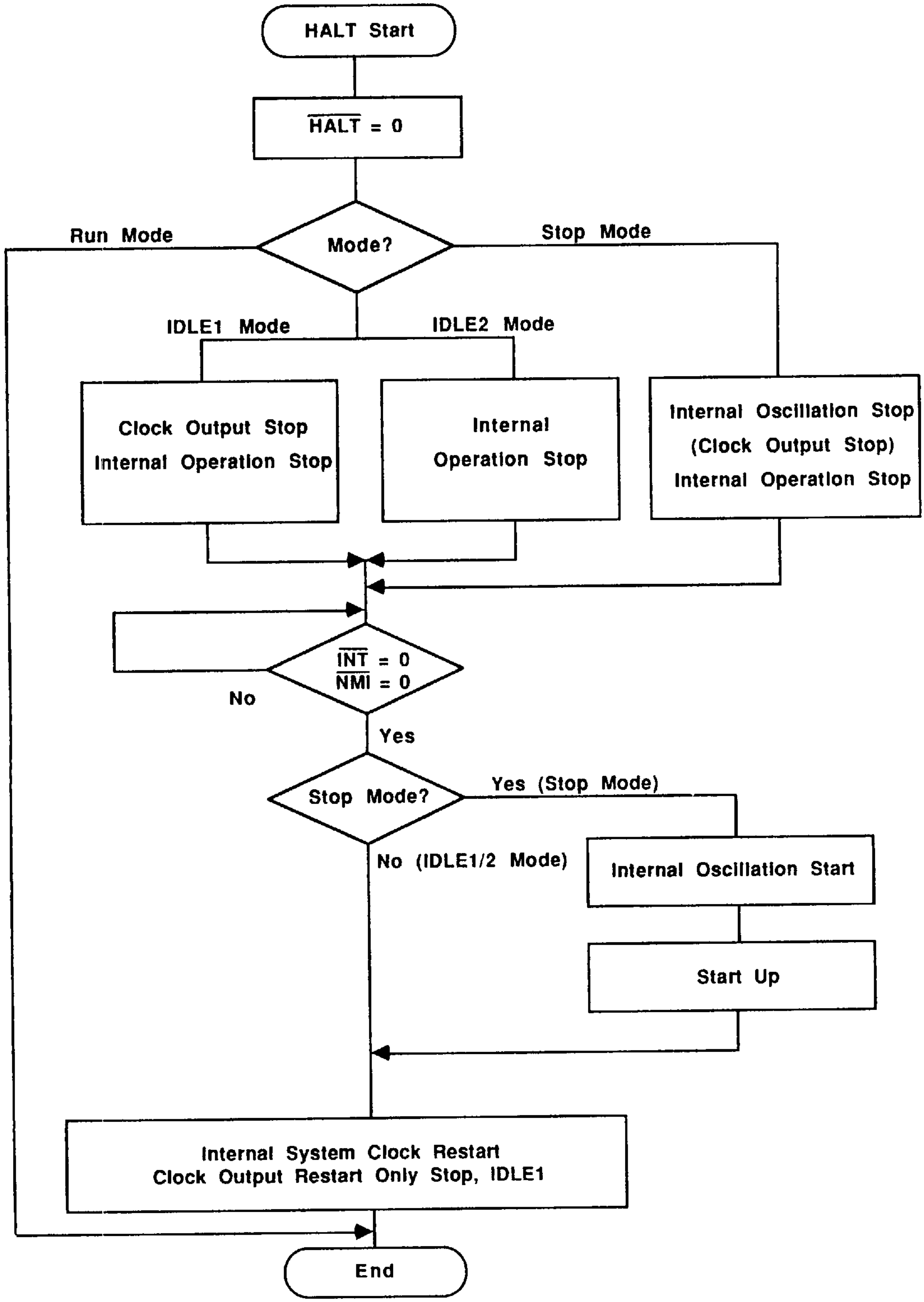

Figure 4 (b) Status Change Flowchart

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Basic Timing. The basic timing is explained here with emphasis placed on the halt function relative to the clock generator. Except $\overline{RFSH}$ signal output, the following items are identical to those for the Z84C00. Refer to the data sheet for the Z84C00.

- Operation code fetch cycle
- Memory read/write operation
- Input/output operation
- Bus request/acknowledge operation
- Maskable interrupt request operation
- Non-maskable interrupt request operation
- Reset operation

Note that the Z84C01 does not have the refresh terminal ($\overline{RFSH}$), but refresh address is output on the address bus in the operation code fetch cycle (M1) as in the Z84C00 since the on-chip refresh control circuit is available.

(1) Operation When HALT Instruction is Executed
When MPU fetches a halt instruction in the operation code fetch cycle, HALT signal goes active (low level) in synchronous with falling edge of T4 state for the peripheral LSI and MPU stops the operation. The system clock generating operation after this differs depending upon the operation mode (RUN Mode, IDLE1/2 Mode or STOP Mode). If the internal system clock is running, MPU continues to execute NOP instruction even in the halt state.

(a) RUN Mode (MS1=1, MS2=1)
Shown in Fig. 5 is the basic timing when the halt instruction is executed in RUN Mode.

In RUN Mode, system clock (ø) in MPU and clock output (CLK) are not stopped, even after the halt instruction is executed. Therefore, until the halt state is released by the interrupt signal ($\overline{NMI}$ or $\overline{INT}$) or $\overline{RESET}$ signal, MPU continues to execute NOP instruction.

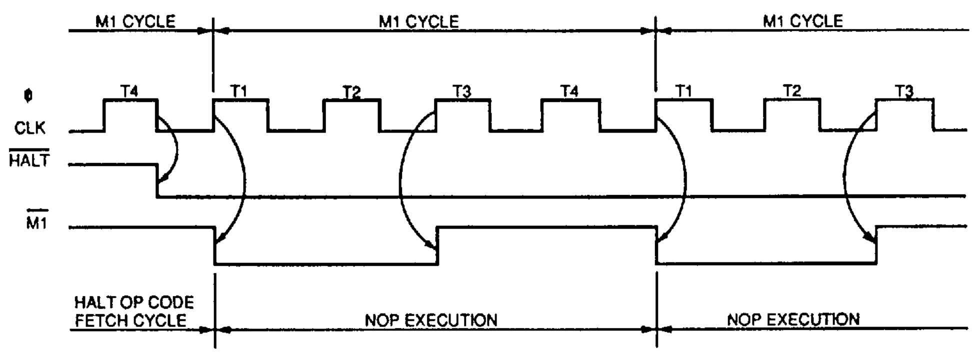

Figure 5 Timing of RUN Mode (at Halt Command Execution)

(b) IDLE1 Mode (MS1=0, MS2=0)
Shown in Fig. 6 is the basic timing when the halt instruction is executed in IDLE1 Mode.

In IDLE1 Mode, system clock (ø) in MPU and clock output (CLK) are stopped and MPU stops its operation after the halt instruction is executed. However, the internal oscillator continues to operate.

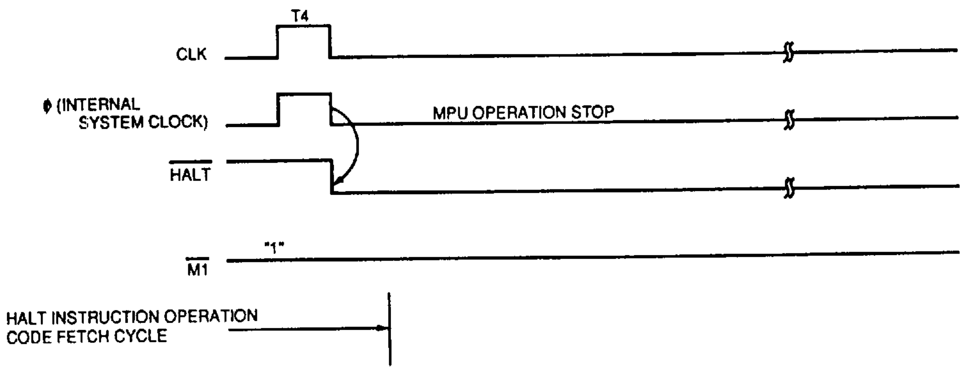

Figure 6 IDLE1 Mode Timing (at Halt Instruction Execution)

(c) IDLE2 Mode (MS1=0, MS2=1)
Shown in Fig. 7 is the basic timing when the halt instruction is executed in IDLE2 Mode.

In IDLE2 Mode, system clock (ø) in MPU is stopped and MPU stops its operation after the halt instruction is executed. However, the internal oscillator and clock output (CLK) to the outside of MPU continues to operate.

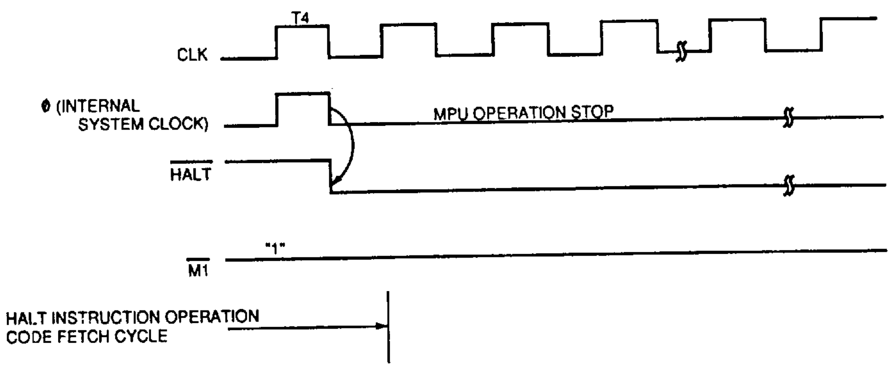

Figure 7 IDLE2 Mode Timing (at Halt Instruction Execution)

(d) **STOP Mode (MS1=1, MS2=0)**
Shown in Fig. 8 is the basic timing when the halt instruction is executed in STOP Mode.

In STOP Mode, internal operation and internal oscillator are stopped after the halt instruction is executed. Therefore, system clock (ϕ) in MPU and clock output (CLK) to the outside of MPU are stopped.

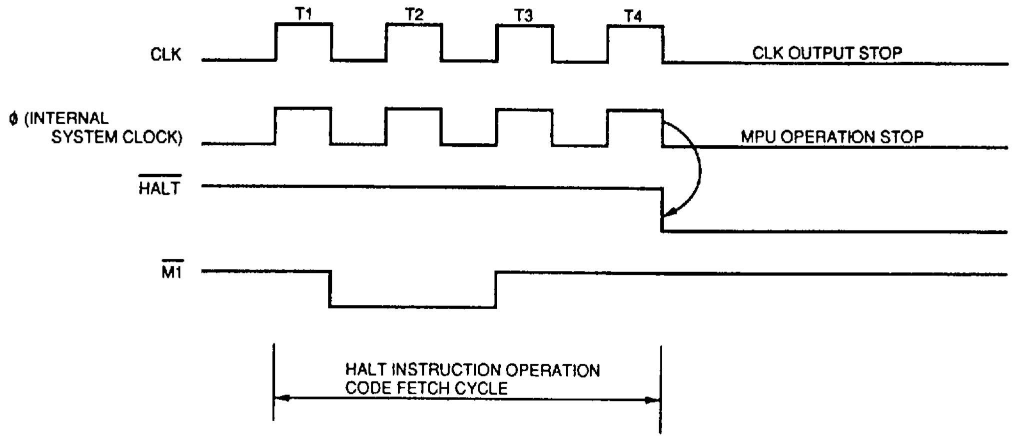

Figure 8 STOP Mode Timing (at Halt Instruction Execution)

(2) **Release from Halt State**
The halt state of MPU is released when "0" is input to RESET signal and MPU is reset or an interrupt request is accepted. An interrupt request signal is sampled at the leading edge of the last clock cycle (T4 state) of NOP instruction. In case of the maskable interrupt, interrupt will be accepted by an active INT signal ("0" level). Also the interrupt enable flip-flop must have been set to "1". The accepted interrupt process is started from next cycle.

Further, when the internal system clock is stopped (IDLE1/2 Mode, STOP Mode), it is necessary first to restart the internal system clock. The internal system clock is restarted when RESET or interrupt signal (NMI or INT) is input.

(a) **RUN Mode (MS1, MS2=1)**
The halt release operation by acceptance of interrupt request in RUN Mode is shown in Fig. 9.

In RUN Mode the internal system clock is not stopped, and therefore, if the interrupt signal is recognized at the rise of T4 state of the continued NOP instruction, MPU will execute the interrupt process from next cycle.

The halt release operation by resetting MPU in RUN Mode is shown in Fig. 10. After reset, MPU will execute an instruction starting from address 0000H. However, in order to reset MPU it is necessary to keep RESET signal at "0" for at least 3 clocks. In addition, if RESET signal becomes "1", after the dummy cycle for at least two T states, MPU executes an instruction from address 0000H.

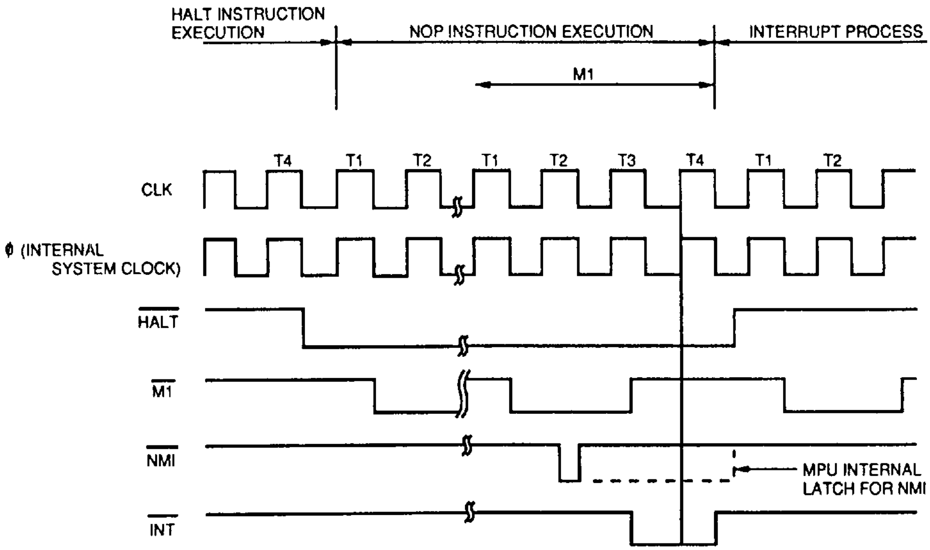

Figure 9 Halt Release Operation Timing by interrupt Request Signal in RUN Mode

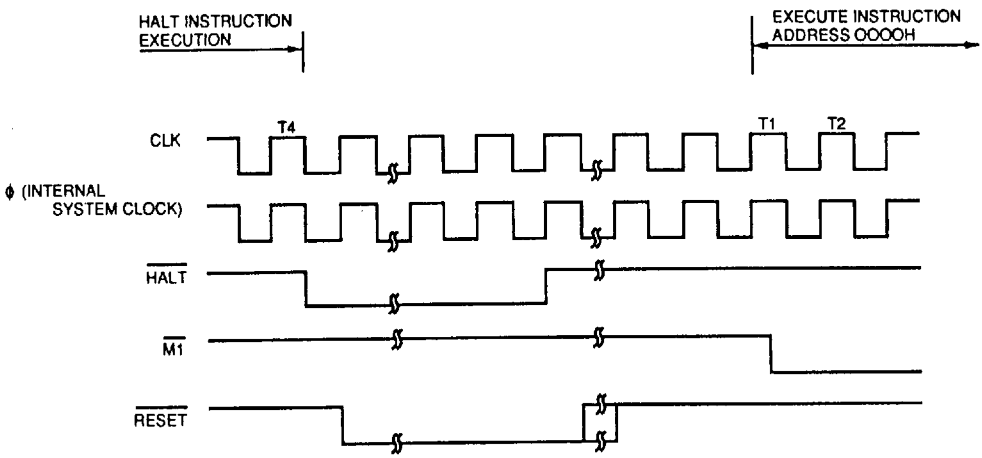

Figure 10 Halt Release Operation Timing by Reset in RUN Mode

(b) IDLE1 Mode (MS1=0, MS2=0), IDLE2 Mode (MS1=0, MS2=1)

The halt release operation by interrupt signal in IDLE1 Mode is shown in Fig. 11 (a) and in IDLE2 Mode in Fig. 11 (b).

When receiving $\overline{NMI}$ or $\overline{INT}$ signal, MPU starts the internal system clock operation. In IDLE1 Mode, MPU starts clock output to the outside at the same time.

The operation stop of MPU in IDLE1/2 Mode is taking place at "0" level during T4 state in the halt instruction operation code fetch cycle. Therefore, after being restarted by the interruption signal, MPU executes one NOP instruction and samples an interrupt signal at the rise of T4 state during the execution of this NOP instruction, and executes the interrupt process from next cycle.

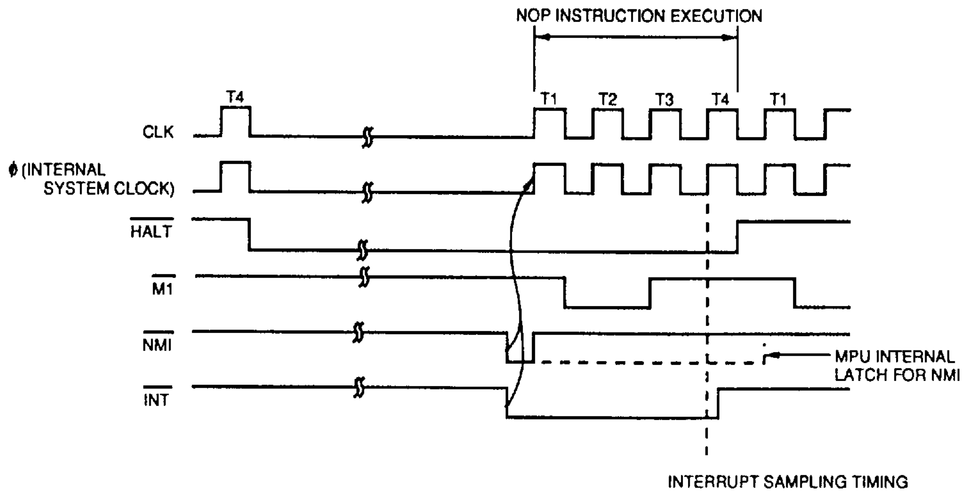

Figure 11 (a) IDLE1 Mode

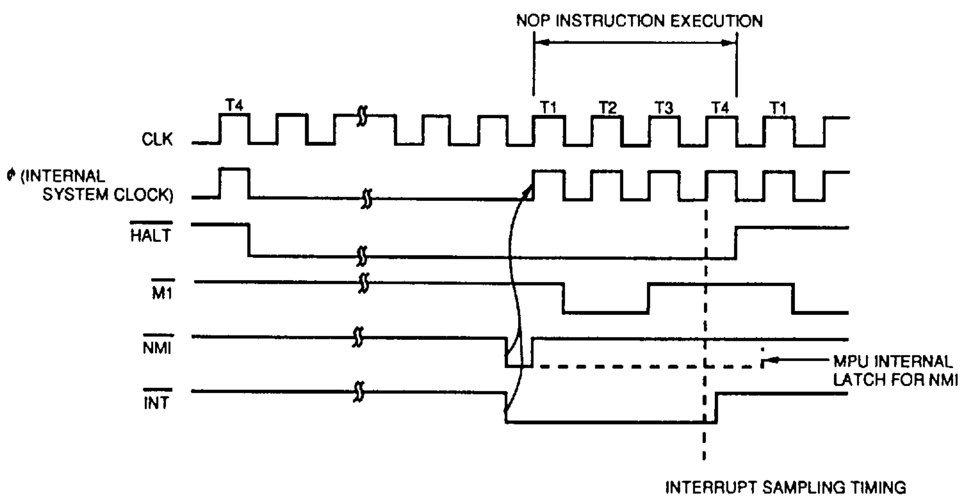

Figure 11 (b) IDLE2 Mode

Figure 11 Halt Release Operation Timing by Interrupt Request Signal in IDLE1/2 Mode

If no interrupt signal is accepted during the execution of the first NOP instruction after the internal system clock is restarted, MPU is not released from the halt state and is placed in IDLE1/2 Mode again at "0" level during T4 state of the NOP instruction, stopping the internal system clock. If $\overline{INT}$ signal is not at "0" level at the rise of T4 state, no interrupt request is accepted.

The halt release operation by resetting MPU in IDLE1 Mode is shown in Fig. 12 (a) and that in IDLE2 Mode in Fig. 12 (b).

When $\overline{RESET}$ signal at "0" level is input into MPU, the internal system clock is restarted and MPU will execute an instruction stored in address 0000H.

At time of $\overline{RESET}$ signal input, it is necessary to take the same care as that in resetting MPU in RUN Mode.

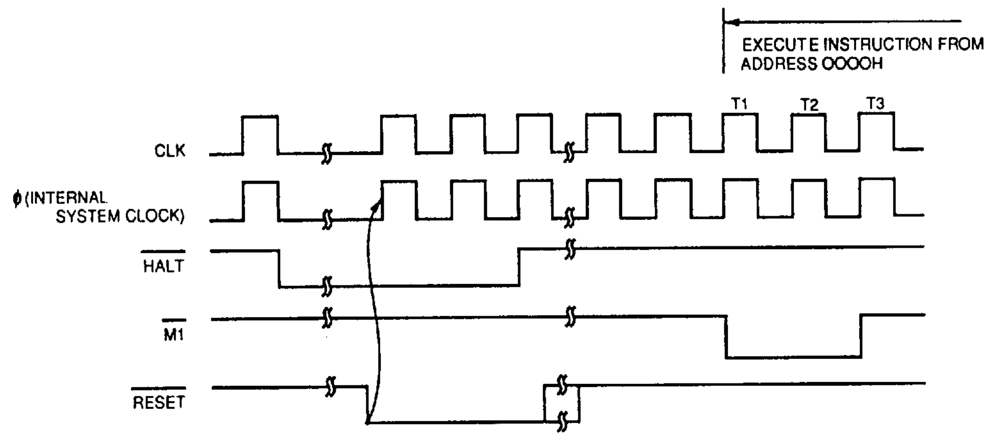

Figure 12 (a) IDLE1 Mode

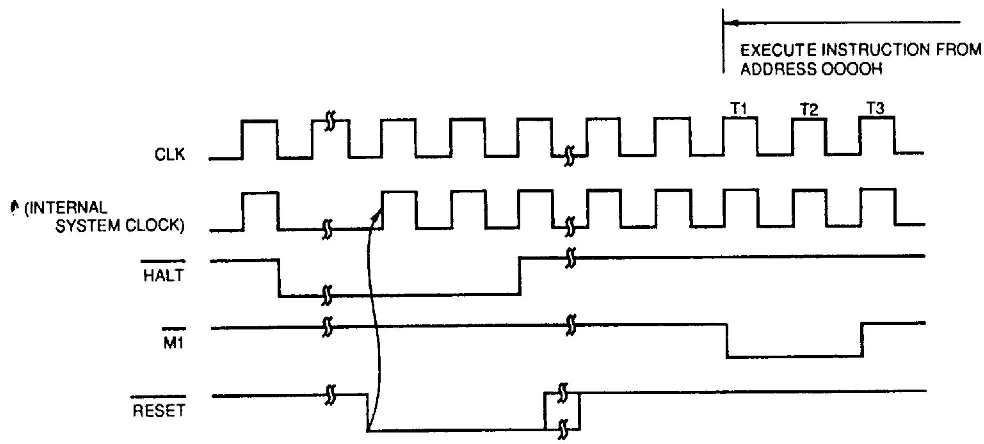

Figure 12 (b) IDLE2 Mode

Figure 12 Halt Release Operation Timing by Reset in IDLE1/2 Mode

(c) STOP Mode (MS1=1, MS2=0)

The halt release operation by interrupt signal in STOP Mode is shown in Fig. 13.

When MPU received an interrupt signal, the internal oscillator is restarted. In order to obtain stabilized oscillation, the internal system clock and clock output to the outside are started after a start-up time of (2^{14}+2.5) TcC (TcC: Clock Cycle) by the internal counter.

MPU executes one NOP instruction after the internal system clock is restarted and at the same time, sampling an interrupt signal at the rise of T4 state during the execution of this NOP instruction. If the interrupt signal is accepted, MPU executes the interrupt process operation from next cycle.

At time of interrupt signal input, it is necessary to take the same care as that in the interrupt signal input in IDLE1/2 Mode. The halt release operation by MPU resetting in STOP Mode is shown in Fig. 14.

When $\overline{RESET}$ signal at "0" level is input into MPU, the internal oscillator is restarted. However, since it performs a quick operation at time of power ON, the internal counter does not operate. Therefore, the operation may not be carried out properly due to unstable clock immediately after the signal in STOP Mode, it is necessary to hold $\overline{RESET}$ signal at "0" level for sufficient time. When $\overline{RESET}$ signal becomes "1", after the dummy cycle for at least 2T states, MPU starts to execute an execution from address 0000H.

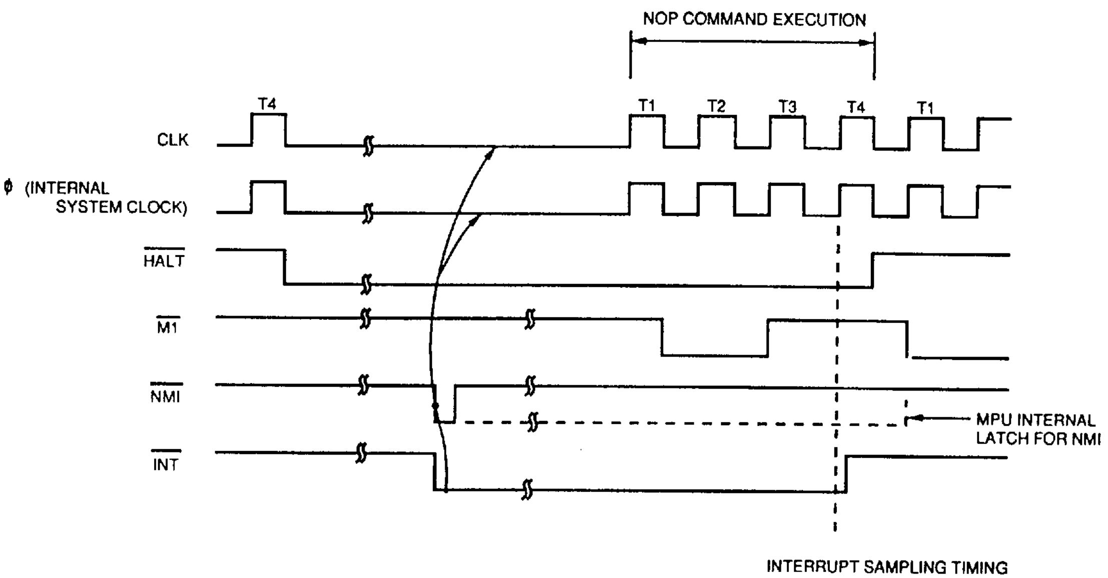

Figure 13 Halt Release Operation Timing by Interrupt Request Signal in STOP Mode

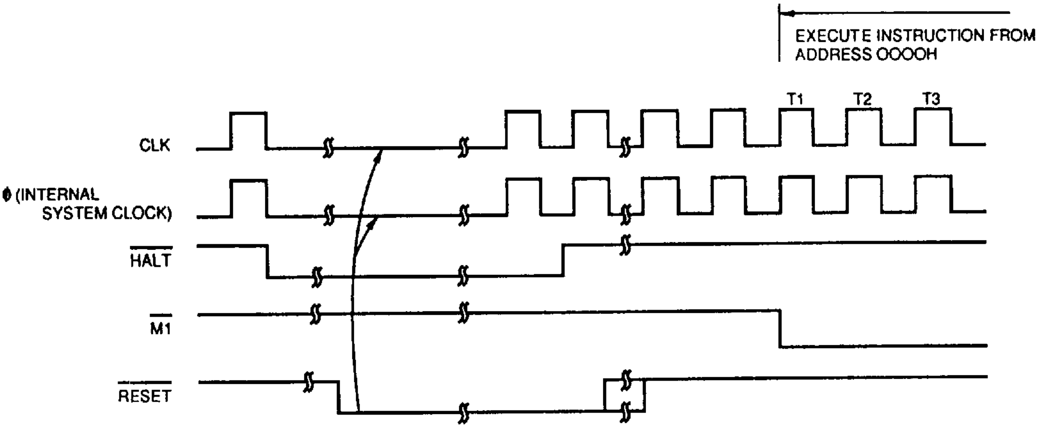

Figure 14 Halt Release Operation Timing by Reset in STOP Mode

Instruction Set. Instruction set of the Z84C01 is the same as that for the Z84C00. For details refer to the data sheet for the Z84C00.

Method of Use. An example of the Z84C01 with the Z80 family peripheral LSI's is shown in Fig. 15.

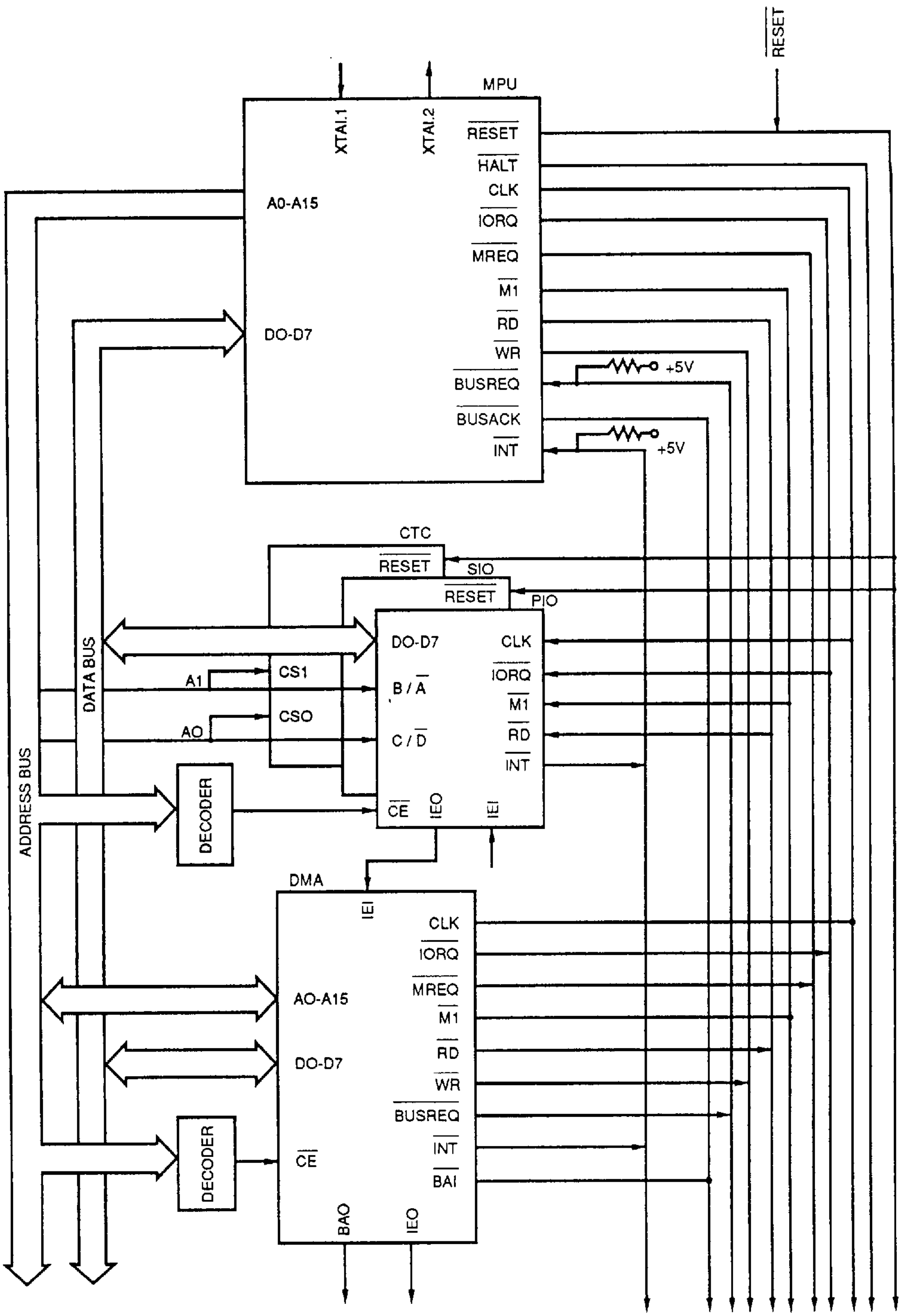

Figure 15 Example of Z80 Family Peripheral LSI

CPU TIMING

Timing Diagrams. The Z84C01 CPU executes instructions by proceeding through a specific sequence of operations:

- Memory read or write
- I/O device read or write
- Interrupt acknowledge

The basic clock period is referred to as a Time or Cycle, and three or more T cycles make up a machine cycle (M1, M2 or M3 for instance). Machine cycles can be extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.

Instruction Opcode Fetch. The CPU places the contents of the Program Counter (PC) on the address bus as the start of the cycle (Figure 16). Approximately one-half clock cycle later, $\overline{MREQ}$ goes active. When active, $\overline{RD}$ indicates that the memory data can be enabled onto the CPU data bus.

The CPU samples the $\overline{WAIT}$ input with the falling edge of clock state T2. During clock states T3 and T4 of an $\overline{M1}$ cycle, dynamic RAM refresh can occur while the CPU starts decoding and executing the instruction.

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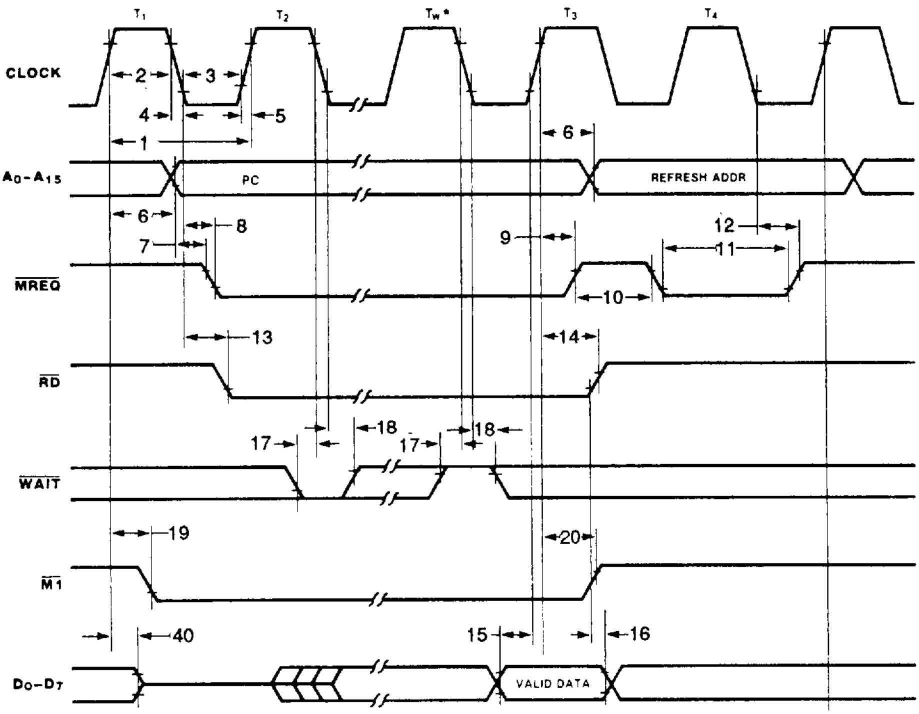


Figure 16 Instruction Opcode Fetch

Memory Read or Write Cycles. Figure 17 shows the timing of memory read or write cycles other than an opcode fetch ($\overline{M1}$) cycle. The $\overline{MREQ}$ and $\overline{RD}$ signals function exactly as in the fetch cycle.

In a memory write cycle, $\overline{MREQ}$ also becomes active when the address bus is stable. The $\overline{WR}$ line is active when the data bus is stable, so that it can be used directly as an R/$\overline{W}$ pulse to most semiconductor memories.

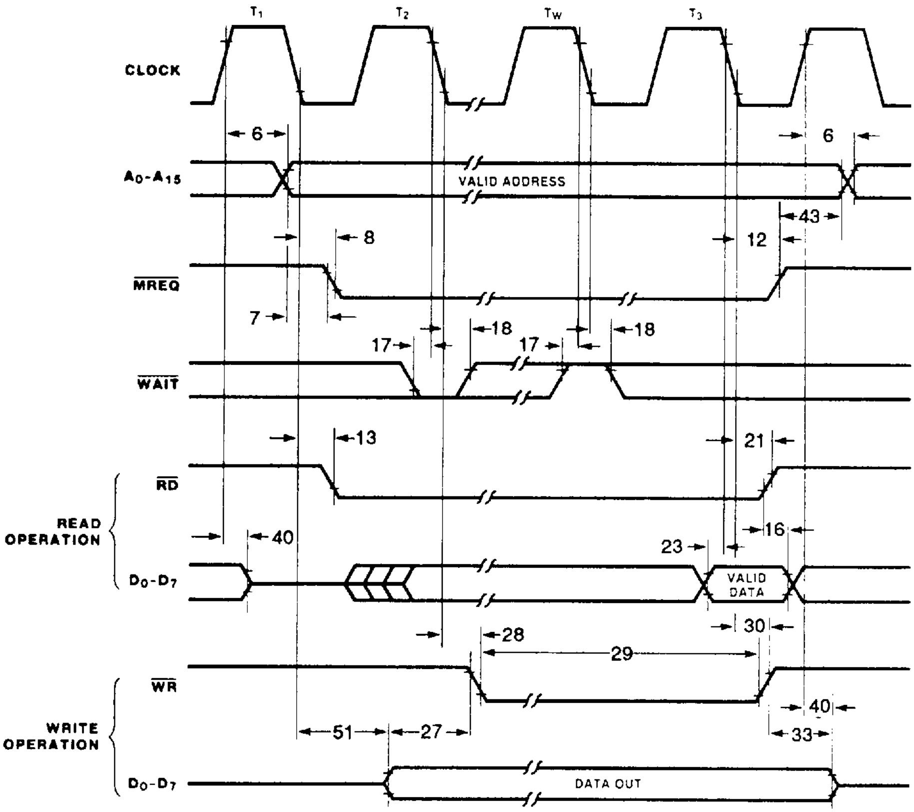
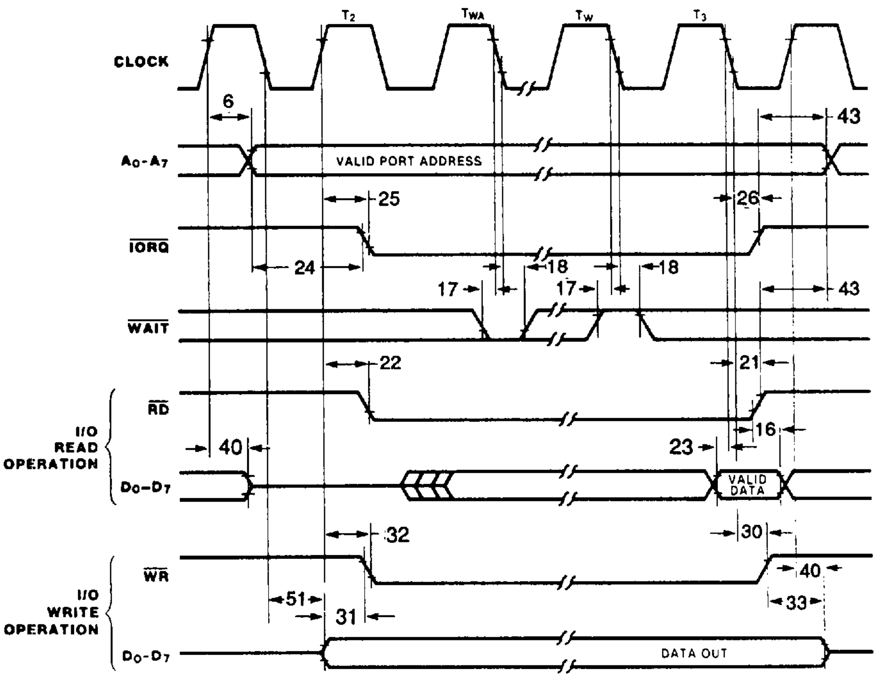


Figure 17 Memory Read or Write Cycles

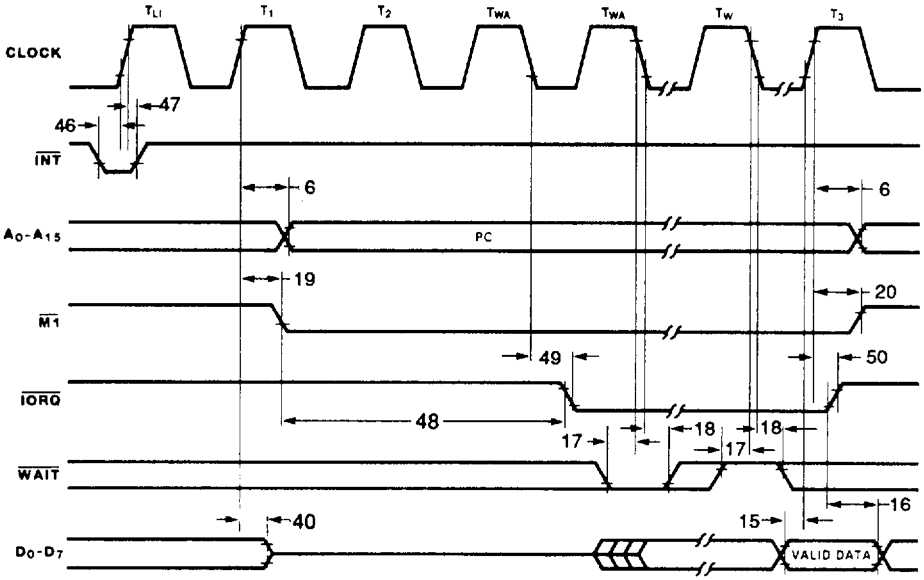
Input or Output Cycles. Fig. 18 shows the timing for an I/O read or I/O write operation. During I/O operations, the CPU automatically inserts a single Wait state (T_{WA}). This extra Wait state allows sufficient time for an I/O port to decode the address from the port address lines.



TWA = One wait cycle automatically inserted by CPU.

Figure 18 Input or Output Cycles

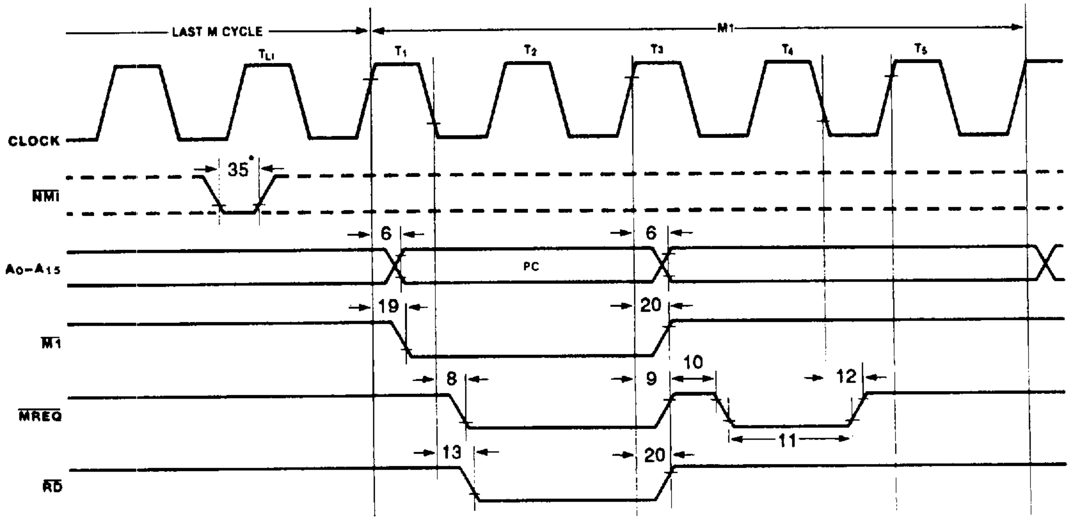
Interrupt Request/Acknowledge Cycle. The CPU samples the interrupt signal with the rising edge of the last clock cycle at the end of any instruction (Fig. 19). When an interrupt is accepted, a special $\overline{M1}$ cycle is generated. During this $\overline{M1}$ cycle, $\overline{IORQ}$ becomes active (instead of $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. The CPU automatically adds two Wait states to this cycle.



NOTES: 1) T_{LI} = Last state of any Instruction cycle.
2) T_{WA} = Wait cycle automatically Inserted by CPU.

Figure 19 Interrupt Request/Acknowledge Cycle

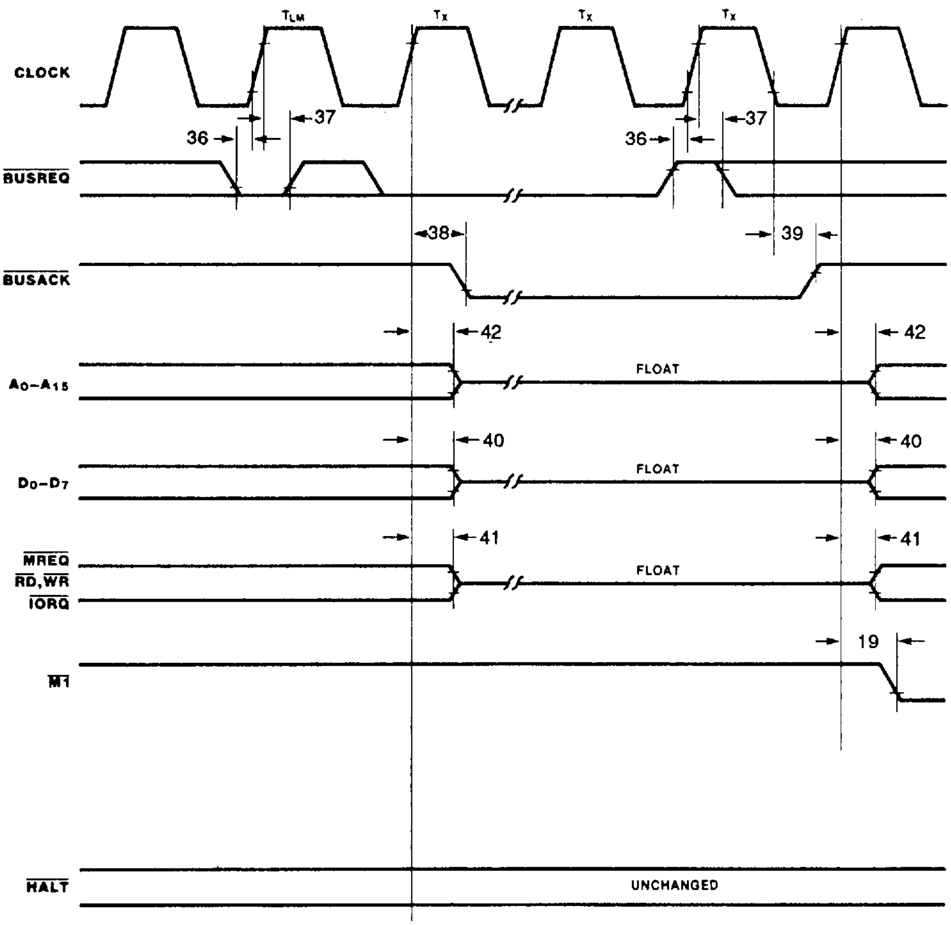
Non-Maskable Interrupt Request Cycle. $\overline{NMI}$ is sampled at the same time as the maskable interrupt input $\overline{INT}$, but has higher priority and cannot be disabled under software control. The subsequent timing is similar to that of a normal memory read operation except that data put on the bus by the memory is ignored. The CPU instead executes a restart (RST) operation and jumps to the $\overline{NMI}$ service routine located at address 0066H (Fig. 20).



*Although $\overline{NMI}$ is an asynchronous input, to guarantee its being recognized on the following machine cycle, $\overline{NMI}$'s falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle (T_{LI}).

Figure 20 Non-Maskable Interrupt Request Operation

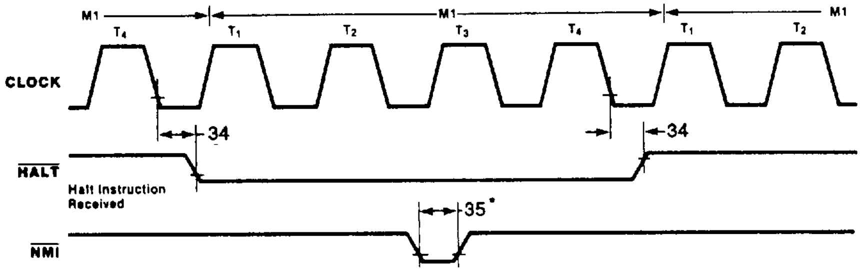
Bus Request/Acknowledge Cycle. The CPU samples $\overline{BUSREQ}$ with the rising edge of the last clock period of any machine cycle (Fig. 21). If $\overline{BUSREQ}$ is active, the CPU sets its address, data, and $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ lines to a high-impedance state with the rising edge of the next clock pulse. At that time, any external device can take control of these lines, usually to transfer data between memory and I/O devices.



NOTES: 1) T_{LM} = Last state of any M cycle.
2) T_X = An arbitrary clock cycle used by requesting device.

Figure 21 BUS Request/Acknowledge Cycle

Halt Acknowledge Cycle.



*Although NMI is an asynchronous input, to guarantee its being recognized on the following machine cycle, NMI's falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle (T_{LI}).

Figure 22 Halt Acknowledge

Reset Cycle. RESET must be active for at least three clock cycles for the CPU to properly accept it. As long as RESET remains active, the address and data buses float, and the control outputs are inactive.

Once RESET goes inactive, two internal T cycles are consumed before the CPU resumes normal processing operation. RESET clears the PC register, so the first opcode fetch will be location 0000H (Fig. 23).

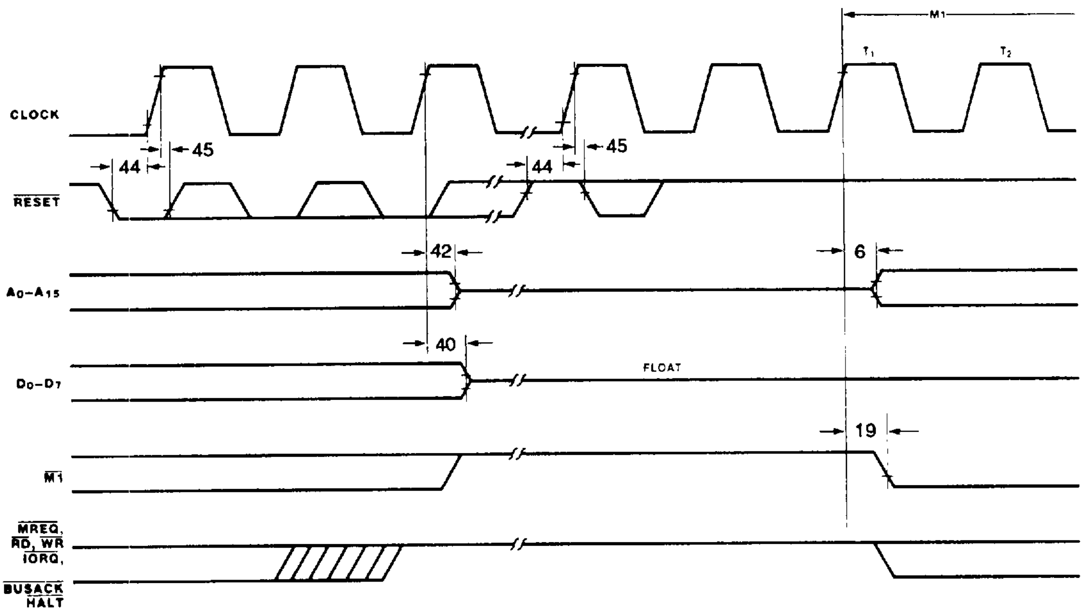


Figure 23 Reset Cycle

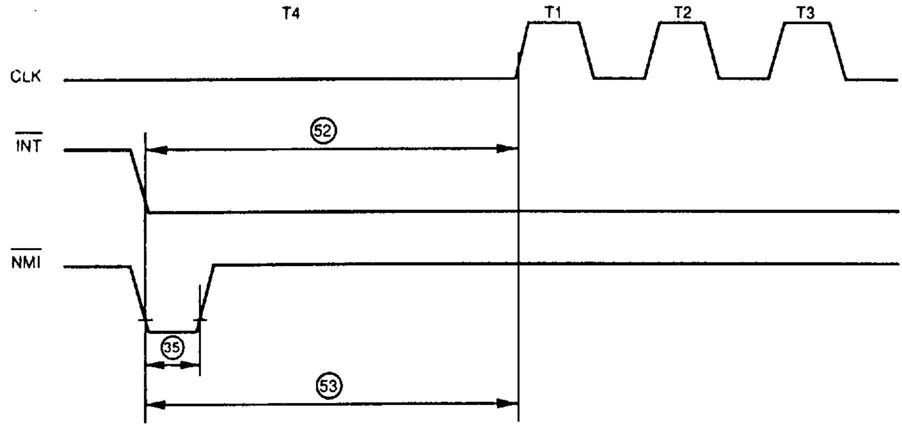


Figure 24 Clock Restart Timing (STOP Mode)

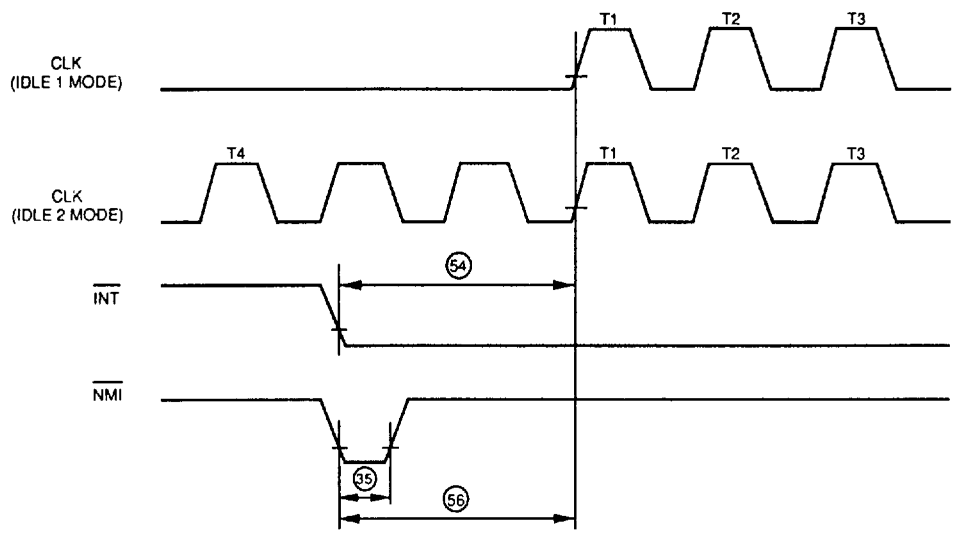


Figure 25 Clock Restart Timing (IDLE1/2 Mode)

PRECAUTIONS:

(1) To reset MPU, it is necessary to hold $\overline{RESET}$ signal input at "0" level for at least three clocks.

In particular, to release the HALT state by $\overline{RESET}$ signal in STOP Mode, hold $\overline{RESET}$ signal at "0" level for sufficient time in order to stabilize output from the internal oscillator.

(2) In releasing MPU from the HALT state by inter rupt signal in IDLE1/2 Mode and STOP Mode, MPU will not be released from the HALT state and the internal system clock will stop again unless an interrupt signal is accepted during the execution of NOP instruction even when the internal system clock is restarted by the interrupt signal input. In particular, care must be taken when $\overline{INT}$ is used.

Other precautions are identical to those for the Z84C00, except those for $\overline{RFSH}$ terminal. Refer to the data sheet for the Z84C00.

AC CHARACTERISTICS:

No	Symbol	Parameter	Z84C0106 Min	Z84C0106 Max	Z84C0110 Min	Z84C0110 Max	Unit	Note
1	TcC	Clock Cycle Time	162*	DC	100*	DC	nS	
2	TwCh	Clock Pulse Width (High)	65	DC	40	DC	nS	
3	TwCl	Clock Pulse Width (Low)	65	DC	40	DC	nS	
4	TfC	Clock Fall Time		20		10	nS	
5	TrC	Clock Rise Time		20		10	nS	
6	TdCr(A)	Address Valid from Clock Rise		90		60	nS	
7	TdA(MREQf)	Address valid to /MREQ Fall	35*		5*		nS	
8	TdCf(MREQf)	Clock Fall to /MREQ Fall Delay		70		40	nS	
9	TdCr(MREQr)	Clock Rise to /MREQ Rise Delay		70		40	nS	
10	TwMREQh	/MREQ Pulse Width (High)	60*		25*		nS	[1]
11	TwMREQl	/MREQ Pulse Width (Low)	132*		70*		nS	[1]
12	TdCf(MERQr)	Clock Fall to /MREQ Rise Delay		70		40	nS	
13	TdCf(RDf)	Clock Fall to /RD Fall Delay		80		40	nS	
14	TdCr(RDr)	Clock Rise to /RD Rise Delay		70		40	nS	
15	TsD(Cr)	Data Setup Time to Clock Rise	30		25		nS	
16	ThD(RDr)	Data Hold Time after /RD Rise	0		0		nS	
17	TsWAIT(Cf)	/WAIT Setup Time to Clock Fall	60		30		nS	
18	ThWAIT(Cf)	/WAIT Hold Time after Clock Fall	10		0		nS	
19	TdCr(M1f)	Clock Rise to /M1 Fall Delay		80		40	nS	
20	TdCr(M1r)	Clock Rise to /M1 Rise Delay		80		40	nS	
21	TdCf(RDr)	Clock Fall to /RD Rise Delay		70		40	nS	
22	TdCr(RDf)	Clock Rise to /RD Fall Delay		70		40	nS	
23	TsD(Cf)	Data Setup to Clock Fall During M2, M3, M4 or M5 Cycles	40		25		nS	
24	TdA(IORQf)	Address Stable Prior to /IORQ Fall	107*		50*		nS	
25	TdCr(IORQf)	Clock Rise to /IORQ Fall Delay		65		40	nS	
26	TdCf(IORQr)	Clock Fall to /IORQ Rise Delay		70		40	nS	
27	TdD(WRf)Mw	Data Stable Prior to /WR Fall	22*		0*		nS	
28	TdCf(WRf)	Clock Fall to /WR Fall Delay		70		40	nS	
29	TwWR	/WR Pulse Width	132*		75*		nS	
30	TdCf(WRr)	Clock Fall to /WR Rise Delay		70		40	nS	
31	TdD(WRf)IO	Data Stable Prior to /WR Fall	-55*		-50*		nS	
32	TdCr(WRf)	Clock Rise to /WR Fall Delay		60		40	nS	
33	TdWRr(D)	Data Stable from /WR Fall	30*		0*		nS	
34	TdCf(HALT)	Clock Fall to /HALT 'L' or 'H'		260		100	nS	
35	TwNMI	/NMI Pulse Width	70		60		nS	
36	TsBUSREQ(Cr)	/BUSREQ Setup Time to Clock Rise	50		35		nS	
37	ThBUSREQ(Cr)	/BUSREQ Hold Time After Clock Rise	10		0		nS	
38	TdCr(BUSACKf)	Clock Rise to /BASACK Fall Delay		90		40	nS	
39	TdCf(BUSACKr)	Clock Fall to /BASACK Rise Delay		90		40	nS	

Z84C01 AC CHARACTERISTICS (Continued)

No	Symbol	Parameter	Z84C0106 Min	Z84C0106 Max	Z84C0110 Min	Z84C0110 Max	Unit	Note
40	TdCr(Dz)	Clock Rise to Data Float Delay		80		40	nS	
41	TdCr(CTz)	Clock Rise to Control Outputs Float Delay (/MREQ, /IORQ, /RD and /WR)		70		40	nS	
42	TdCr(Az)	Clock Rise to Address Float Delay		80		50	nS	
43	TdCTr(A)	Address Hold Time From /MREQ, /IORQ, /RD or /WR	35*		5*		nS	
44	TsRESET(Cr)	/RESET to Clock Rise Setup Time	60		30		nS	
45	ThRESET(Cr)	/RESET to Clock Rise Hold Time	10		0		nS	
46	TsINTf(Cr)	/INT Fall to Clock Rise Setup Time	70		50		nS	
47	ThINTr(Cr)	/INT Rise to Clock Rise Hold Time	10		0		nS	
48	TdM1f(IORQf)	/M1 Fall to /IORQ Fall Delay	359*		205*		nS	
49	TdCf(IORQf)	/Clock Fall to /IORQ Fall Delay		70		40	nS	
50	TdCf(IORQr)	Clock Rise to /IORQ Rise Delay		70		40	nS	
51	TdCf(D)	Clock Fall to Data Valid Delay		150		80	nS	
52	TRST1S	CLK Restart Time by /INT (STOP Mode)	(typ) $(2^{14}+2.5)$TcC		(typ) $(2^{14}+2.5)$TcC			
53	TRST2S	CLK Restart Time by /NMI (STOP Mode)	(typ) $(2^{14}+2.5)$TcC		(typ) $(2^{14}+2.5)$TcC			
54	TRST1I	CLK Restart Time by /INT (IDLE1/2 Mode)	(typ)2.5TcC		(typ)2.5TcC			
55	TRST2I	CLK Restart Time by /NMI (IDLE1/2 Mode)	(typ)2.5TcC		(typ)2.5TcC			

Notes:

* For clock periods other than minimum shown, calculate parameters using following 'Note'. Calculated values above assumed TrC = TfC = maximum.

[1] Increasing delay by 10nS for each 50pF increase in loading, 200pF max for data lines, and 100pF for control lines.

Z84C01 AC CHARACTERISTICS

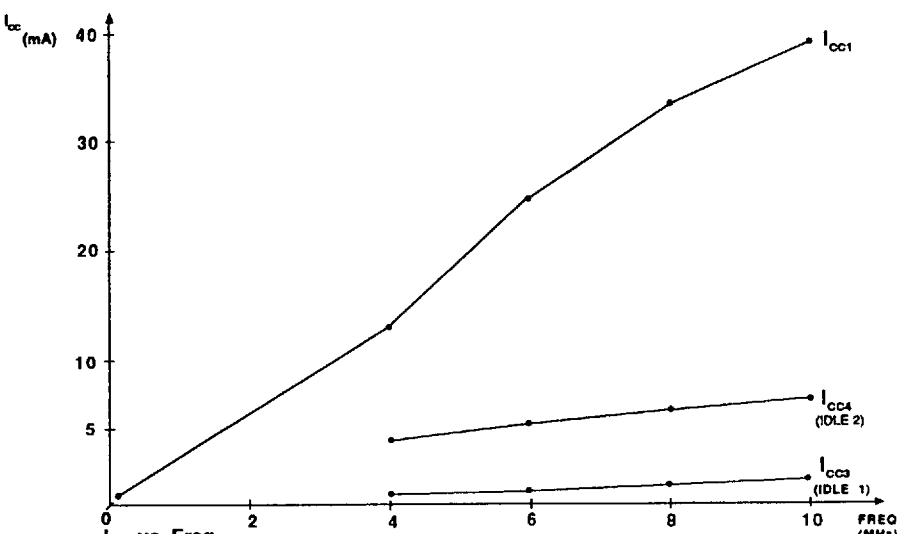
Footnotes

No	Symbol	Parameter	Z84C0106	Z84C0110
1	TcC	TwCh + TwCl + TrC + TfC		
7	TdA(MREQf)	TwCh + TfC	-50	-45
10	TwMREQh	TwCh + TfC	-25	-25
11	TwMREQl	TcC	-30	-30
24	TdA(IORQf)	TcC	-55	-50
27	TdD(WRf)	TcC	-140	-100
29	TwWR	TcC	-30	-25
31	TdD(WRf)	TwCl + TrC	-140	-100
33	TdWRr(D)	TwCl + TrC	-55	-50
43	TdCTr(A)	TwCl + TrC	-50	-45
48	TdM1f(IORQf)	2TcC + TwCh + TfC	-50	-45

DC CHARACTERISTICS VCC = 5.0 V +-10%

Symbol	Parameter	Min	Max	Unit	Condition	Note
V_{OLC}	Clock Output High Voltage	V_{CC}-0.6		V	-2.0mA	
V_{OHC}	Clock Output Low Voltage		0.4	V	+2.0mA	
V_{IH}	Input Low Voltage	-0.3	0.8	V		
V_{IL}	Input High Voltage	2.2	V_{CC}	V		
V_{OL}	Output Low Voltage		0.4	V	I_{LO}=2.0mA	[5]
V_{OH1}	Output High Voltage	2.4		V	I_{OH}=-1.6mA	[4]
V_{OH2}	Output High Voltage	V_{CC}-0.8		V	I_{OH}=-250μA	[5]
I_{CC1}	Power Supply Current - 10MHz		50	mA	V_{CC}=5V	[1]
	- 6MHz		30	mA	V_{IH}=V_{CC}-0.2V	
					V_{IL}=0.2V	
I_{CC2}	Power Supply Current (STOP Mode)		10	μA	V_{CC}=5V	
I_{CC3}	Power Supply Current (IDLE1 Mode)				V_{CC}=5V	
	- 10MHz		4	mA	V_{IH}=V_{CC}-0.2V	
	- 6MHz		4	mA	V_{IL}=0.2V	
I_{CC4}	Power Supply Current (IDLE2 Mode)				V_{CC}=5V	
	- 10MHz		15	mA	V_{IH}=V_{CC}-0.2V	[1]
	- 6MHz		13	mA	V_{IL}=0.2V	[1]
I_{LI}	Input Leakage Current	-10	10	μA	V_{IN}=0.4V to V_{CC}	[4]
I_{LO}	3-state Output Leakage Current in Float	-10	10	μA	V_{OUT}=0.4V to V_{CC}	[2]

Notes:
[1] Measurements made with outputs floating.
[2] A15-A0, D7-D0, /MREQ, /IORQ, /RD and /WR.
[3] I_{CC2} Standby Current is guaranteed when the halt pin is low in STOP mode.
[4] All Pins except XTALI, where I_{LI} = ± 25μA.
[5] A15-A0, D7-D0, /MREQ, /IORQ, /RD, /WR, /HALT, /M1 and /BUSACK.



I_{CC} vs Freq
CONDITIONS: V_{IHC}=V_{IH}=V_{CC}-0.2V V_{CC} = 5V, TEMP= 0°C to 70°C V_{ILC}=V_{IL} = 0.2V

Figure 26 Z84C01 Typical I_{CC} vs Freq

ELECTRICAL CHARACTERISTICS:

ABSOLUTE MAXIMUM RATINGS

Voltage on Vcc with respect to Vss..........-0.3V to + 7V
Voltages on all inputs with respect to Vss..-0.3V to Vcc + 0.3V
Operating Ambient
Temperature.......................See Ordering Information
Storage Temperature...............-65°C to + 150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Test Conditions

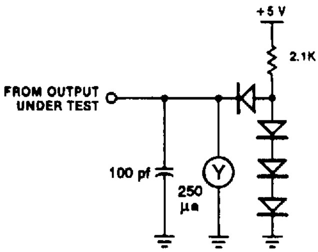
The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (OV). Positive current flows into the referenced pin.

Available operating temperature ranges are:

E = -40°C to +100°C
Voltage Supply Range: +4.50V ≤ V_{CC} ≤ +5.50V

All AC parameters assume a load capacitance of 100 pf. Add 10 ns delay for each 50 pf increase in load up to a maximum of 150 pf for the data bus and 100 pf for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pf.

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.



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