3.3V 1:4 Clock Fanout Buffer

Description

The NB3N2304NZ is a low skew 1-to 4 clock fanout buffer, designed for high speed clock distribution such as in PCI-X applications. The NB3N2304NZ guarantees low output-to-output skew. Optimal design, layout and processing minimizes skew within a device and from device-to-device.

The Output Enable (OE) pin forces the outputs LOW when LOW.

Features

- Input/Output Clock Frequency up to 140 MHz
- Low Skew Outputs (100 ps)
- Output Enable
- Operating Range: V_{DD} = 3.0 V to 3.6 V
- Ideal for PCI-X and networking clocks
- Packaged in 8-pin TSSOP, 4.4 mm x 3 mm
- Industrial Temperature Range
- These are Pb-Free Devices*

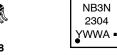


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MARKING DIAGRAM*





TSSOP-8 DT SUFFIX CASE 948S





A = Assembly Location

Y = Year WW = Work Week

■ = Pb-Free Package

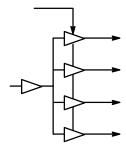


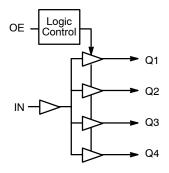
Figure 1. Simplified Logic Diagram

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

^{*}For additional marking information, refer to Application Note AND8002/D.





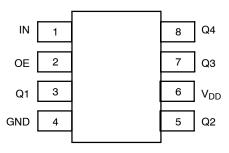


Figure 3. NB3N2304NZ Package Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Туре	Description
1	IN	LVCMOS/LVTTL Input	Clock Input
2	OE	LVCMOS/LVTTL Input	Output Enable for the clock outputs. Outputs are enabled when forced HIGH. Outputs are forced to logic LOW when OE is forced LOW.
3	Q1	LVCMOS/LVTTL Output	Clock Output 1
4	GND	Power	Negative Supply Voltage; Connect to Ground, 0 V
5	Q2	(LV)CMOS/(LV)TTL Input	Clock Output 2
6	V_{DD}	Power	Positive Supply Voltage (3.0 V to 3.6 V)
7	Q3	(LV)CMOS/(LV)TTL Output	Clock Output 3
8	Q4	(LV)CMOS/(LV)TTL Input	Clock Output 4

Table 2. OE, OUTPUT ENABLE FUNCTION TABLE

In	puts	Outputs
IN	OE	
L	L	L
Н	L	L
L	Н	L
Н	Н	Н

Table 3. ATTRIBUTES

Charac	Value				
ESD Protection Human Body Model Machine Model		> 2kV > 200 V			
Moisture Sensitivity, Indefinite T	Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)				
Flammability Rating	UL 94 V-O @ 0.125 in				
Transistor Count	480 Devices				
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test					

^{1.} For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{DD}	Positive Power Supply	GND = 0 V		V _{DD} + 0.5V	V
VI	Input Voltage			$GND - 0.5 \le V_{I} \le V_{DD} + 0.5$	V
T _A	Operating Temperature Range, Industrial			≥ -40 to ≤ +85	°C
T _{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8		°C/W °C/W
θJC	Thermal Resistance (Junction-to-Case)		TSSOP-8		°C/W
T _{SOL}	Wave Solder Pb-Free	(Note 2)		265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. EDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 5. DC CHARACTERISTICS $V_{DD} = 3.0 \text{ V}$ to 3.6 V, GND = 0 V, $T_A = -40 ^{\circ}\text{C}$ to $+85 ^{\circ}\text{C}$

Symbol	Characteristic			Тур	Max	Unit
I _{DD}	Power Supply Current @ 66.66 MHz, Unloaded Outputs			12	25	mA
V _{OH}	Output HIGH Voltage	– IOH = −24 mA –IOH = −12 mA	2.0 2.4			V
V _{OL}	Output LOW Voltage	-IOL = 24 mA -IOL = 12 mA			0.8 0.55	V
V _{IH}	Input HIGH Voltage, IN and OE (Note 3)		2.0			V
V _{IL}	Input LOW Voltage, IN and OE (Note 3)				0.8	V
I _{IH}	Input HIGH Current, V _{IN} = V _{DD}		-50		50	μΑ
I _{IL}	Input LOW Current, V _{IN} = 0 V		-100		100	μΑ
CIN	Input Capacitance, IN, OE			5	7	pF

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. IN input has a threshold voltage of $V_{DD}/2$.

Table 6. AC CHARACTERISTICS $V_{DD} = 3.0 \text{ V}$ to 3.6 V, GND = 0 V, $T_A = -40 ^{\circ}\text{C}$ to $+85 ^{\circ}\text{C}$ (Note 4) (Figure 4)

Symbol	Characteristic	Min	Тур	Max	Unit
f _{in}	Input Clock Frequency	DC		140	MHz
t _{DCskew}	Duty Cycle Skew = t2 ÷ t1 (Figure 4) Measured at 1.5 V	40	50	60	%
tr/tf	Output Rise and Fall Times; 0.8 V to 2.0 V		0.9	1.5	ns
t _{pd}	Propagation Delay, IN-to-Qn (Note 5)	2.5	3.5	5	ns
t _{skew}	Output-to-Output Skew; (Note 5)			100	ps
t _{pu}	Powerup Time for V _{DD} to Reach Minimum Specified Voltage	0.05		50	ms

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Measured on rising edges at $V_{DD} \div 2$; all outputs with equal loading.

^{4.} All outputs loaded equally with C_L = 25 pF to GND. Duty cycle out = duty in. A 0.01 μ F decoupling capacitor should be connected between V_{DD} and GND.

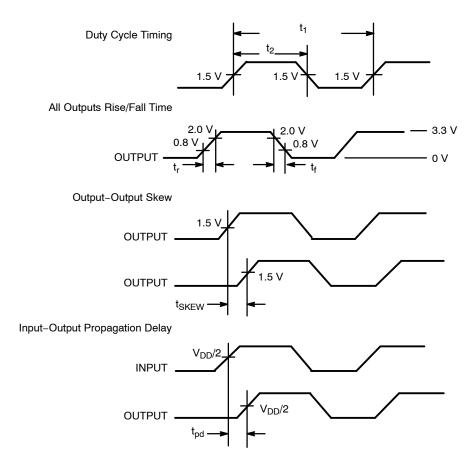


Figure 4. Switching Waveforms

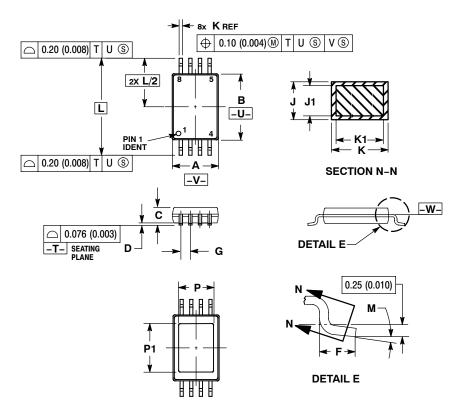
ORDERING INFORMATION

Device	Package	Shipping [†]
NB3N2304NZDTG	TSSOP-8 (Pb-Free)	100 Units / Rail
NB3N2304NZDTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
NB3N2304NZMNR4G*	DFN8 (Pb-Free)	1000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. *Contact a sales representative.

PACKAGE DIMENSIONS

TSSOP-8 CASE 948S-01 **ISSUE B**



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- PER SIDE.

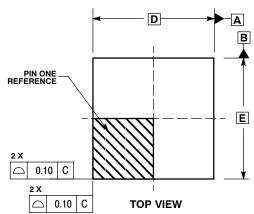
 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

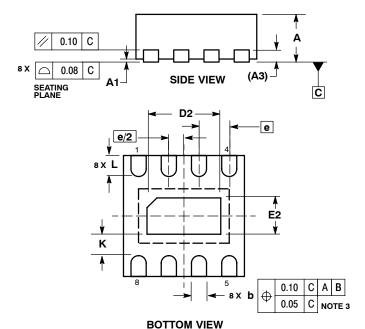
 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE W-.

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	2.90	3.10	0.114	0.122
В	4.30	4.50	0.169	0.177
С	-	1.10		0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65	BSC	0.026	BSC
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC			BSC
M	0°	8°	0°	8°
Р	-	2.20		0.087
P1		3.20		0.126

PACKAGE DIMENSIONS

DFN8 CASE 506AA-01 ISSUE D





NOTES:

- DIMENSIONING AND TOLERANCING PER
 ASME V14 FM 1994
- ASME Y14.5M, 1994 .
 2. CONTROLLING DIMENSION: MILLIMETERS.
- 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
 4. COPLANARITY APPLIES TO THE EXPOSED
- 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	MAX	
Α	0.80	1.00	
A1	0.00	0.05	
А3	0.20	REF	
b	0.20	0.30	
D	2.00	BSC	
D2	1.10	1.30	
Е	2.00	BSC	
E2	0.70	0.90	
е	0.50 BSC		
Κ	0.20		
L	0.25	0.35	

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