OXFORD SEMICONDUCTOR

Data Sheet

OXU121HP
USB On-The-Go Full-Speed Host and High-Speed Peripheral Controller

Features

- Single-chip USB OTG full-speed host and high-speed peripheral controller
  - Replaces two-chip system
  - Reduces system cost and board space
  - Minimizes system design complexity and power consumption
  - Simultaneous host and peripheral operation
- Compatible with the *Universal Serial Bus Specification*, Revision 2.0 and the *On-The-Go Supplement to the USB Specification 2.0,* Revision 1.0
- Single 3.3 V power supply, flexible I/O voltage of 1.65 V to 3.6 V (LVCMOS/TTL) to interface to a wide range of MCUs
- Low power operation, suitable for mobile applications
  - 30 mA (max) for host operation
  - 75 mA (max) for peripheral operation
- Power saving mode for the host controller and suspend mode for peripheral controller
- Integrated on-chip charge pump, supports up to 100 mA of current, enables support for broad range of USB devices
- Small package and footprint saves board space
  - 7×7 mm BGA, 84-ball, RoHS compliant
  - 12×12 mm LQFP, 100-pin, RoHS compliant
- 16-bit memory mapped interface can gluelessly interface to most popular microprocessors and DSPs
- Fast microprocessor access cycle and double/multi-buffering support for all four types of USB transfers
- Two DMA (slave) channels for the high-speed peripheral controller, lowering CPU utilization
- Integrated PLL supports external crystal or crystal oscillators of 12 MHz and 30 MHz, for system flexibility
- 16 Kbytes of on-chip SRAM, optimized buffer size for performance/cost

- Allows up to 8 bi-directional endpoints and transfers for support of multi-function systems
- Configurable hardware Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- Transaction scheduling and transfer level protocol implemented in hardware (including data toggle, retry and bandwidth management) for high performance
- Operating temperature range: -40 to 85 degrees C

Device Overview

The Oxford Semiconductor OXU121HP (formerly TD1120) is a single-chip USB On-The-Go (OTG) controller that incorporates a full-speed host and a high-speed peripheral controller. It enables an embedded system to operate as a USB host and a peripheral simultaneously, thereby dramatically expanding the degree of interconnectivity and extending the applicability of USB into many new areas, especially in mobile communication, consumer electronics, and printer applications. The combination of the OXU121HP high-speed peripheral and full-speed host controller enables users to perform high-speed USB data transfer for peripheral connectivity when connected to a host device, and operate at full speed in host mode operation to maximize system battery life in a mobile environment.

The OXU121HP is ideal for mobile applications. It enables high-speed PC synchronization to reduce data file transfer time when operating in USB peripheral mode. In host mode, it enables the system to connect to a wide range of USB devices such as flash drives, keyboards, mice, and digital still cameras (DSC). These mobile applications include smart phones, PDAs, MP3 players, portable media players, digital photo albums, and GPS devices.

The OXU121HP is well suited for PictBridge printers. It enables high-speed data transfer between PC and printer. While utilizing the host port, it adds PictBridge printing capability to the printer to support direct photo printing from a DSC. The OXU121HP replaces existing two-chip solutions by combining discrete host and peripheral controllers into a single chip, thus minimizing system cost, board space, design complexity, and power consumption.

The OXU121HP allows for simultaneous host and peripheral operation. The ports can be configured in one of two modes:

- 1 OTG + 1 Host: one OTG port and one full-speed host port
- 1 Peripheral + 2 Host: one high-speed peripheral port and two full-speed host ports

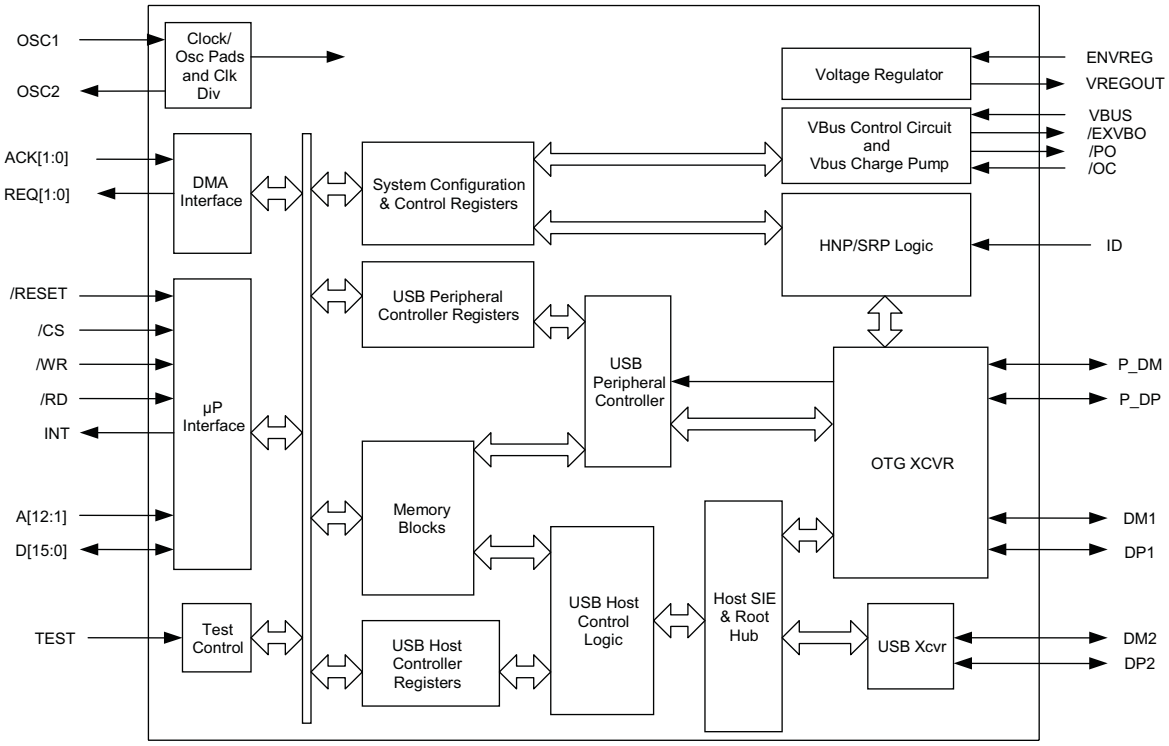
Software solutions for the OXU121HP include USB device drivers and the Oxford Semiconductor USBLink™ product suite. The USBLink host,

peripheral, and OTG stacks have been ported to a wide variety of real time operating systems including VxWorks®, ThreadX®, and Nucleus®.

In addition, Oxford Semiconductor also makes available low-level controller drivers for other native USB stacks such as those included with Windows® CE and Linux® 2.6.x.

Figure 1 shows the OXU121HP architectural diagram.

Figure 1 OXU121HP Architectural Diagram



Development Support

The OXU121HP product suite includes the USB controller as well as the protocol stacks and the driver software that enable a wide variety of USB applications. This unique ability to deliver a total hardware and software solution sets Oxford Semiconductor apart from other semiconductor companies and benefits customers by:

- Shortening time to market
- Reducing risk
- Offering a single source for hardware and software, thereby reducing the number of suppliers the customer has to deal with

Oxford Semiconductor is a Microsoft® Windows® Embedded Partner and has developed host and peripheral controller drivers for Windows CE 5.0. Similar software support is also available for Linux® 2.6.x.

For customers using a real time operating system (RTOS) such as VxWorks®, ThreadX®, Nucleus®, OSE, LynxOS® and AMX™ among others, Oxford Semiconductor offers its USBLink host, peripheral and On-The-Go software solutions.

The USBLink Product Suite is a modularized approach to providing USB connectivity for a wide variety of embedded products. Due to its flexible architecture and broad based support for USB host, peripheral and OTG applications, Oxford Semiconductor can tailor the USBLink software deliverables to meet each customer's USB requirements.

The USBLink solutions are configurable and can support systems with:

- Big or little endian processors
- DMA or non-DMA USB controllers
- A wide variety of USB controllers, including the OXU121HP
- A broad range of operating systems

Oxford Semiconductor has over eight years of experience developing embedded USB technology. Its USBLink software has been ported to twenty different operating systems and a wide variety of embedded architectures. USBLink is shipping in many millions of units.

Sample Applications

- Portable media players
- MP3 players
- Car audio & navigation
- Printers
- Smart mobile phones
- Digital televisions
- Home media centers
- Digital video cameras
- Digital still cameras
- External storage products
- Set-Top Boxes (STB)
- Personal Video Recorders (PVR)
- Personal Digital Assistants (PDA)
- DVD recorders

Electrical Characteristics

Tables 3 to 11 detail the required operating conditions for the device and the DC and AC electrical characteristics.

Table 1 Absolute Maximum Device Ratings

Symbol	Parameter	Condition	Min	Max	Unit
$V_{DD3.3}$	3.3 V power supply		-0.3	4.0	V
$V_{DD1.8}$	1.8 V power supply		-0.3	2.16	V
V_{DDW}	1.8 V to 3.3 V power supply		-0.3	4.0	V
V_I	DC input voltage		-0.3	4.0	V
T_S	Storage temperature		-40	+150	°C

Note: 1 Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the normal operating conditions specified in the following section. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
$V_{DD3.3}$	3.3 V power supply		2.97	3.63	V
$V_{DD1.8}$	1.8 V power supply		1.62	1.98	V
V_{DDW}	1.8 - 3.3 V wide-range I/O power supply		1.62	3.63	V
$V_{I3.3}$	DC input voltage of 3.3 V pins		0	3.6	V
V_{IW}	DC input voltage of wide-range pins		0	$1.1*V_{DDW}$	V
T_O	Operating temperature		-40	+85	°C

Table 3 DC Characteristics, Full-Speed USB I/O Signals: DP_1, DP_2, DM_1, DM_2

Symbol	Parameter	Condition	Min	Max	Unit
V_{DI}	Diff. input sensitivity	$\|V_{I(DP^N)} - V_{I(DM^N)}\|$ (where N = 1 or 2)	0.2		V
V_{CM}	Diff. comm. mode range		0.8	2.5	V
V_{OL}	Static output low		0.0	0.3	V
V_{OH}	Static output high		2.8	3.6	V
V_{CRS}	Output signal crossover		1.3	2.0	V
C_{IN}	Input capacitance			20	pF

Table 4 DC Characteristics, High-Speed USB I/O Signals: DP_P and DM_P Only

Symbol	Parameter	Condition	Min	Max	Unit
V_{HSDIFF}	High-speed differential input sensitivity	$\|V_{I(DP^P)} - VI(DM^P)\|$	300		mV
V_{HSCM}	High-speed data signaling common mode range		-50	500	mV
V_{HSSQ}	High-speed squelch detection threshold	Squelch detected		100	mV
		No squelch detected	150		mV
V_{HSIO}	High-speed idle output voltage (differential)		-10	10	mV
V_{HSOL}	High-speed low-level output voltage (differential)		-10	10	mV
V_{HSOH}	High-speed high-level output voltage (differential)		-360	400	mV
V_{CHIRPK}	Chirp-K output voltage (differential)		-900	-500	mV

Table 5 DC Characteristics, Logic Signals

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}	Low-level output voltage			0.4	V
V_{OH}	High-level output voltage	V_{DDW} = 3.3 V	2.4		V
		V_{DDW} = 1.8 V	0.75*V_{DDW}		V
V_{IL}	Low-level input voltage	V_{DDW} = 3.3 V		0.8	V
		V_{DDW} = 1.8 V		0.3*V_{DDW}	V
V_{IH}	High-level input voltage	V_{DDW} = 3.3 V	2.0		V
		V_{DDW} = 1.8 V	0.7*V_{DDW}		V
C_{IN}	Input capacitance		2.2 (typical)		pF
C_{OUT}	Output capacitance		2.2 (typical)		pF
C_{BI}	Bi-directional capacitance		2.2 (typical)		pF
I_{IN}	Input leakage current	No pull up or pull down	-10	10	µA

Note: The capacitances listed above do not include pad capacitance and package capacitance. One can estimate pin capacitance by adding pad capacitance of about 0.5 pF; and the package capacitance, which is about 0.86 pF max for QFP and 0.42 pF max for BGA.

Table 6 DC Characteristics, ID Resistance

Symbol	Parameter	Condition	Min	Max	Unit
$R_{B\text{-}PLUG\text{-}ID}$	Resistance to ground on mini-B plug		100 K		Ω
$R_{A\text{-}PLUG\text{-}ID}$	Resistance to ground on mini-A plug			10	Ω

Table 7 DC Characteristics, Regulator

Symbol	Parameter	Condition	Min	Max	Unit
RV_{out}	Output voltage	Driving current <= 100 mA	1.8 (typical)		V
RI_{drive}	Driving current	$V_{DD3.3A}$ = 3.3 V Output voltage = 1.8 V		150	mA
Rt_{st}	Start-up time when enabled	$V_{DD3.3A}$ = 3.3 V RV_{out} = 1.62 V (90%)	25 (typical)		µs

Note: The $V_{DD3.3A}$ pin that corresponds to the regulator supply is QFP pin 81 and BGA pin B9.

Table 8 DC Characteristics, Charge Pump

Symbol	Parameter	Condition	Min	Max	Unit
CV_{out}	Output voltage	Driving current <= 100 mA	4.75	5.07	V
$V_{DD1.8}$	Driving current	$V_{CPSUPPLY}$ = 3.3 V Output voltage = 5 V		100	mA
V_{DDW}	Start-up time when enabled	$V_{CPSUPPLY}$ = 3.3 V RV_{out} = 4.5 V (90%)	400 (typical)		µs

Note: The charge pump supply $V_{CPSUPPLY}$ supplies the external components of the charge pump circuit.

Table 9 AC Characteristics, High-Speed DP_P and DM_P Driver Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
t_{HSR}	High-speed differential rise time		500		ps
t_{HSF}	High-speed differential fall time		500		ps
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip	40.5	49.5	Ω

Table 10 AC Characteristics, Full-Speed DP_1, DP_2, DM_1, DM_2 Driver Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
t_{FR}	Rise time	C_L = 50 pF	4	20	ns
t_{FF}	Fall time	C_L = 50 pF	4	20	ns
t_{FRFM}	T_R/T_F matching		90	110	%
Z_{DRV}	Driver output resistance	Steady state drive with external 33 Ω series resistor	3	9	Ω

Table 11 AC Characteristics, Low-Speed DP_1, DP_2, DM_1, DM_2 Driver Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
t_{LR}	Rise time	C_L = 200 - 600 pF	75	300	ns
t_{LF}	Fall time	C_L = 200 - 600 pF	75	300	ns
t_{FRFM}	T_R/T_F matching		80	125	%

Power Consumption

Table 12 gives typical power consumption figures for the OXU121HP.

Table 12 OXU121HP Power Consumption

	Condition	Min	Max	Unit
Host operational current	ENVREG = 1		30	mA
Peripheral operational current	High-speed, ENVREG = 1		75	mA
	Full-speed, ENVREG = 1		50	mA
Host suspend state current	ENVREG = 1	150 (typical)		µA
Peripheral suspend state current	ENVREG = 1	400 (typical)		µA
Power save state current	ENVREG = 1	150 (typical)		µA

The above measurements are at typical process corner and room temperature and do not account for process and temperature variations.

Peripheral operational current is measured with 5 m cable with maximum switching and BULK OUT transfer at 400 Mbps with 92.6% bus utilization during one microframe. The actual average current in customer applications will be lower.

Pin Layout

The OXU121HP is supplied as a 100-pin LQFP package and as a 84-ball BGA package. Figure 2 shows the chip layout of the 100-pin LQFP package.

Figure 2 OXU121HP 100-Pin LQFP Package (Top View)

Table 13 lists the LQFP pin allocations.

*Table 13 OXU121HP **100-Pin LQFP** Pin Allocations (Sheet 1 of 3)*

Pin	No. Bits	Type[(1)]	Name	Description
Processor Interface (37 pins)				
2, 3, 4, 5, 8, 9, 10, 11, 13, 14, 15, 16, 96, 97, 98, 99	16	MSBCT	D_0 - D_{15}	16-bit data bus. Pull-up/pull-down can be controlled through register 0x034, bits 2:1. Default is none
22, 23, 24, 25, 28, 29, 30 32, 33, 34, 35, 36	12	MSID	A_1 - A_{12}	Address bus for direct address space of 8 Kbytes. Pull-up can be enabled through register 0x034, bits 9:8. Default is pull-down
20	1	MSIU	/WR	Write strobe. Pull-up can be disabled through register 0x034, bit 13. Default is pull-up
21	1	MSIU	/RD	Read strobe. Pull-up can be disabled through register 0x034, bit 13. Default is pull-up
39	1	MSIU	/CS	Chip select. Pull-up can be disabled through register 0x034, bit 13. Default is pull-up
19	1	MOCT	/INT	Interrupt to the MCU.This pin can be software configured as a driven output or open drain. Open drain is the default
86	1	MSIU	/RESET	Hardware reset. Pull-up is always enabled
89, 92	2	MOCT	DRQ_1, DRQ_0	DMA request outputs to support two channels
90, 93	2	MSI	ACK_1, ACK_0	DMA acknowledge. Pull-up/pull-down can be controlled through register 0x03A, bits 1:0. Default is none
General Purpose I/O (1 pin)				
88	1	BC	GPIO	General purpose I/O
Power & Ground (34 pins)				
1, 12, 27, 41, 51, 65, 75, 83	8		V_{SS}	Digital/wide-range ground
42, 47, 69, 74, 82	5		V_{SSA}	Analog ground
6, 18, 40, 53, 57, 66, 84, 100	8		$V_{DD1.8}$	1.8 V core power. VREGOUT may be used for the supplies
43, 48, 70, 73, 81	5		$V_{DD3.3A}$	Analog +3.3 V power
56, 78	2		$V_{DD3.3}$	Digital +3.3 V power
7, 17, 26, 31, 85, 95	6		V_{DDW}	Wide-range I/O +1.8 V to +3.3 V. If using +1.8 V, VREGOUT may be used for these supplies
USB Interface (13 pins)				
76, 77	2	B	DP_2, DM_2	Data lines for host port 2, a dedicated USB host port. If not used, these pins should be left floating
54, 55	2	B	DP_1, DM_1	Data lines for host port 1, which can serve as a USB host or an OTG port in combination with the peripheral port. If not used, these pins should be left floating

*Table 13 OXU121HP **100-Pin LQFP** Pin Allocations (Sheet 2 of 3)*

Pin	No. Bits	Type[(1)]	Name	Description
44, 45	2	B	DP_P, DM_P	Data lines for USB peripheral port, which can serve as an OTG port in combination with host port 1. If not used, these pins should be left floating
46	1	B	R_{REF}	Connect external reference resistor (12 KΩ +/- 1%) to V_{SSA}
72	1	5I	VBUS	VBUS input used by the voltage comparators of the OTG port for connection. This pin should be left floating in a host-only application
60	1	OC	VBP	VBUS pulsing control. This pin is used only when the OTG port is operating as a B-device
59	1	O	/EXVBO	Turn on/off the external V_{BUS} (5 V) for OTG operation (1:V_{BUS} off, 0: V_{BUS} on) when using the external VBUS source
58	1	IU	/OC	Over current condition indicator for powered host ports. Pull-up is always enabled
62	1	IU	ID	Connected to the ID pin of the mini-AB connector for OTG applications. With the help of an internal pull-up resistor, this pin determines the chip's responsibility in an OTG application (0: A-device, 1:B-device). Pull-up can be disabled through register 0x038, bits 7:6. Default is pull-up
61	1	O	/PO	Turn on/off gang power for all host ports
Clock Interface (3 pins)				
50	1	I	OSC_1	Input. A 12 MHz or 30 MHz passive crystal should be connected across the two pins (OSC_1 and OSC_2). Optionally, a 12 MHz or 30 MHz oscillator can be connected to OSC_1 while keeping OSC_2 unconnected
49	1	O	OSC_2	Output
63	1	I	CLKCFG	Indicates whether a 12 MHz or a 30 MHz crystal/ oscillator is being used. 0 = 12 MHz crystal or 12 MHz 3.3 V oscillator input on OSC_1 1 = 30 MHz crystal or 30 MHz 3.3 V oscillator input on OSC_1
Internal VBUS Charge Pump (3 pins)				
68	1	O	PD_PMOS	Internal charge pump output for P-MOSFET (optional switch on the VOUT)
71	1	O	EXT	Internal charge pump output for N-MOSFET
67	1	I	VOUT	Internal charge pump output voltage feedback pin
Internal Voltage Regulator (2 pins)				
79	1	I	ENVREG	Enables the internal voltage regulator if asserted. If not used, this pin should be tied to V_{SS}

*Table 13 OXU121HP **100-Pin LQFP** Pin Allocations (Sheet 3 of 3)*

Pin	No. Bits	Type[1]	Name	Description
80	1	O	VREGOUT	Internal voltage regulator output of 1.8 V. If enabled, this output should be connected to the $V_{DD1.8}$ (and V_{DDW} if wide-range IO is at 1.8 V) supplies of the chip. If the regulator is disabled, then this pin should be treated as another $V_{DD1.8}$ supply input to the chip
Test (3 pins)				
87	1	ID	TEST	Factory test mode. This pin should be grounded or left floating (has an internal pull-down) for normal operation. Pull-down is always enabled
37	1	ID	ATEST13	Additional address pin for debug use. Should be grounded or left floating (has an internal pull down) for normal use. Pull-down is always enabled
64	1	I	XMODE	This pin must be grounded for normal operation
Miscellaneous (4 pins)				
91, 94	2	-	$RSVD_0$, $RSVD_1$	Reserved
38, 52	2	-	NC	No connection. This pin should be left floating

Note to Table 13: 1 Type key: format is [(L)(W_)X(Y)(_Z(A))] where the following conventions apply:

L—Logic Level		W—Tolerance		X—Type		Y—Pull		Z—Drive	T—Tristate	
M[2]	Multi-voltage: 3.3 V CMOS 2.5 V CMOS 1.8 V CMOS	5	5 V	I	Input	U	Pull up	C[3]	T	Tristate
			3.3 V	O	Output	D	Pull down			Normal
S	Schmitt Trigger			B	Bidirectional		None			

2 Program to 3.3, 2.5, or 1.8 V by setting the V_{IO} voltage level.

3 Program to 2 mA, 4 mA, 6 mA, 8 mA, 10 mA, 12 mA, 14, mA, or 16 mA via the I/O Configuration Register (0x034).

Figure 3 shows the chip layout of the 84-ball BGA package.

Figure 3 OXU121HP 84-Ball BGA Package (Top View)

	A	B	C	D	E	F	G	H	J	K
10	DM_2	V_{SSA}	V_{SSA}	EXT	VOUT	XMODE	/PO	/OC	DP_1	OSC_1
9	DP_2	$V_{DD3.3A}$	$V_{DD3.3A}$	$V_{DD3.3A}$	PD_PMOS	CLKCFG	VBP	DM_1	OSC_2	$V_{DD3.3A}$
8	VREGOUT	ENVREG	V_{SS}	VBUS	V_{SSA}	ID	/EXVBO	$V_{DD3.3}$	R_{REF}	V_{SSA}
7	TEST	GPIO	DRQ_0					$V_{DD3.3A}$	DP_P	DM_P
6	DRQ_1	/RESET	$V_{DD3.3}$					V_{SS}	/CS	V_{SSA}
5	ACK_0	$RSVD_0$	$V_{DD1.8}$					V_{DDW}	A_{12}	ATEST13
4	ACK_1	$RSVD_1$	D_1					A_{10}	A_9	A_{11}
3	D_0	D_2	V_{SS}	D_{11}	$V_{DD1.8}$	V_{DDW}	/WR	$V_{DD1.8}$	A_7	A_8
2	D_3	D_6	D_8	D_{10}	D_{13}	D_{14}	INT	A_2	A_3	A_5
1	D_4 ●	D_5	D_7	D_9	D_{12}	D_{15}	/RD	A_1	A_4	A_6

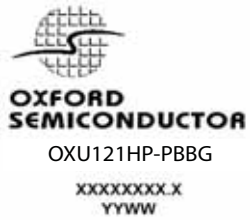


Table 14 lists the BGA pin allocations.

Table 14 OXU121HP 84-Ball BGA Pin Allocations (Sheet 1 of 3)

Pin	No. Bits	Type[(1)]	Name	Description
Processor Interface (37 pins)				
A3, C4, B3, A2, A1, B1, B2, C1, C2, D1, D2, D3, E1, E2, F2, F1	16	MSBCT	D_0 - D_{15}	16-bit data bus. Pull-up/pull-down can be controlled through register 0x034, bits 2:1. Default is none
H1, H2, J2, J1, K2, K1, J3, K3, J4, H4, K4, J5	12	MSID	A_1 - A_{12}	Address bus for direct address space of 8 Kbytes. Pull-up can be enabled through register 0x034, bits 9:8. Default is pull-down
G3	1	MSIU	/WR	Write strobe. Pull-up can be disabled through register 0x034, bit 13. Default is pull-up
G1	1	MSIU	/RD	Read strobe. Pull-up can be disabled through register 0x034, bit 13. Default is pull-up
J6	1	MSIU	/CS	Chip select. Pull-up can be disabled through register 0x034, bit 13. Default is pull-up
G2	1	MOCT	/INT	Interrupt to the MCU.This pin can be software configured as a driven output or open drain. Open drain is the default
B6	1	MSIU	/RESET	Hardware reset. Pull-up is always enabled
C7, A6	2	MOCT	DRQ_0, DRQ_1	DMA request outputs to support two channels
A5, A4	2	MSI	ACK_1, ACK_0	DMA acknowledge. Pull-up/pull-down can be controlled through register 0x03A, bits 1:0. Default is none
General Purpose I/O (1 pin)				
B7	1	B	GPIO	General purpose I/O
Power & Ground (20 pins)				
C3, C8, H6	3		V_{SS}	Digital ground
B10, C10, E8,K6, K8	5		V_{SSA}	Analog ground
C5, E3, H3	3		$V_{DD1.8}$	1.8 V core power. VREGOUT may be used for these supplies
B9, C9, D9, H7, K9	5		$V_{DD3.3A}$	Analog +3.3 V power
C6, H8	2		$V_{DD3.3}$	Digital +3.3 V power
F3, H5	2		V_{DDW}	Wide-range I/O +1.8 V to +3.3 V. If using +1.8 V, VREGOUT may be used for these supplies
USB Interface (13 pins)				
A9, A10	2	B	DP_2, DM_2	Data lines for host port 2, a dedicated USB host port. If not used, these pins should be left floating
J10, H9	2	B	DP_1, DM_1	Data lines for host port 1, which can serve as a USB host or an OTG port in combination with the peripheral port. If not used, these pins should be left floating
J7, K7	2	B	DP_P, DM_P	Data lines for USB peripheral port, which can serve as an OTG port in combination with host port 1. If not used, these pins should be left floating

Table 14 OXU121HP 84-Ball BGA Pin Allocations (Sheet 2 of 3)

Pin	No. Bits	Type[(1)]	Name	Description
D8	1	5I	VBUS	VBUS input used by the voltage comparators of the OTG port for connection. This pin should be left floating in a host only application
G9	1	OC	VBP	VBUS pulsing control. This pin is used only when the OTG port is operating as a B-device
G8	1	P5O	/EXVBO	Turn on/off the external V_{BUS} (5 V) for OTG operation (1:V_{BUS} off, 0:V_{BUS} on) when using the external charge pump
H10	1	IU	/OC	Over current condition indicator for powered host ports. Pull-up is always enabled
J8	1	B	R_{REF}	Connect external reference resistor (12 KΩ +/- 1%) to V_{SSA}
F8	1	IU	ID	Connected to the ID pin of the mini-AB connector for OTG applications. With the help of an internal pull-up resistor, this pin determines the chip's responsibility in an OTG application (0: A-device, 1:B-device). Pull-up can be disabled through register 0x038, bits 7:6. Default is pull-up
G10	1	P5O	/PO	Turn on/off gang power for all host ports
Clock Interface (3 pins)				
K10	1	I	OSC_1	Input. A 12 MHz or 30 MHz passive crystal should be connected across the two pins (OSC_1 and OSC_2). Optionally, a 12 MHz or 30 MHz oscillator can be connected to OSC_1 while keeping OSC_2 unconnected
J9	1	O	OSC_2	Output
F9	1	I	CLKCFG	Indicates whether a 12 MHz or a 30 MHz crystal/oscillator is being used. 0 = 12 MHz crystal or 12 MHz 3.3 V oscillator input on OSC_1 1 = 30 MHz crystal or 30 MHz 3.3 V oscillator input on OSC_1
Internal VBUS Charge Pump (3 pins)				
E9	1	O	PD_PMOS	Internal charge pump output for P-MOSFET (optional switch on the VOUT)
D10	1	O	EXT	Internal charge pump output for N-MOSFET
E10	1	I	VOUT	Internal charge pump output voltage feedback pin
Internal Voltage Regulator (2 pins)				
B8	1	I	ENVREG	Enables the internal voltage regulator if asserted. If not used, this pin should be tied to V_{SS}
A8	1	O	VREGOUT	Internal voltage regulator output of 1.8 V. If enabled, this output should be connected to the $V_{DD1.8}$, (and V_{DDW} if wide-range IO is at 1.8 V) supplies of the chip. If the regulator is disabled, then this pin should be treated as another $V_{DD1.8}$ supply input to the chip

Table 14 OXU121HP 84-Ball BGA Pin Allocations (Sheet 3 of 3)

Pin	No. Bits	Type[1]	Name	Description
Test (3 pins)				
A7	1	ID	TEST	Factory test mode. This pin should be grounded or left floating (has an internal pull-down) for normal operation. Pull-down is always enabled
K5	1	ID	ATEST13	Additional address pin for debug use. Should be grounded or left floating (has an internal pull down) for normal use. Pull-down is always enabled
F10	1	I	XMODE	This pin must be grounded for normal operation
Miscellaneous (2 pins)				
B5, B4	2	-	$RSVD_0$, $RSVD_1$	Reserved

Note to Table 14: 1 Type key: format is [(L)(W_)X(Y)(_Z(A))] where the following conventions apply:

L—Logic Level		W—Tolerance		X—Type		Y—Pull		Z—Drive	T—Tristate	
M[2]	Multi-voltage: 3.3 V CMOS 2.5 V CMOS 1.8 V CMOS	5	5 V	I	Input	U	Pull up	C[3]	T	Tristate
			3.3 V	O	Output	D	Pull down			Normal
S	Schmitt Trigger			B	Bidirectional		None			

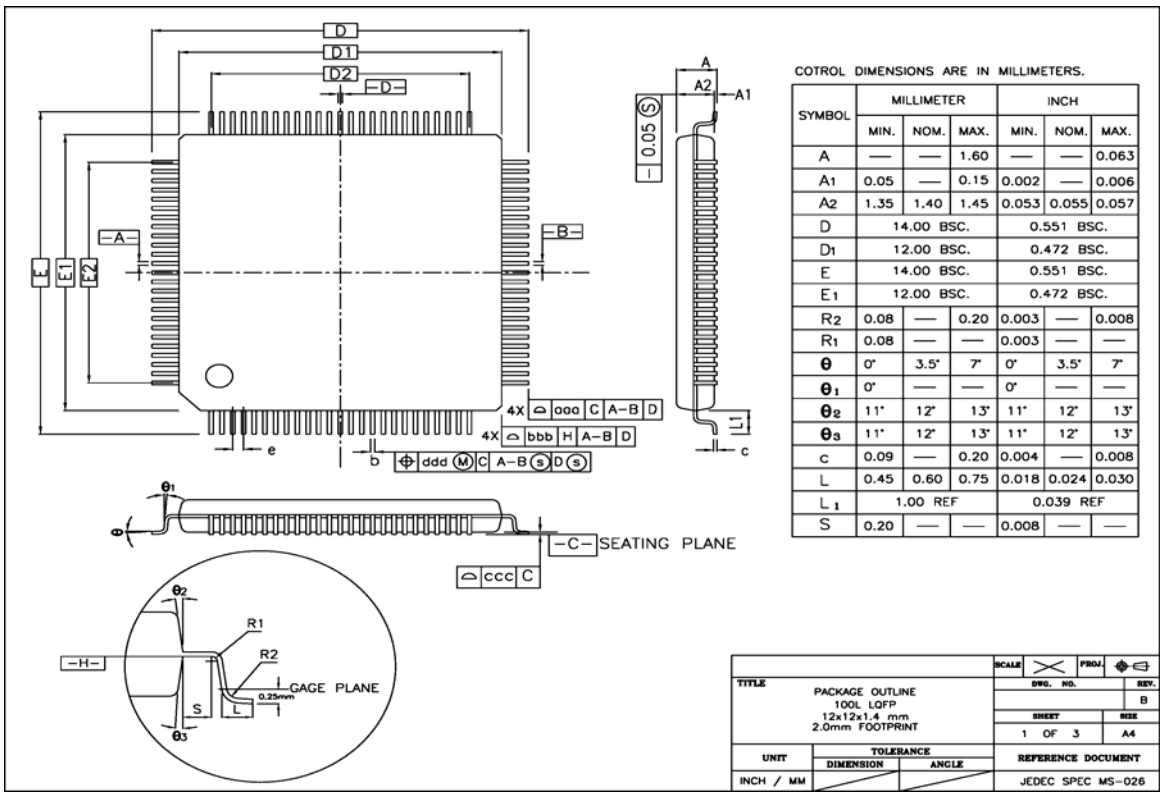
2 Program to 3.3, 2.5, or 1.8 V by setting the V_{IO} voltage level.

3 Program to 2 mA, 4 mA, 6 mA, 8 mA, 10 mA, 12 mA, 14, mA, or 16 mA via the I/O Configuration Register (0x034).

Package Layout

Figure 4 shows the package layout for the 100-pin LQFP package.

Figure 4 100-Pin LQFP



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	14.00 BSC.			0.551 BSC.		
D1	12.00 BSC.			0.472 BSC.		
E	14.00 BSC.			0.551 BSC.		
E1	12.00 BSC.			0.472 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

TITLE: PACKAGE OUTLINE 100L LQFP 12x12x1.4 mm 2.0mm FOOTPRINT		SCALE:	PROJ.
		DWG. NO.	REV. B
		SHEET 1 OF 3	SIZE A4
UNIT: INCH / MM	TOLERANCE: DIMENSION / ANGLE	REFERENCE DOCUMENT: JEDEC SPEC MS-026	

SYMBOL	100L						
	MILLIMETER			INCH			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
b	0.13	0.16	0.23	0.005	0.006	0.009	
e	0.40 BSC.			0.016 BSC.			
D2	9.60			0.378			
E2	9.60			0.378			
TOLERANCES OF FORM AND POSITION							
aaa	0.20			0.008			
bbb	0.20			0.008			
ccc	0.08			0.003			
ddd	0.07			0.003			

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.

TITLE: PACKAGE OUTLINE 100L LQFP 12x12x1.4 mm 2.0mm FOOTPRINT		SCALE:	PROJ.
		DWG. NO.	REV. B
		SHEET 2 OF 3	SIZE A4
UNIT: INCH / MM	TOLERANCE: DIMENSION / ANGLE	REFERENCE DOCUMENT: JEDEC SPEC MS-026	

Figure 5 shows the layout for the 84-ball TFBGA.

Figure 5 84-Ball TFBGA Package

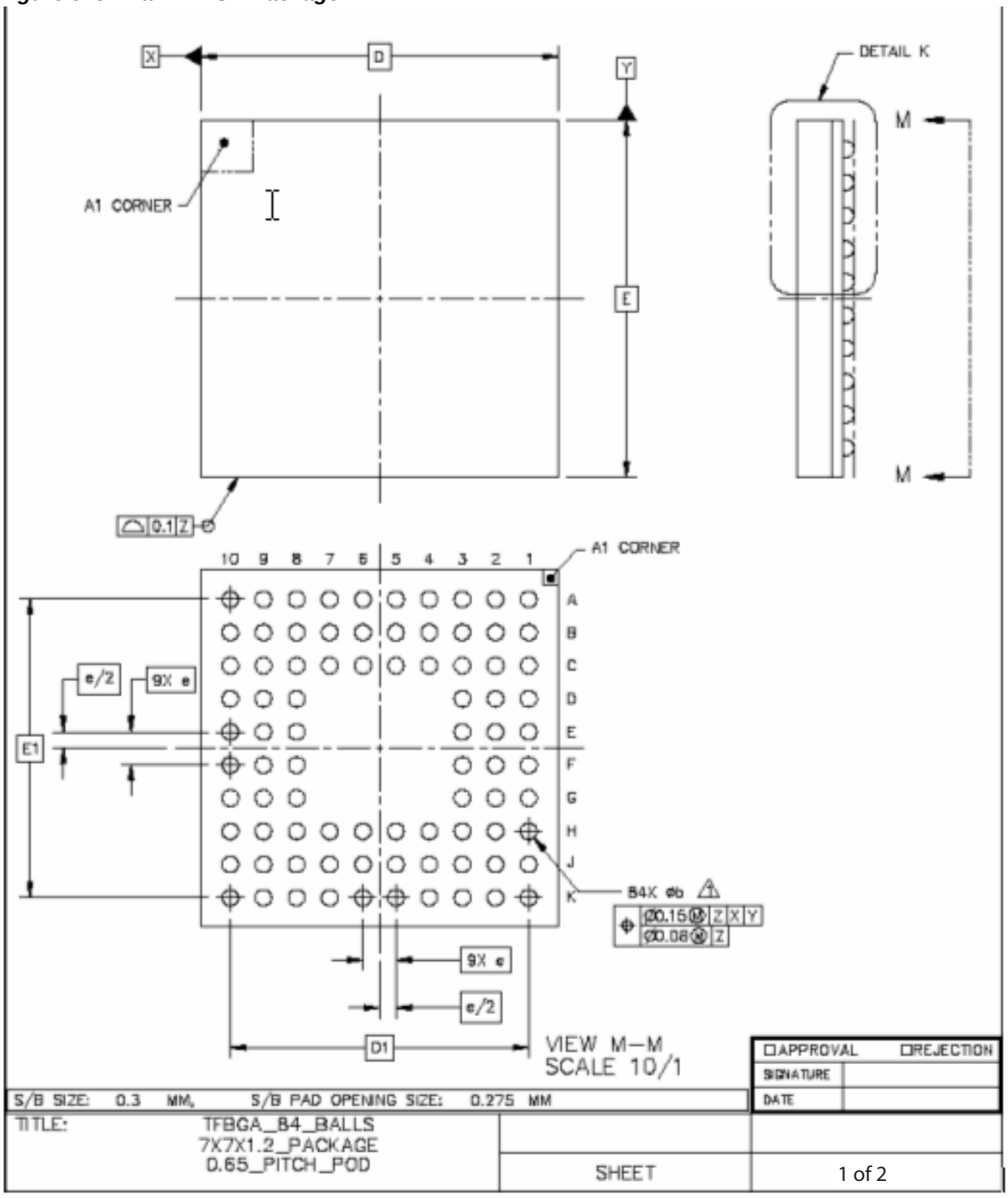
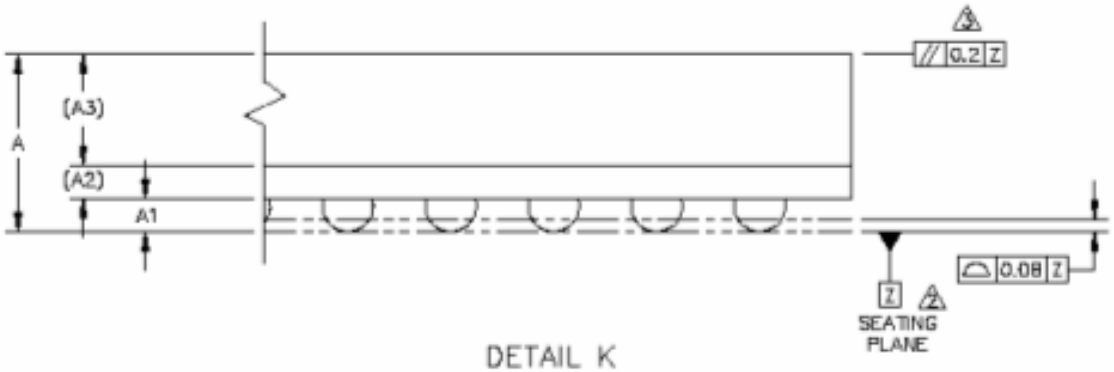


Figure 5 84-Ball TFBGA Package (continued)

	PACKAGE OUTLINE		98A0084MB014
			D



DETAIL K
SCALE 25/1
(ROTATE 90°)

DIM	MIN.	NOR.	MAX.
A	---		1.2
A1	0.16		0.26
A2		0.21 REF	
A3		0.7 REF	
b	0.27		0.37
D		7 BSC	
E		7 BSC	
e		0.65 BSC	
D1		5.85 BSC	
E1		5.85 BSC	

NOTES

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
2. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
UNIT	ASME_Y14.5M	REFERENCE_DOCUMENT
TITLE: TFBGA_84_BALLS 7X7X1.2_PACKAGE 0.65_PITCH_POD		
	SHEET	2 of 2

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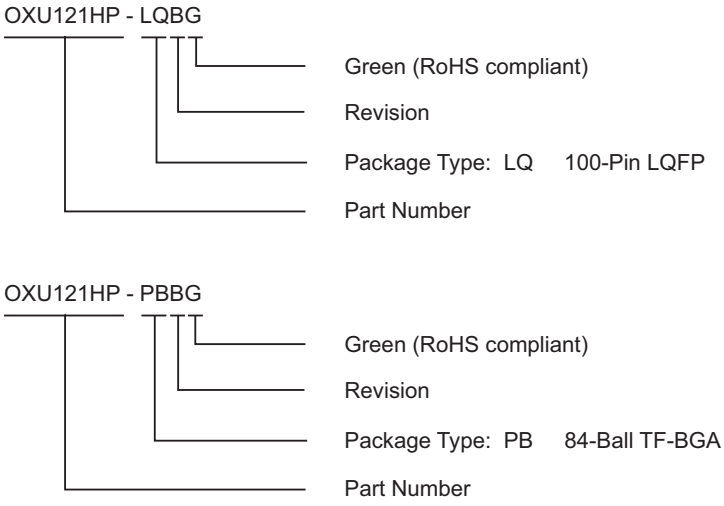
The following conventions are used to identify Oxford Semiconductor products.



Contacting Oxford Semiconductor

See the Oxford Semiconductor website (http://www.oxsemi.com) for further detail about Oxford Semiconductor devices, or email sales@oxsemi.com.

Revision Information

Table 15 documents the revisions of this guide.

Table 15 Revision Information

Revision	Modification
August 06	First publication

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