STGW39NC60VD

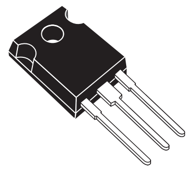
N-channel 40A - 600V - TO-247
Very fast switching PowerMESH™ IGBT

PRELIMINARY DATA

General features

Type	V_{CES}	$V_{CE(sat)}$ (Max)@ 25°C	I_C @100°C
STGW39NC60VD	600V	<2.5V	40A

- Low C_{RES} / C_{IES} ratio (no cross conduction susceptibility)
- High frequency operation
- Very soft ultra fast recovery anti parallel diode

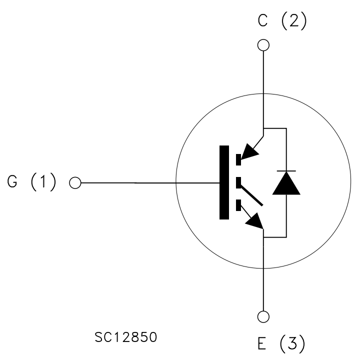


TO-247

Description

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix "V" identifies a familyoptimized for high frequency application.

Internal schematic diagram



Applications

- High frequency inverters, ups
- Motor drivers
- Induction heating

Order codes

Part number	Marking	Package	Packaging
STGW39NC60VD	GW39NC60VD	TO-247	Tube

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GS} = 0)	600	V
I_C (1)	Collector current (continuous) at 25°C	70	A
I_C (1)	Collector current (continuous) at 100°C	40	A
I_{CL} (2)	Collector current (pulsed)	220	A
V_{GE}	Gate-emitter voltage	± 20	V
I_F	Diode RMS forward current at Tc=25°C	15	A
P_{TOT}	Total dissipation at T_C = 25°C	250	W
T_j	Operating junction temperature	– 55 to 150	°C
T_{stg}	Storage temperature		
T_L	Maximum lead temperature for soldering purpose (1.6 mm from case, for 10 sec.)	300	°C

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. Vclamp = 480V , Tj = 150°C, R_G = 10Ω, V_{GE}= 15V

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	0.5	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient Max	50	°C/W

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	I_C = 1mA, V_{GE} = 0	600			V
$V_{CE(SAT)}$	Collector-emitter saturation voltage	V_{GE}=15V, I_C=30A,Tj=25°C V_{GE}=15V, I_C=30A,Tj=125°C		1.8 1.6	2.5	V V
$V_{GE(th)}$	Gate threshold voltage	V_{CE}= V_{GE}, I_C= 250µA	3.75		5.75	V
I_{CES}	Collector-emitter leakage current (V_{GE} = 0)	V_{CE} = Max rating,Tc=25°C V_{CE}= Max rating, Tc=125°C			500 10	µA mA
I_{GES}	Gate-emitter leakage current (V_{CE} = 0)	V_{GE} = ± 20V , V_{CE} = 0			± 100	nA
g_{fs}	Forward transconductance	V_{CE} = 15V, I_C= 30A		20		S

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies} C_{oes} C_{res}	Input capacitance Output capacitance Reverse transfer capacitance	V_{CE} = 25V, f = 1 MHz, V_{GE}= 0		2900 298 59		pF pF pF
Q_g Q_{ge} Q_{gc}	Total gate charge Gate-emitter charge Gate-collector charge	V_{CE} = 390V, I_C = 30A, V_{GE} = 15V, *(see Figure 16)*		126 16 46		nC nC nC

Table 5. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $(di/dt)_{onf}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC}=390 V, I_C= 30A, R_G=10Ω, V_{GE}=15V Tj=25°C *(see Figure 15)*		33 13 2500		ns ns A/µs
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC}=390 V, I_C= 30A, R_G=10Ω, V_{GE}=15V Tj=125°C *(see Figure 15)*		32 14 2280		ns ns A/µs
$t_{r(Voff)}$ $t_{d(off)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC}=390 V, I_C= 30A, R_G=10Ω, V_{GE}=15V Tj=25°C *(see Figure 15)*		33 178 65		ns ns ns
$t_{r(Voff)}$ $t_{d(off)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC}=390 V, I_C= 30A, R_G=10Ω, V_{GE}=15V Tj=125°C *(see Figure 15)*		68 238 128		ns ns ns

Table 6. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
E_{on} (1) E_{off}(2) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 390V, I_C = 30A R_G= 10Ω, V_{GE}= 15V, Tj= 25°C *(see Figure 17)*		333 537 870		µJ µJ µJ
E_{on} (1) E_{off} (2) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 390V, I_C = 30A R_G= 10Ω, V_{GE}= 15V, Tj= 125°C *(see Figure 17)*		618 1125 1743		µJ µJ µJ

1. Eon is the tun-on losses when a typical diode is used in the test circuit in figure 2 Eon include diode recovery energy. If the IGBT is offered in a package with a co-pak diode, the co-pack diode is used as external diode. IGBTs & Diode are at the same temperature (25°C and 125°C)
2. Turn-off losses include also the tail of the collector current

Table 7. Collector-emitter diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
V_f	Forward on-voltage	If = 15A If = 15A, Tj = 125°C		1.6 1.4	2.8	V V
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	If = 15A, V_R = 40 V, T_j = 25°C, di/dt =100A/µs *(see Figure 18)*		45 56 2.55		ns nC A
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	If = 15A, V_R = 40V, T_j = 125°C,di/dt =100A/µs *(see Figure 18)*		100 290 5.8		ns nC A

2.1 Electrical characteristics (curves)

Figure 1. Output characterisics

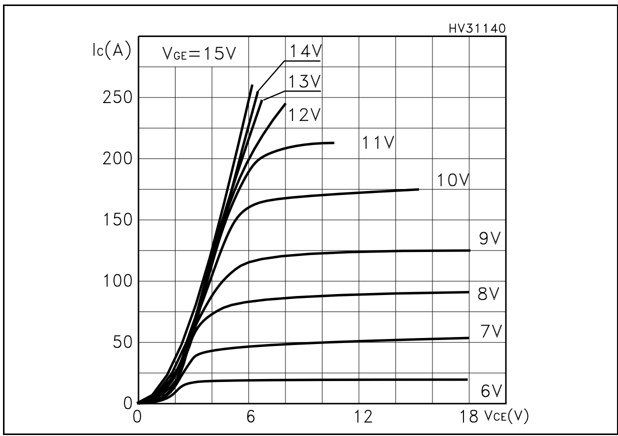


Figure 2. Transfer characteristics

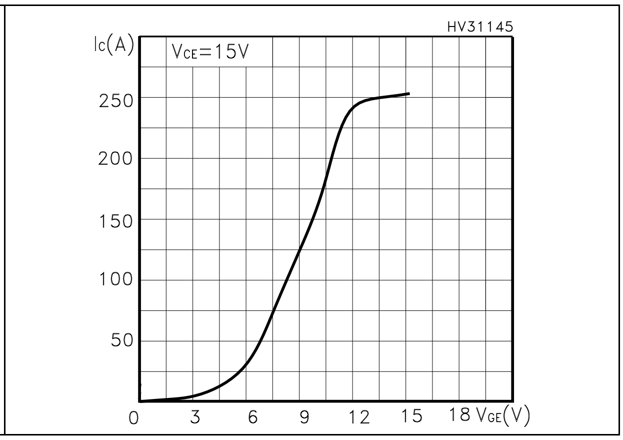


Figure 3. Transconductance

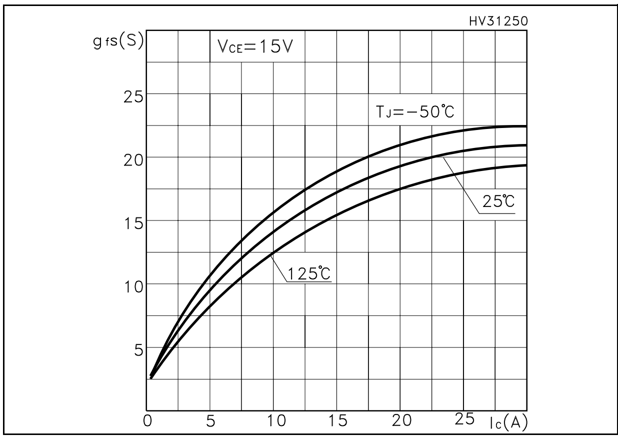


Figure 4. Collector-emitter on voltage vs temperature

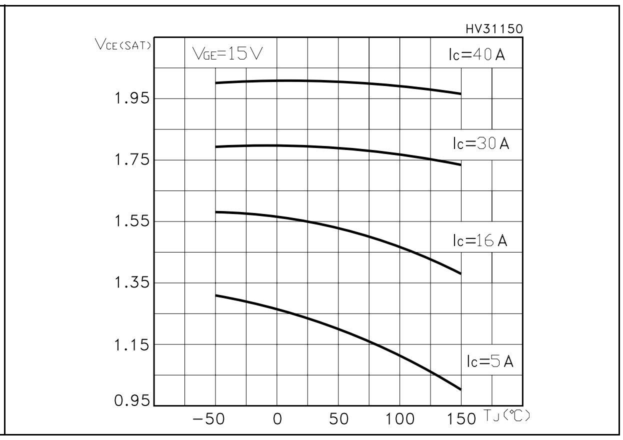


Figure 5. Collector-emitter on voltage vs collector current

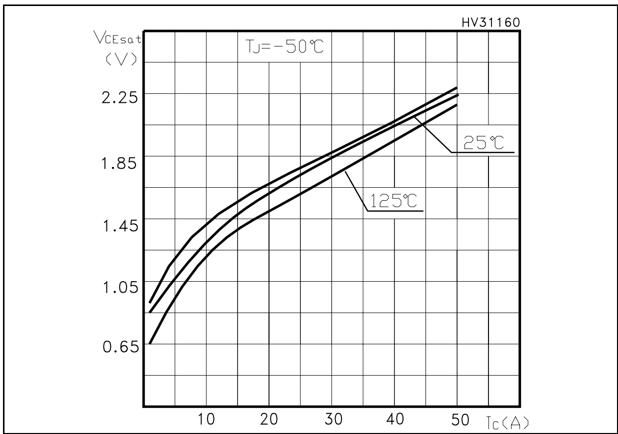


Figure 6. Normalized gate threshold vs temperature

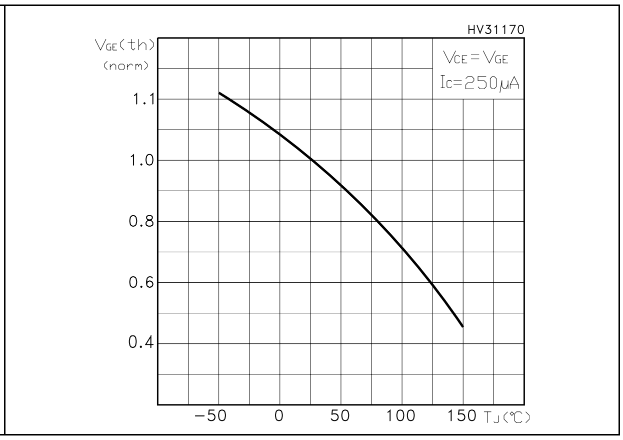


Figure 7. Normalized breakdown voltage vs temperature

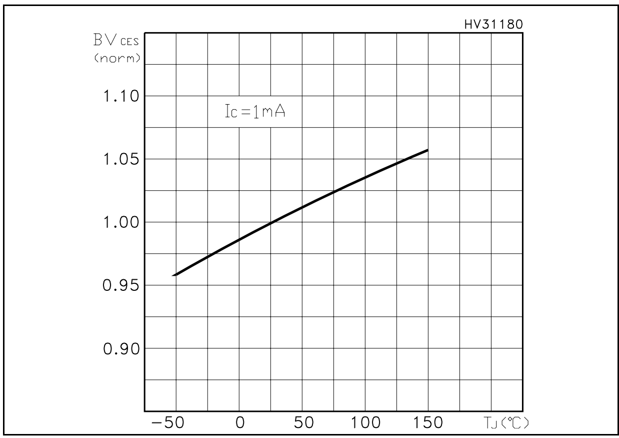


Figure 8. Gate charge vs gate-emitter voltage

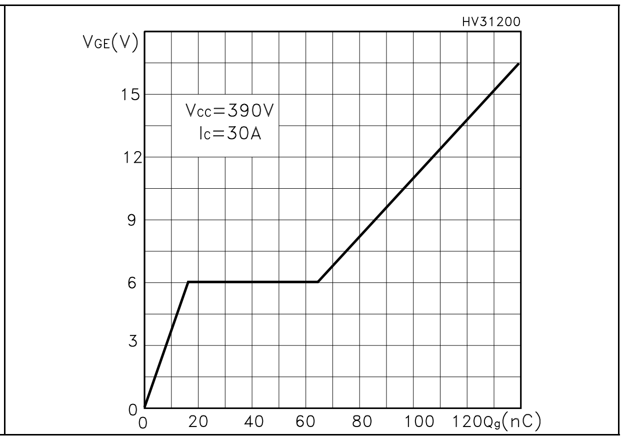


Figure 9. Capacitance variations

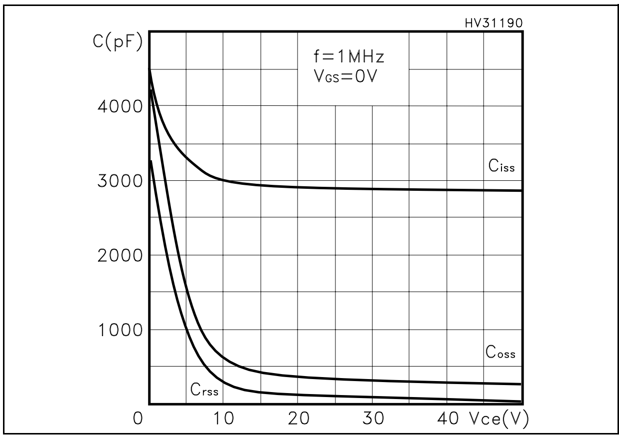


Figure 10. Switching losses vs temperature

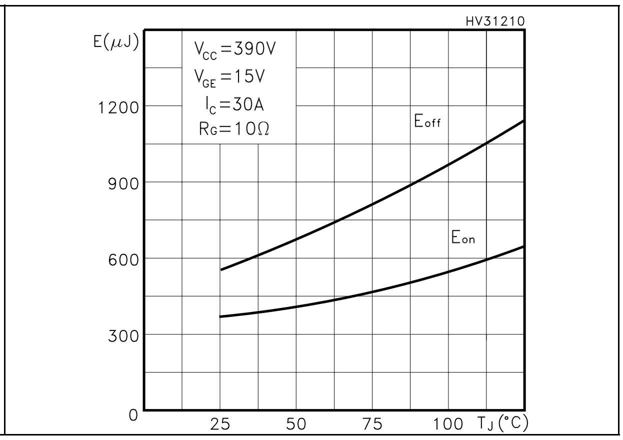


Figure 11. Switching losses vs gate resistance

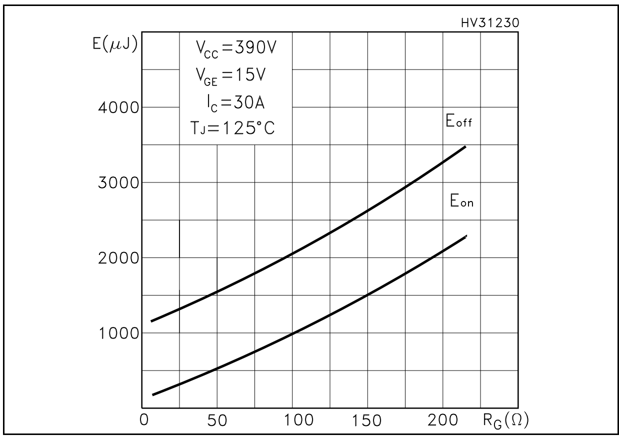


Figure 12. Switching losses vs collector current

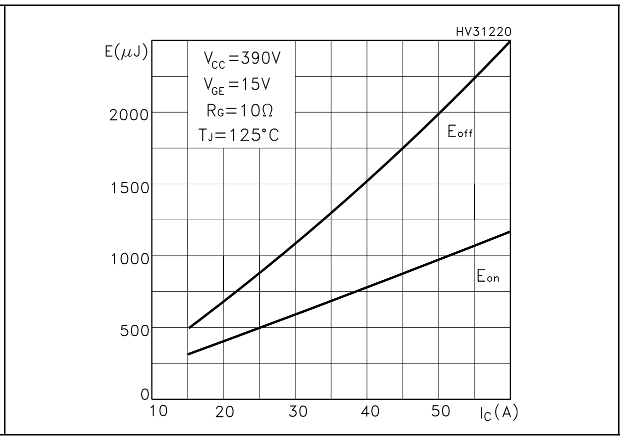


Figure 13. Thermal impedance

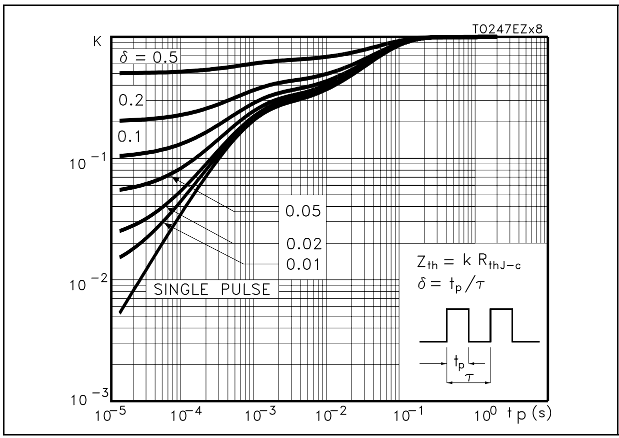
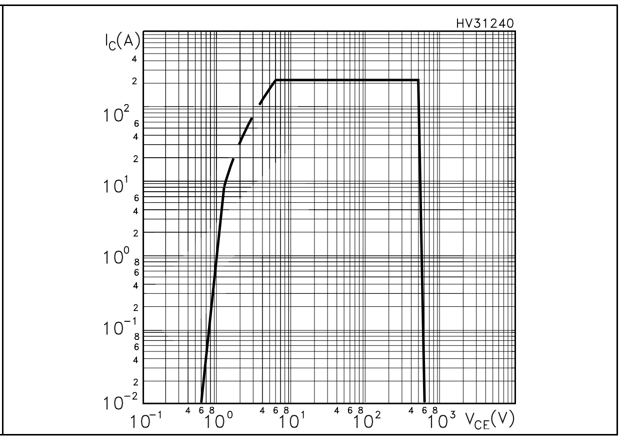


Figure 14. Turn-off SOA



3 Test circuit

Figure 15. Test circuit for inductive load switching

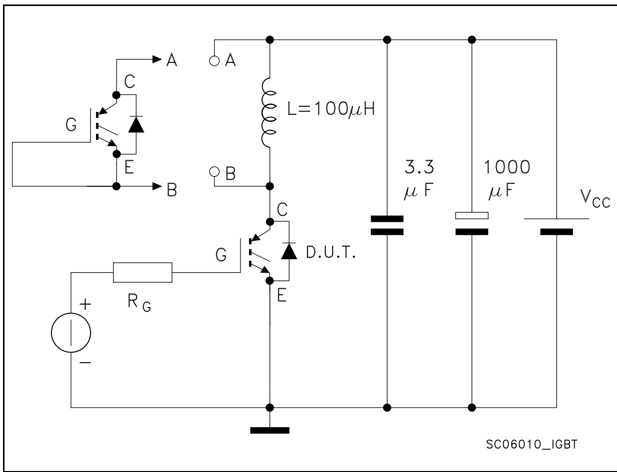


Figure 16. Gate charge test circuit

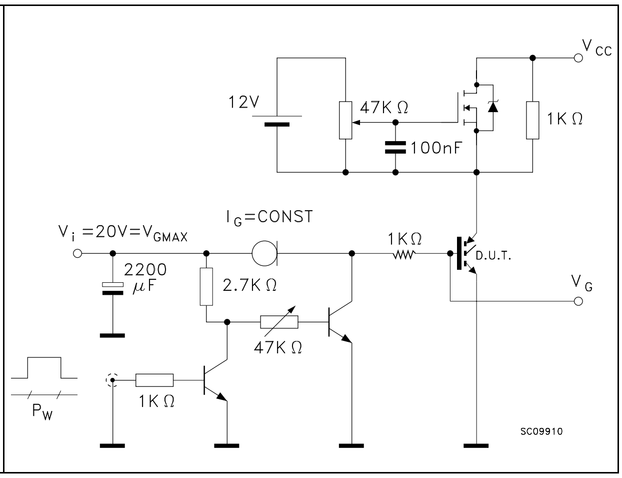


Figure 17. Switching waveforms

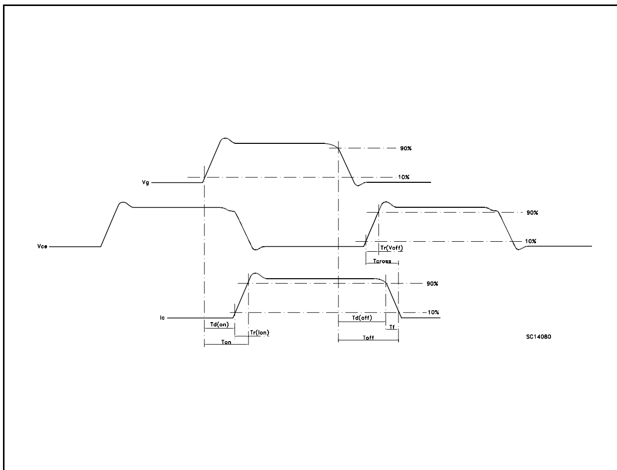
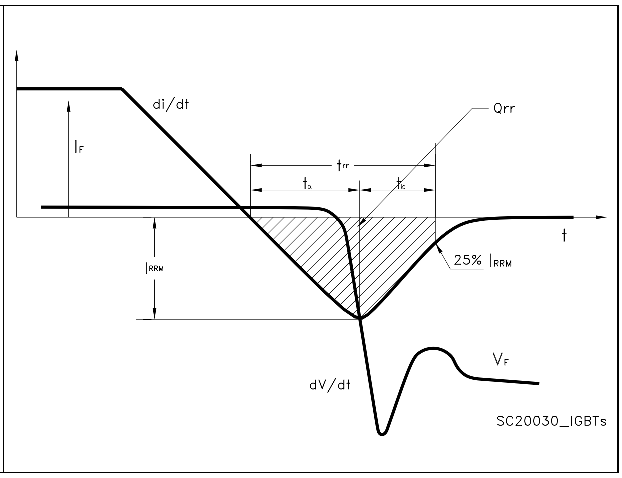


Figure 18. Diode recovery times waveform

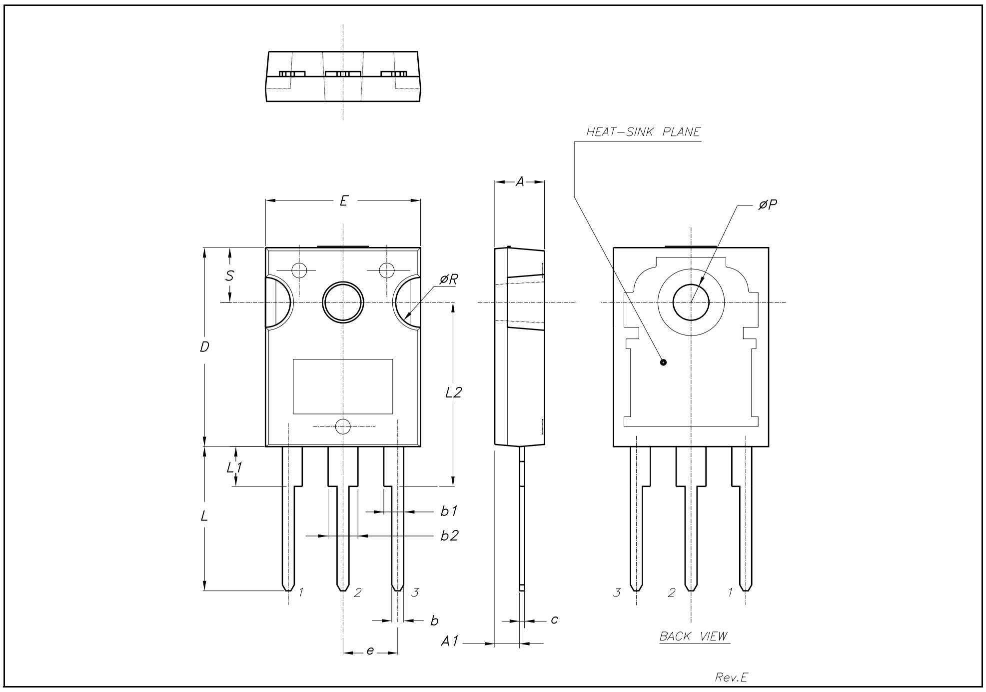


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
17-Nov-2005	1	First release
05-May-2006	2	Inserted curves
10-Jul-2006	3	Modified value on *Absolute maximum ratings*
28-Jul-2006	4	Modified value on *Dynamic*