BOURNS®

TISP4290J3BJ THRU TISP4395J3BJ

BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS

TISP4xxxJ3BJ Overvoltage Protector Series

Ion-Implanted Breakdown Region
-Precise and Stable Voltage
-Low Voltage Overshoot Under Surge

Designed for Transformer Center Tap (Ground Return) Overvoltage Protection
-Enables GR-1089-CORE Compliance
-High Holding Current Allows Protection of Data Lines with d.c. Power Feed

Can be Used to Protect Rugged Modems Designed for Exposed Applications Exceeding TIA-968-A

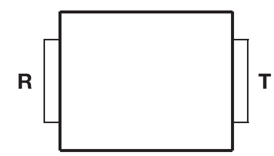
Device Name	V_{DRM} V	$V_{(BO)}$ V
TISP4290J3BJ	220	290
TISP4350J3BJ	275	350
TISP4395J3BJ	320	395

Rated for International Surge Wave Shapes

Wave Shape	Standard	I_{PPSM} A
2/10	GR-1089-CORE	1000
8/20	IEC 61000-4-5	800
10/160	TIA-968-A (FCC Part 68)	400
10/700	ITU-T K.20/21/45	350
10/560	TIA-968-A (FCC Part 68)	250
10/1000	GR-1089-CORE	200

... UL Recognized Components

SMB Package (Top View)



MDXXBGI

Device Symbol

SD4XAp

Description

The range of TISP4xxxJ3BJ devices are designed to limit overvoltages on telecom lines. The TISP4xxxJ3BJ is primarily designed to address GR-1089-CORE compliance on data transmission lines with d.c. power feeding. When overvoltage protection is applied to transformer coupled lines from the transformer center tap to ground, the total ground return current can be 200 A, 10/1000 and 1000 A, 2/10. The high 150 mA holding current is set above common d.c. feed system levels to allow the TISP4xxxJ3BJ to reset following a disturbance.

These devices allow signal voltages, without clipping, up to the maximum off-state voltage value, V_{DRM}, see Figure 1. Voltages above V_{DRM} are limited and will not exceed the breakover voltage, $V_{(BO)}$, level. If sufficient current flows due to the overvoltage, the device switches into a low voltage on-state condition, which diverts the current from the overvoltage through the device. When the diverted current falls below the holding current, I_H, level the devices switches off and restores normal system operation.

How to Order

Device	Package	Carrier	For Standard Termination Finish Order As	For Lead Free Termination Finish Order As	Marking Code	Std. Qty.
TISP4xxxJ3BJ	SMB (DO-214AA)	Embossed Tape Reeled	TISP4xxxJ3BJR	TISP4xxxJ3BJR-S	4xxxJ3	3000

Insert xxx value corresponding to device name.

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex
JULY 2003 - REVISED FEBRUARY 2005

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating		Symbol	Value	Unit
Repetitive peak off-state voltage	'4290 '4350 '4395	V_{DRM}	±220 ±275 ±320	V
Non-repetitive peak on-state pulse current (see Notes 1 and 2) 2/10 (Telcordia GR-1089-CORE, 2/10 voltage wave shape) 8/20 (IEC 61000-4-5, combination wave generator, 1.2/50 voltage wave shape) 10/160 (TIA-968-A (Replaces FCC Part 68), 10/160 voltage wave shape) 4/250 (ITU-T K.20/21, 10/700 voltage wave shape, simultaneous) 5/310 (ITU-T K.20/21, 10/700 voltage wave shape, single) 5/320 (TIA-968-A (Replaces FCC Part 68), 9/720 voltage wave shape, single) 10/560 (TIA-968-A (Replaces FCC Part 68), 10/560 voltage wave shape) 10/1000 (Telcordia GR-1089-CORE, 10/1000 voltage wave shape)		I_{PPSM}	 1000 800 400 370 350 350 250 200	A
Non-repetitive peak on-state current (see Notes 1 and 2) 50 Hz, 1 cycle 60 Hz, 1 cycle		I_{TSM}	 80 100	A
Initial rate of rise of on-state current, Linear current ramp, Maximum ramp value < 50 A		di_T/dt	800	A/µs
Junction temperature		T_J	-40 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTES: 1. Initially, the device must be in thermal equilibrium with T_J = 25 °C.
2. These non-repetitive rated currents are peak values of either polarity. The surge may be repeated after the device returns to its initial conditions.

Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = \pm V_{DRM}$	T_A = 25 °C T_A = 85 °C			±5 ±10	µA
$V_{(BO)}$	AC breakover voltage	dv/dt = ±250 V/ms, R_{SOURCE} = 300	'4290 '4350 '4395			±290 ±350 ±395	V
$V_{(BO)}$	Ramp breakover voltage	dv/dt ≤ ±1000 V/µs, Linear voltage ramp, Maximum ramp value = ±500 V di/dt = ±20 A/µs, Linear current ramp, Maximum ramp value = ±10 A	'4290 '4350 '4395			±303 ±364 ±409	V
$V_{(BO)}$	Impulse breakover voltage	2/10 wave shape, I_{PP} = ±1000 A, R_S = 2.5 Ω, (see Note 3)	'4290 '4350 '4395		±320 ±386 ±434		V
$I_{(BO)}$	Breakover current	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω				±600	mA
I_H	Holding current	I_T = ±5 A, di/dt = +/-30 mA/ms		±150			mA
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85 V_{DRM}		±5			kV/µs

Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
I_D	Off-state current	V_D = ±50 V T_A = 85 °C			±10	μA
C_{off}	Off-state capacitance	f = 1 MHz, Vd = 1 V rms, V_D = 0		105	125	pF
		f = 1 MHz, Vd = 1 V rms, V_D = -1 V		95	115	
		f = 1 MHz, Vd = 1 V rms, V_D = -2 V		90	105	
		f = 1 MHz, Vd = 1 V rms, V_D = -50 V		42	50	
		f = 1 MHz, Vd = 1 V rms, V_D = -100 V		35	40	

NOTE 3: Dynamic voltage measurements should be made with an oscilloscope with limited band width (20 MHz) to avoid high frequency noise.

Thermal Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to free air thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C, (see Note 4)			90	°C/W

NOTE 4: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

Parameter Measurement Information

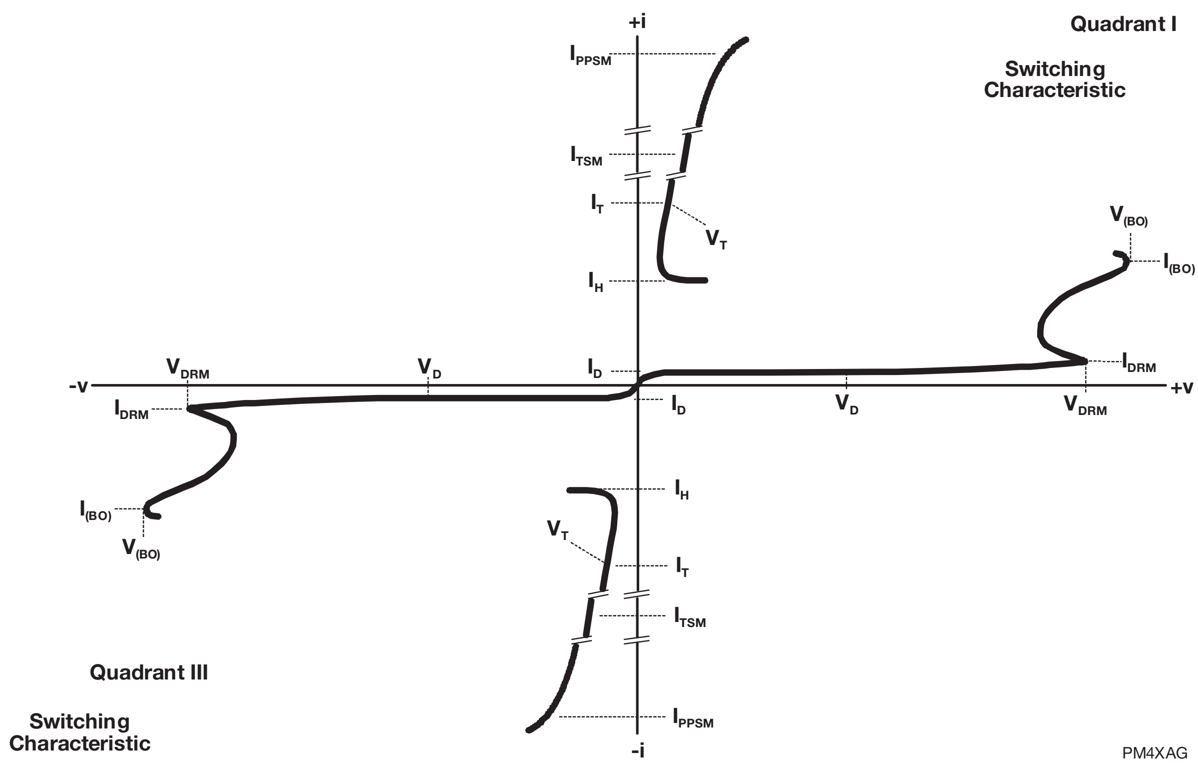


Figure 1. Voltage-Current Characteristic for Terminals T and R
All Measurements are Referenced to Terminal T

Typical Characteristics

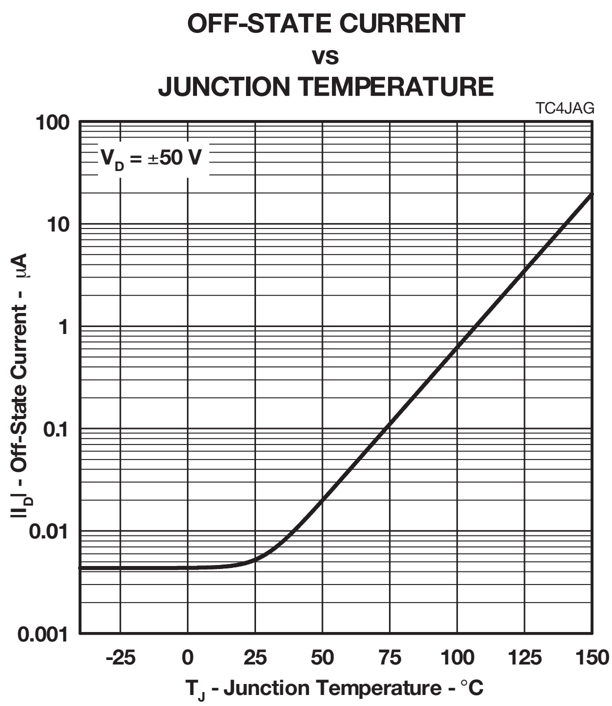


Figure 2.

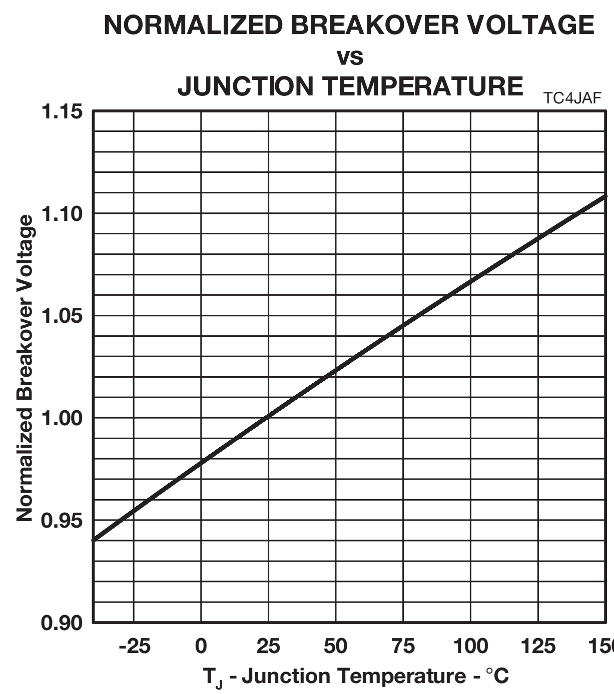


Figure 3.

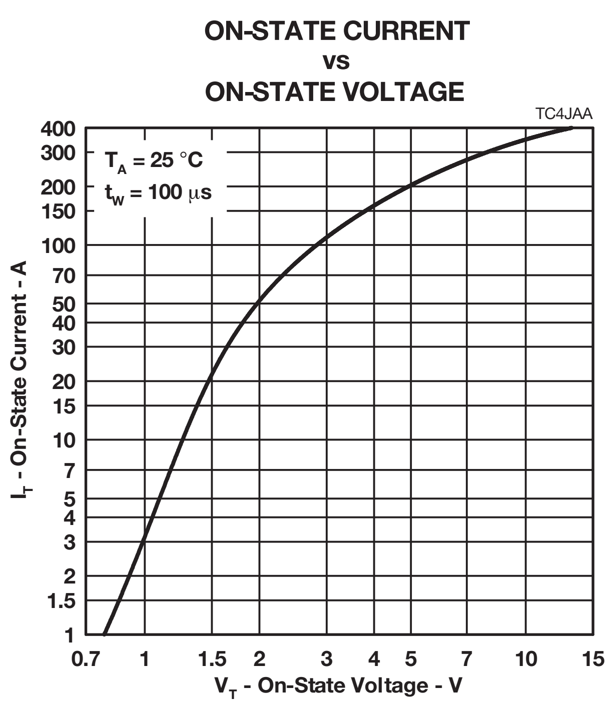


Figure 4.

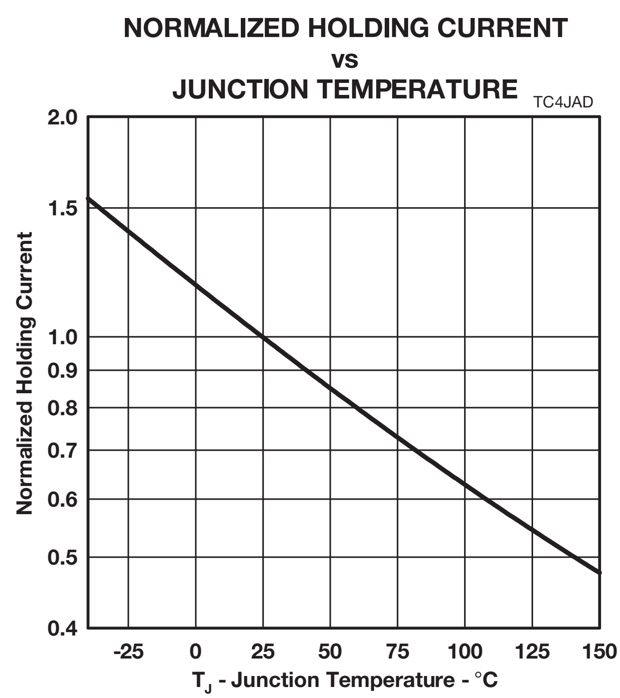


Figure 5.

Typical Characteristics

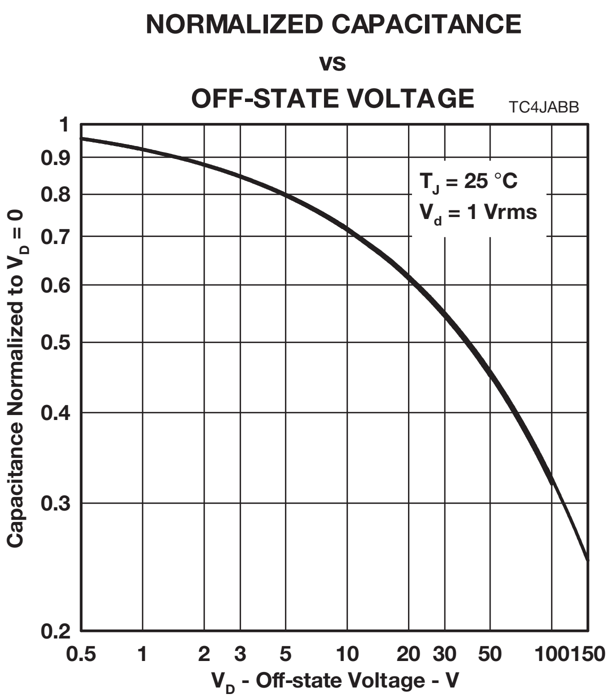


Figure 6.

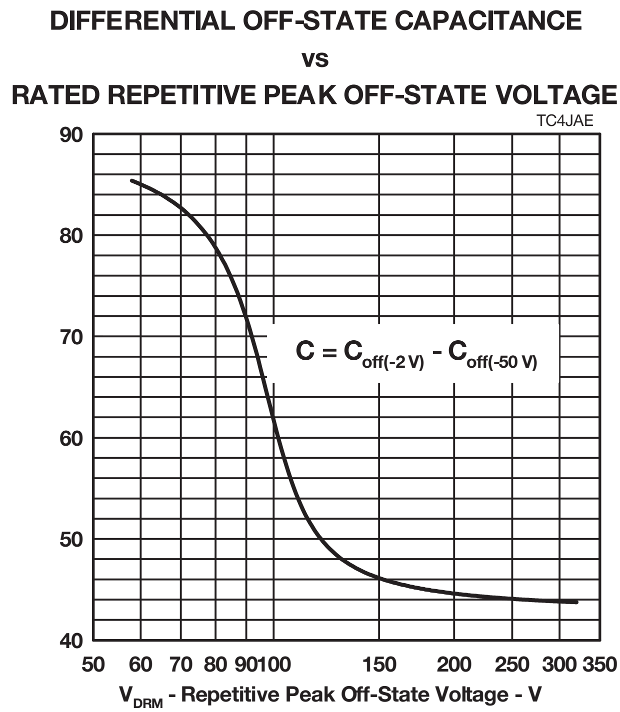


Figure 7.

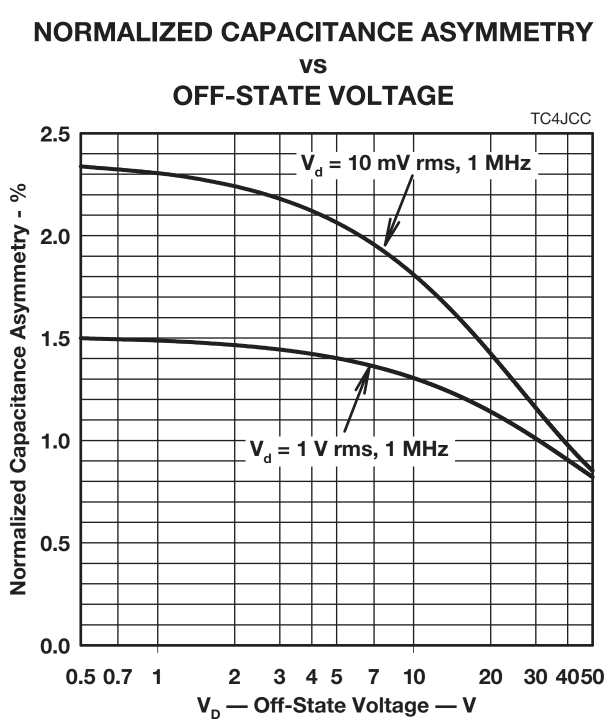


Figure 8.

Rating and Thermal Characteristics

NON-REPETITIVE PEAK ON-STATE CURRENT vs CURRENT DURATION

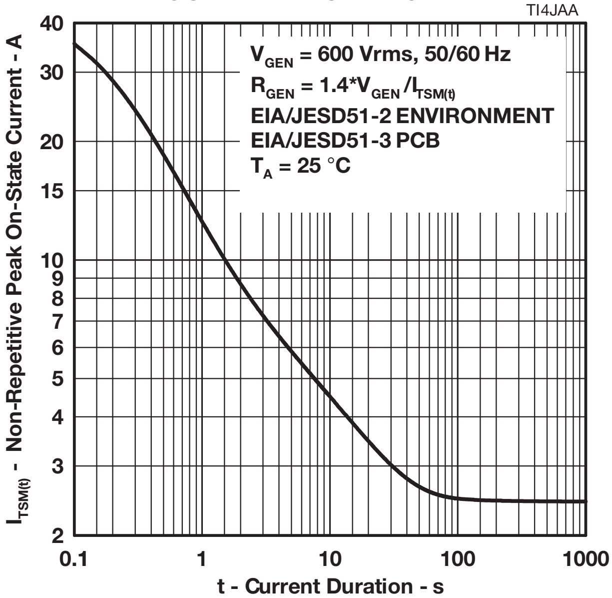


Figure 9.

V_{DRM} DERATING FACTOR vs MINIMUM AMBIENT TEMPERATURE

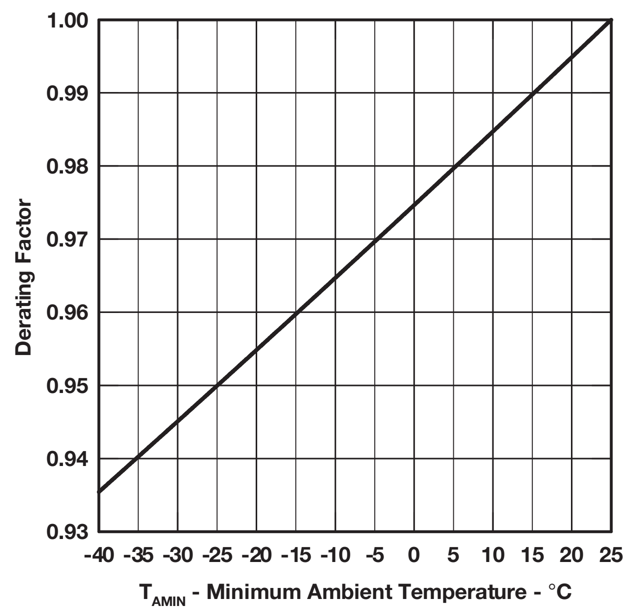


Figure 10.

Applications Circuits