

NON-ISOLATED DC/DC CONVERTERS

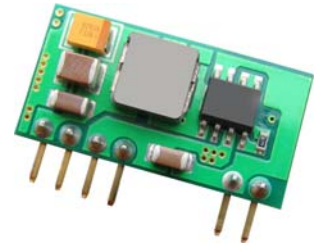
2.4 V - 5.5 V Input 0.75 V - 3.63 V/6 A Output

bel
POWER PRODUCTS

VRBA-06F2Ax Series

RoHS Compliant

- Non-Isolated
- High Efficiency
- High Power Density
- Fixed Frequency (300 kHz)
- Flexible Output Voltage Sequencing
- Under-voltage Lockout (UVLO)
- Wide Trim
- OCP/SCP
- Remote On/Off
- Active Low/High (option)
- Able to Sink & Source Current



Description

The Bel VRBA-06F2Ax modules are a series of non-isolated dc/dc converters that deliver up to 6A of output current with full load efficiency of 93% at 3.3 V output. These modules provide precisely regulated voltage programmable via external resistor from 0.75 V to 3.63 V over a wide range of input voltage (2.4 V-5.5 V). These modules have a sequencing feature that enables designers to implement various types of output voltage sequencing when powering multiple voltages on a board. The open-frame construction and small footprint enable designers to develop cost and space-efficient solutions. Standard features include remote On/Off, over current protection, short circuit protection, wide input, and programmable output voltage.

Part Selection

Output Voltage	Input Voltage	Max. Output Current	Max. Output Power	Typical Efficiency	Model Number Active Low	Model Number Active High
0.75 V - 3.63 V ¹	2.4 V - 5.5 V	6 A	21.8 W	93%	VRBA-06F2AL	VRBA-06F2A0

- Notes:** 1. These modules use a buck topology, so the output voltages must be 0.5 V less than the input voltage.
2. Add "G" suffix at the end of the model number to indicate Tray Packaging.

Absolute Maximum Ratings

Parameter	Min	Typ	Max	Notes
Input Voltage (continuous)	-0.3 V	-	5.8 V	
Output Enable Terminal Voltage	-0.3 V	-	5.5 V	
Sequencing Voltage ¹	-0.3 V	-	V _{in}	
Ambient Temperature	-40 °C	-	85 °C	
Storage Temperature	-55 °C	-	125 °C	

- Notes:** All specifications are typical at 25 °C unless otherwise stated.
1. VRBA-06F2Ax series of modules include a sequencing feature that enables users to implement various types of output voltage sequencing in their applications. This is accomplished via an additional sequencing pin. When not used sequencing feature, tie the SEQ pin to V_{in}.

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Input Specifications

Parameter	Min	Typ	Max	Notes
Input Voltage				
Vo ≤ 1.5 V	2.4 V	-	5.5 V	
Vo = 1.8 V	3.0 V	-	5.5 V	
2.5 V ≤ Vo ≤ 3.3 V	4.5 V	-	5.5 V	
Input Current (full load)				
Vo = 3.3V	-	-	4.73 A	
Vo = 2.5V	-	-	3.66 A	
Vo = 1.8V	-	-	4.09 A	
Vo = 1.5V	-	-	4.31 A	
Vo = 1.2V	-	-	3.57 A	
Vo = 0.75V	-	-	2.40 A	
Input Current (no load)				
Vo = 3.3 V	-	50 mA	-	
Vo = 0.75 V	-	25 mA	-	
Remote Off Input Current	-	0.6 mA	-	
Input Reflected Ripple Current (pk-pk)	-	120 mA	-	Tested with simulated source impedance of 1 uH, 5 Hz to 20 MHz, one 1000 uF/25 V AL capacitor and two 100 uF/ 10 V Tantalum capacitor at the input.
Input Reflected Ripple Current (rms)	-	35 mA	-	
I ² t Inrush Current Transient	-	-	0.04 A ² s	
Turn-on Voltage Threshold	-	2.05 V	2.4 V	
Turn-off Voltage Threshold	1.8 V	2.0 V	-	

Output Specifications

Parameter	Min	Typ	Max	Notes	
Output Voltage Set Point	-2% Vo,set	-	2% Vo,set	Vin=5 V, 50% full load	
Output Voltage Set Point	-3% Vo,set	-	3% Vo,set	Over all operating input voltages, resistive loads and temperature conditions	
Adjustment Range Selected by External Resistor or Voltage	0.7525 V	-	3.63 V		
Load Regulation	-	0.4% Vo,set	-	Io=Iomin to 50%Iomax to 100%Iomax	
Line Regulation	-	0.3% Vo,set	-	Vin=Vinmin to 50%Vinmax to 100%Vinmax	
Regulation Over Temperature (-40 °C to +85 °C)	-	0.4% Vo,set	-	Tref=Tamin to Tamax	
Output Current	0 A	-	6 A		
Current Limit Threshold	9 A	-	18 A		
Short Circuit Surge Transient	-	0.32 A ² s	-		
Ripple and Noise (pk-pk)	-	40 mV	70 mV	Tested with 0-20 MHz, with 10 uF Tantalum capacitor & 1 uF/10 V ceramic capacitor at the output.	
Ripple and Noise (rms)	-	10 mV	30 mV		
Turn on Time	-	6 mS	10 mS		
Overshoot at Turn on	-	-	3%		
Output Capacitance					
Min ESR ≥ 1mohm	0 uF	-	1000 uF		
Max ESR ≥ 10mohm	0 uF	-	3000 uF		
Transient Response					
50% ~ 100% Max Load	Vo = 0.75 V - 3.63 V	-	130 mV	-	di/dt=2.5 A/uS; Vin=5 V; and with 10 uF Tantalum capacitor & 1 uF/10 V TDK ceramic capacitor at the output
Settling Time		-	25 uS	-	
100% ~ 50% Max Load		-	130 mV	-	
Settling Time		-	25 uS	-	

Note: All specifications are typical at nominal input, full load at 25 °C unless otherwise stated.

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General Specifications

Parameter	Min	Typ	Max	Notes
Efficiency				Measured at Vin=5 V, full load
Vo=3.3 V	-	93%	-	
Vo=2.5 V	-	91%	-	
Vo=1.8 V	-	88%	-	
Vo=1.5 V	-	87%	-	
Vo=1.2 V	-	84%	-	
Vo=0.75 V	-	78%	-	
Switching Frequency	250 kHz	300 kHz	350 kHz	
Over Temperature Shutdown	-	135 °C	-	
Output Voltage Trim Range	0.7525 V	-	3.63 V	
MTBF	7,142,646 hours			Calculated Per Bell Core SR-332 (Vin=5 V; Vo=0.75 V; Io = 4.8 A; Ta = 25°C)
Dimensions				
Inches (L x W x H)	1.0 x 0.5 x 0.243			
Millimeters (L x W x H)	25.4 x 12.7 x 6.16			
Weight	-	5 g	-	

Note: All specifications are typical at 25 °C unless otherwise stated.

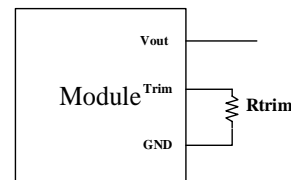
Control Specifications

Parameter	Min	Typ	Max	Notes
Remote On/Off				
Signal Low (Unit Off)	-0.2 V	-	0.3 V	VRBA-06F2A0; Remote On/Off pin open, Unit on.
Signal High (Unit On)	-	-	Vin, max	
Signal Low (Unit On)	-0.2 V	-	0.3 V	VRBA-06F2AL; Remote On/Off pin open, Unit on.
Signal High (Unit Off)	1.5 V	-	Vin, max	
Sequencing Voltage	0 V	-	Vin	Sequencing Voltage applied on SEQ pin should be higher than output voltage.
Sequencing Slew Rate Capability	-	-	2 V/mS	
Sequencing Delay Time	10 mS	-	-	Delay from Vin, min to application of voltage on SEQ pin
Tracking Accuracy				
Power-Up	-	100 mV	200 mV	
Power-Down	-	200 mV	400 mV	

Output Trim Equations

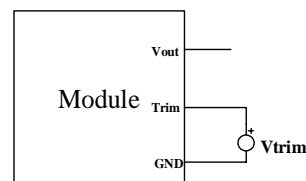
Equation for calculating the trim resistor (in kΩ) given the desired adjusted voltage (Vadj) is shown below. The Trim Up resistor should be connected between the Trim pin and Ground.

$$R_{trim} = \frac{21.07}{V_{adj} - 0.7525} - 5.11$$



Equation for calculating the trim voltage (in V) given the desired adjusted voltage (Vadj) is shown below. The Trim Up voltage should be connected between the Trim pin and Ground.

$$V_{trim} = 0.7 - 0.1698 \times (V_{adj} - 0.7525)$$

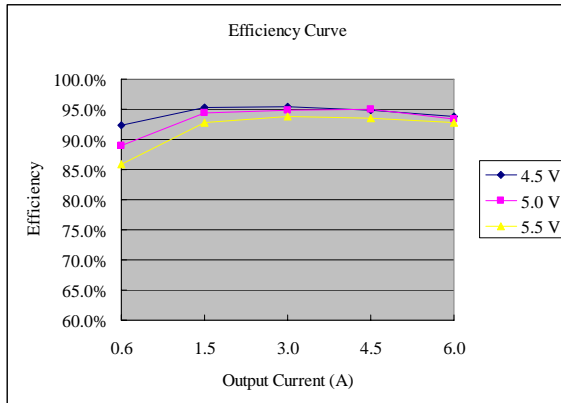


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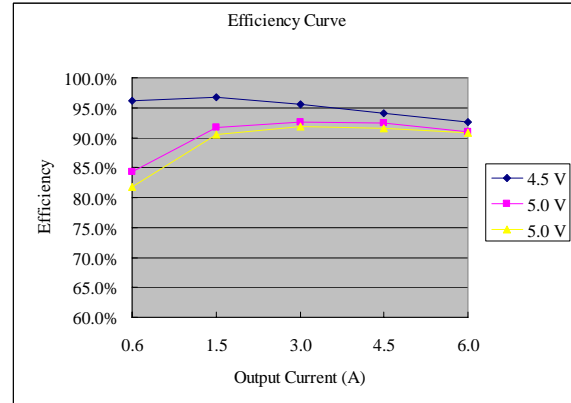
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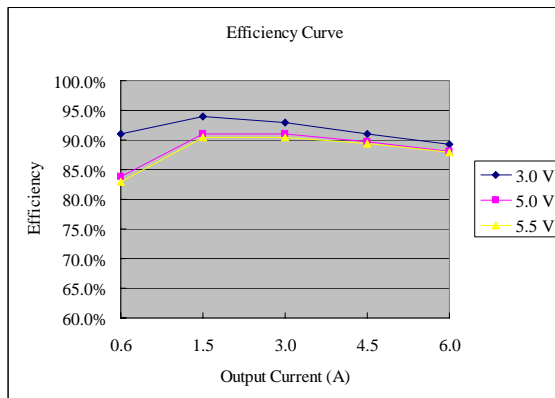
Efficiency Data



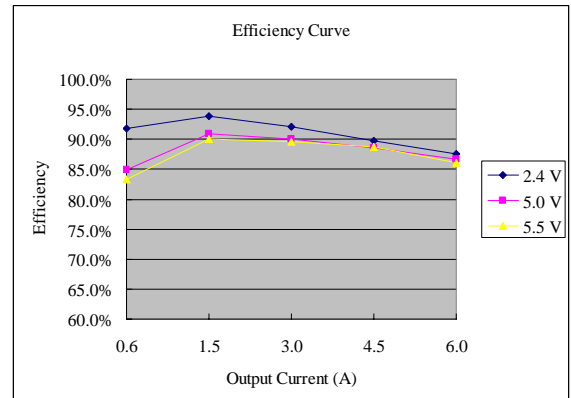
$V_o=3.3\text{ V}$



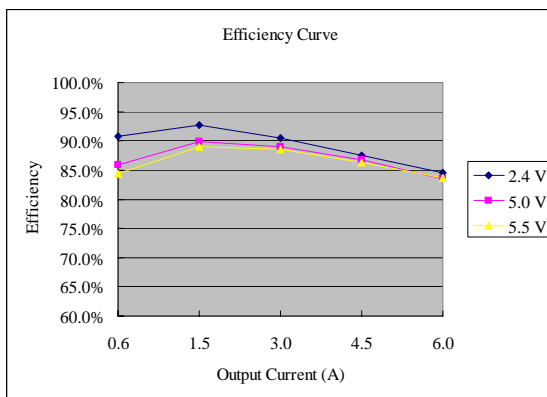
$V_o=2.5\text{ V}$



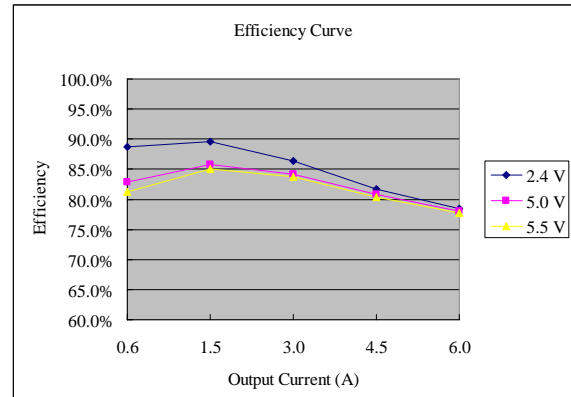
$V_o=1.8\text{ V}$



$V_o=1.5\text{ V}$



$V_o=1.2\text{ V}$



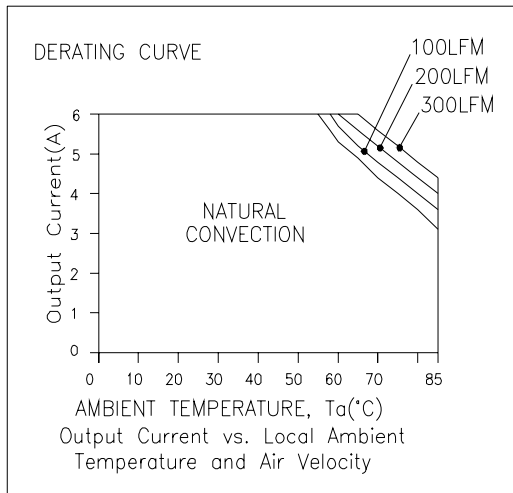
$V_o=0.7525\text{ V}$

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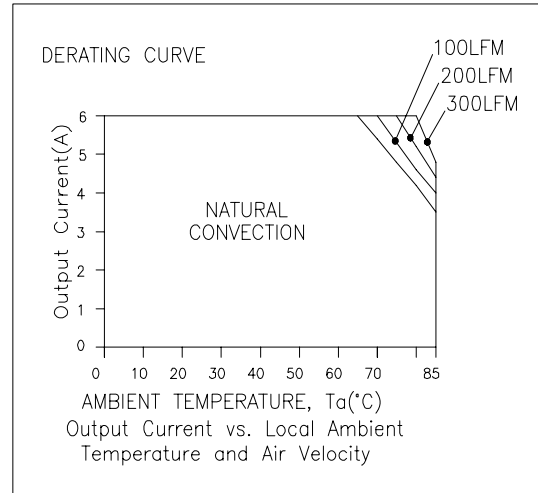
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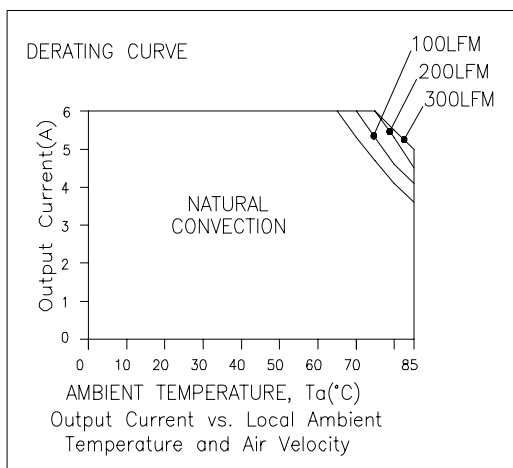
Thermal Derating Curves



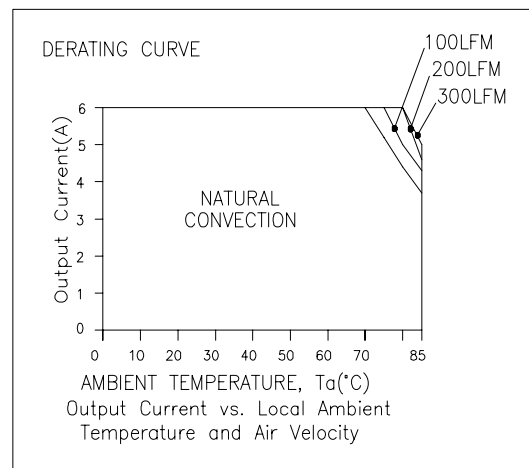
Vin=5 V, Vo = 3.3 V



Vin=5 V, Vo = 0.75 V



Vin=4.5 V, Vo = 2.5 V



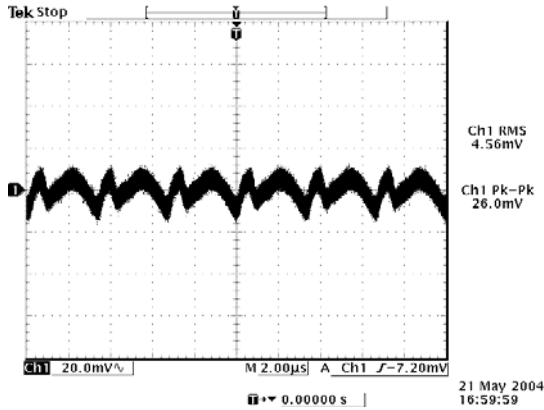
Vin=3.3 V, Vo = 0.75 V

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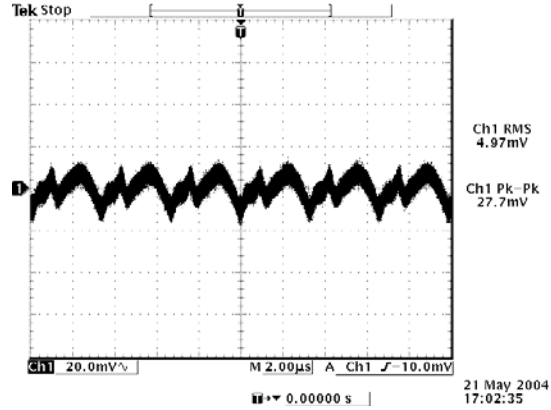
2.4 V - 5.5 V Input 0.75 V - 3.63 V/6 A Output



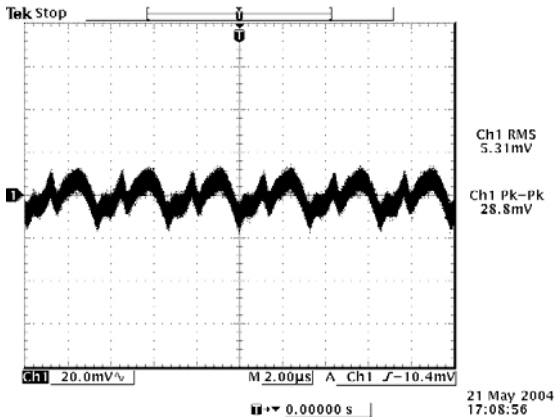
Ripple and Noise Waveforms



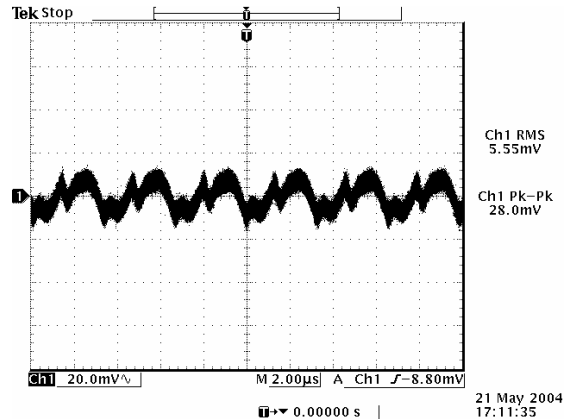
Ripple and noise at full load, $V_{in}=5.0$ V, $V_o=0.7525$ V



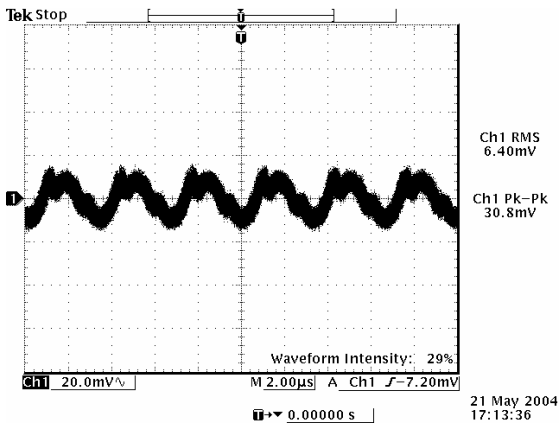
Ripple and noise at full load, $V_{in}=5.0$ V, $V_o=1.2$ V



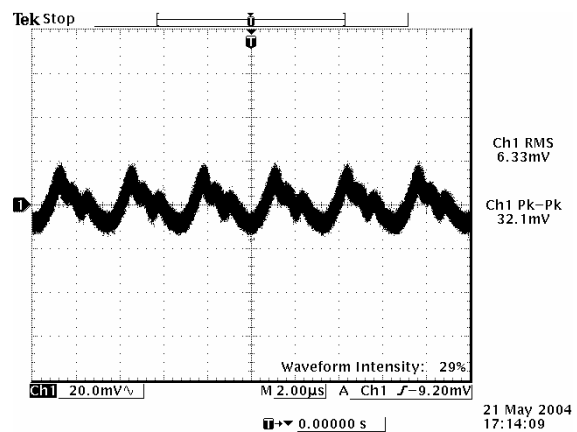
Ripple and noise at full load, $V_{in}=5.0$ V, $V_o=1.5$ V



Ripple and noise at full load, $V_{in}=5.0$ V, $V_o=1.8$ V



Ripple and noise at full load, $V_{in}=5.0$ V, $V_o=2.5$ V



Ripple and noise at full load, $V_{in}=5.0$ V, $V_o=3.3$ V

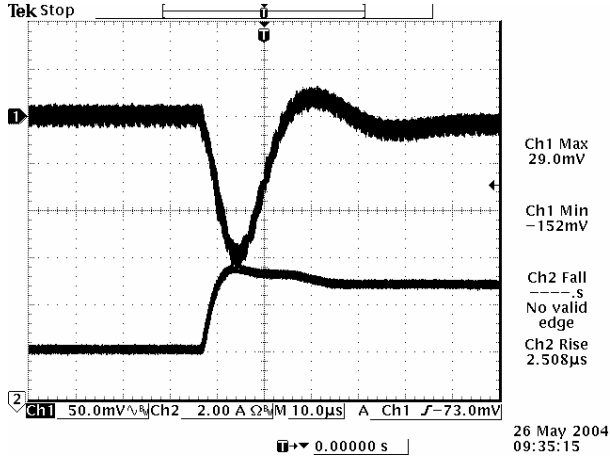
Note: Ripple and noise is tested at 0-20 MHz BW, 10 μ F/10 V tantalum capacitor and 1 μ F/10 V ceramic capacitor, $T_a=25$ deg C.

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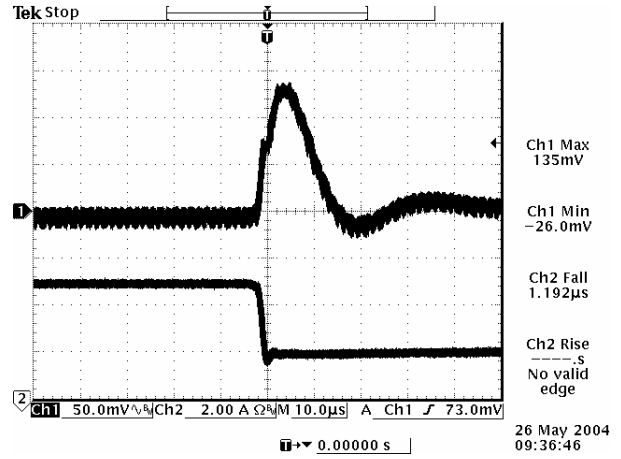
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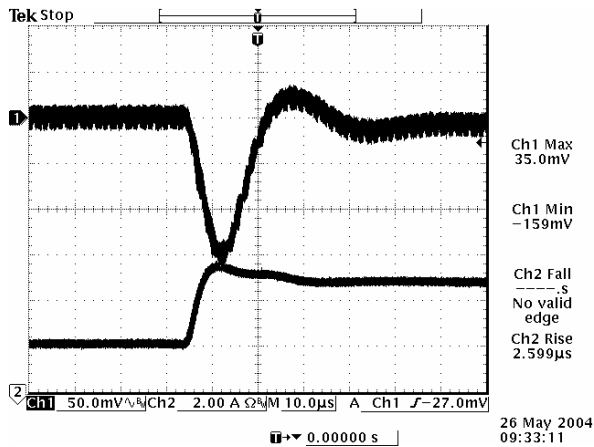
Transient Response Waveforms



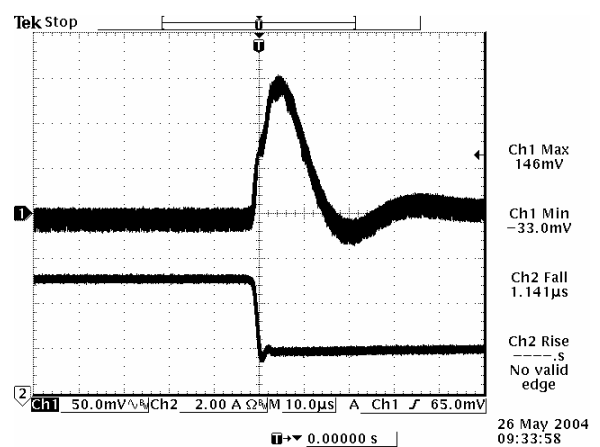
50% to 100% load step at $V_{in}=5\text{ V}$, $V_o=0.75\text{ V}$



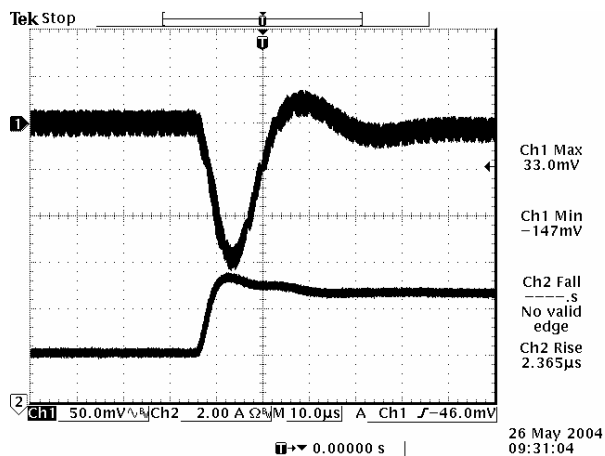
100% to 50% load step at $V_{in}=5\text{ V}$, $V_o=0.75\text{ V}$



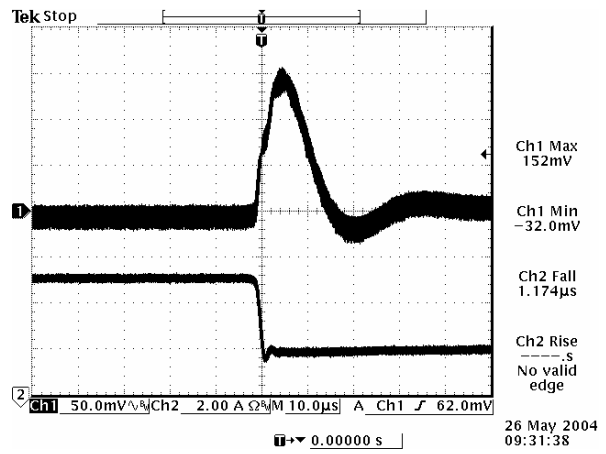
50% to 100% load step at $V_{in}=5\text{ V}$, $V_o=1.2\text{ V}$



100% to 50% load step at $V_{in}=5\text{ V}$, $V_o=1.2\text{ V}$



50% to 100% load step at $V_{in}=5\text{ V}$, $V_o=1.5\text{ V}$



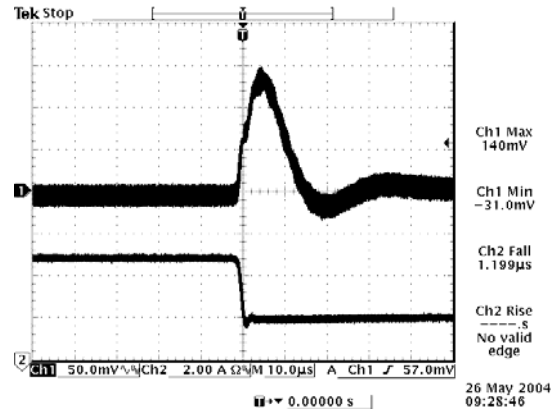
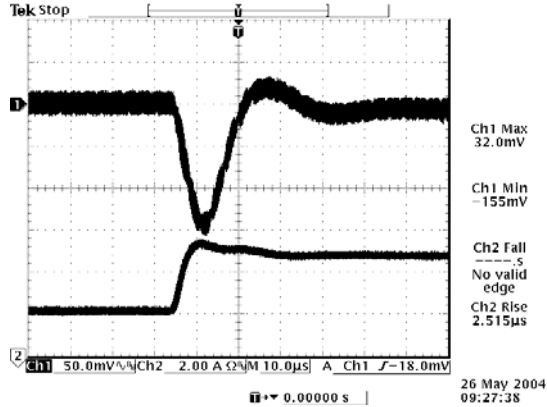
100% to 50% load step at $V_{in}=5\text{ V}$, $V_o=1.5\text{ V}$

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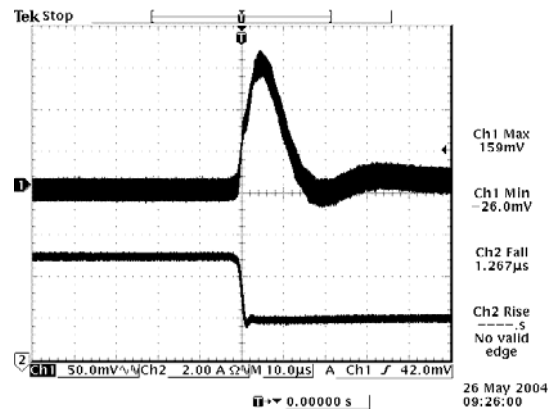
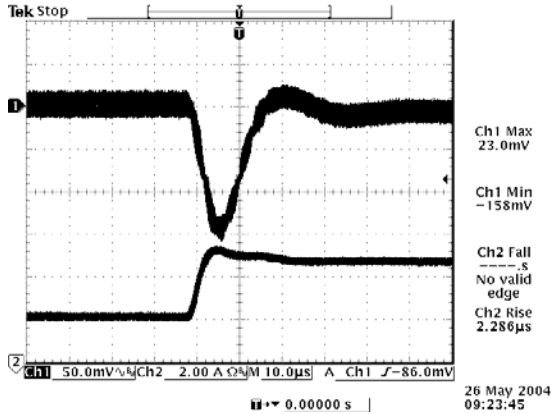


Transient Response Waveforms (continued)



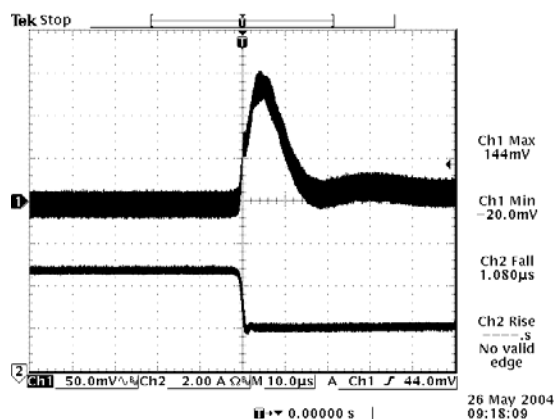
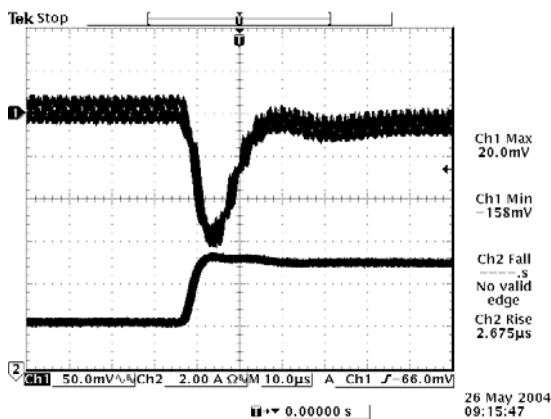
50% to 100% load step at $V_{in}=5\text{ V}$, $V_o=1.8\text{ V}$

100% to 50% load step at $V_{in}=5\text{ V}$, $V_o=1.8\text{ V}$



50% to 100% load step at $V_{in}=5\text{ V}$, $V_o=2.5\text{ V}$

100% to 50% load step at $V_{in}=5\text{ V}$, $V_o=2.5\text{ V}$



50% to 100% load step at $V_{in}=5\text{ V}$, $V_o=3.3\text{ V}$

100% to 50% load step at $V_{in}=5\text{ V}$, $V_o=3.3\text{ V}$

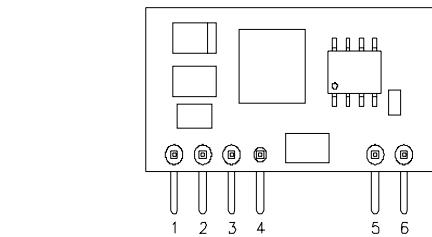
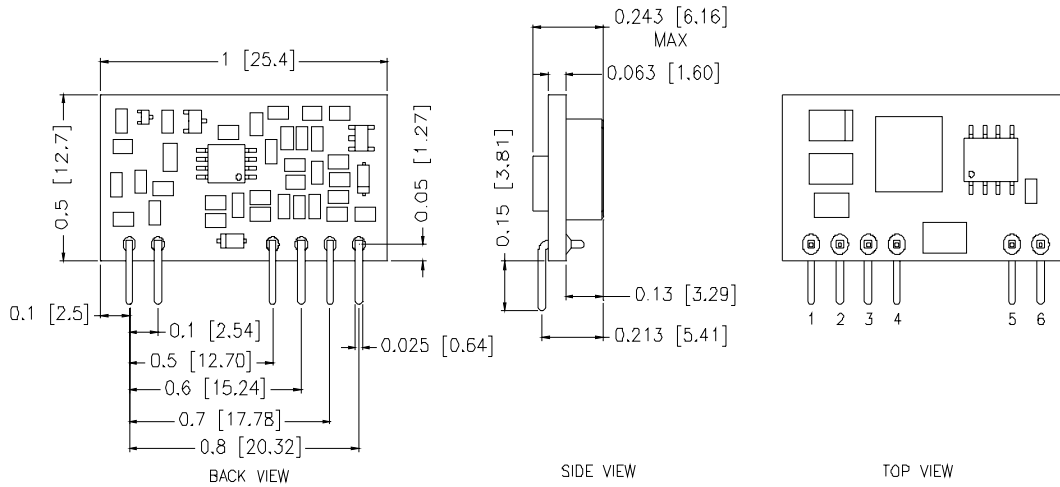
Note: Transient response is tested at $di/dt=2.5\text{ A}/\mu\text{S}$, with $10\text{ }\mu\text{F}/10\text{ V}$ tantalum capacitor and $1\text{ }\mu\text{F}/10\text{ V}$ ceramic capacitor, $T_a=25\text{ deg C}$.

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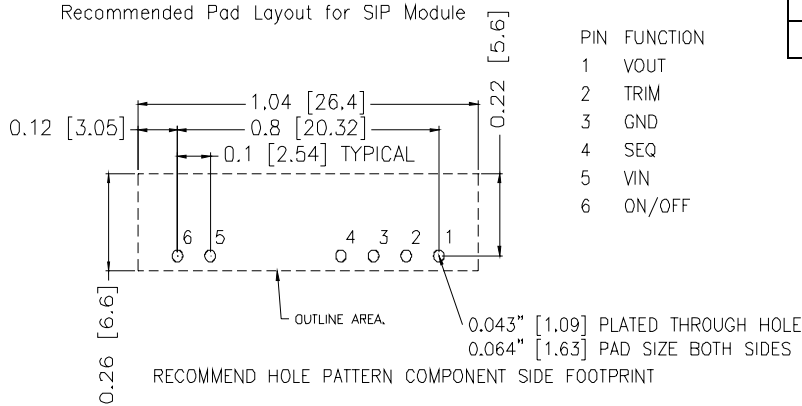
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Mechanical Outline



Recommended Pad Layout for SIP Module



PIN	FUNCTION
1	VOUT
2	TRIM
3	GND
4	SEQ
5	VIN
6	ON/OFF

Pin Connections

Pin	Function
1	Vout
2	Trim
3	Ground
4	SEQ
5	Vin
6	Remote On/Off

RoHS Compliance

Complies with the European Directive 2002/95/EC, calling for the elimination of lead and other hazardous substances from electronic products.



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CORPORATE

Bel Fuse Inc.
206 Van Vorst Street
Jersey City, NJ 07302
Tel 201-432-0463
Fax 201-432-9542
www.belfuse.com

FAR EAST

Bel Fuse Ltd.
8F/ 8 Luk Hop Street
San Po Kong
Kowloon, Hong Kong
Tel 852-2328-5515
Fax 852-2352-3706
www.belfuse.com

EUROPE

Bel Fuse Europe Ltd.
Preston Technology Management Centre
Marsh Lane, Suite G7, Preston
Lancashire, PR1 8UD, U.K.
Tel 44-1772-556601
Fax 44-1772-888366
www.belfuse.com