PRELIMINARY DATA SHEET

AP147-320: ISM 900 MHz Band 2-Watt InGaP HBT Power Amplifier

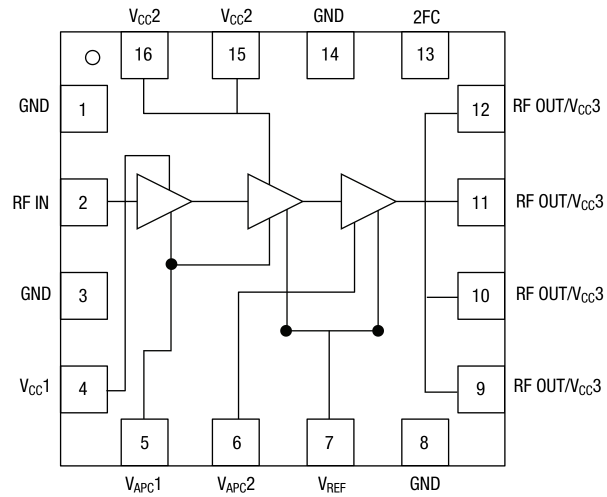
Features

- 902–928 MHz operation
- Output power greater than 33 dBm
- 3.2 V nominal operating voltage
- Integrated analog power control voltage, V_{APC} = 0.1–2.8 V
- High PAE of 50% at maximum output power
- Ultrasmall, thermally enhanced micro lead frame package.
- Low current in standby mode of < 10 μA
- Available on tape and reel

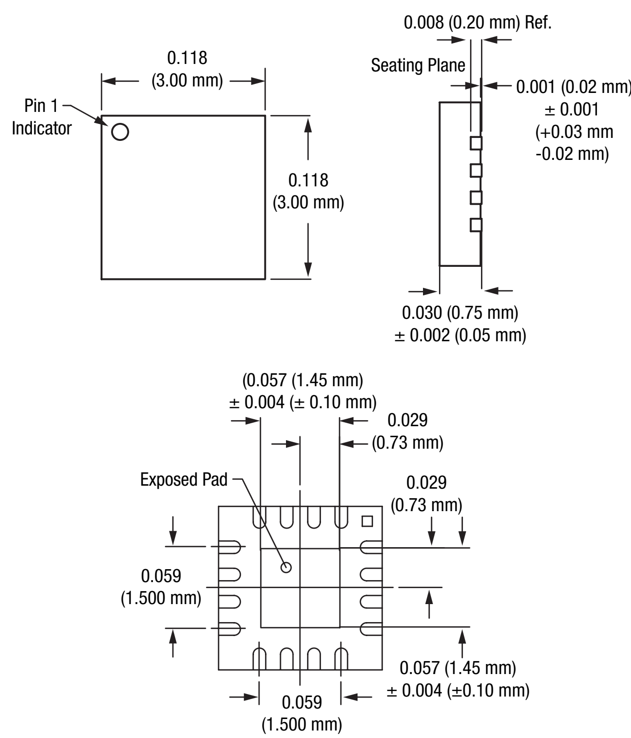
Description

The AP147-320 is a high-performance 3-stage, high-power amplifier IC designed for use in 900 MHz ISM band applications such as automatic meter readers and RFID. It has an integrated analog power control voltage for achieving the desired output power levels. The IC is manufactured on an advanced InGaP HBT process. The AP147-320 is packaged in a thermally enhanced, ultrasmall, micro lead frame package.

Block Diagram



Package Dimensions



Pin Assignments

Pin	Symbol	Description
1, 3, 8, 14	GND	Equipotential point. Connect to the printed circuit board common via the lowest possible impedance.
2	RF IN	RF input to the amplifier
4	$V_{CC}1$	DC power supply voltage input to the first amplifier stage
5	$V_{APC}1$	Power control voltage input to the first and second amplifier stages
6	$V_{APC}2$	Power control voltage input to the final amplifier stage
9, 10, 11, 12	RF OUT/$V_{CC}3$	RF output port and DC power supply voltage input to the final amplifier stage. These pins should be connected together directly at the pins for DC current sharing.
13	2_{FC}	(Optional) Harmonic trap. Connect a series resonant circuit at the second harmonic of the RF input signal to reduce second harmonic power at the RF output.
15, 16	$V_{CC}1$	DC power supply voltage input to the second amplifier stage. These pins should be connected together directly at the pins for DC current sharing.
Exposed Pad		Connect to the printed circuit board common via the lowest possible electrical and thermal impedance.

Absolute Maximum Ratings

Characteristic	Value
Supply voltage (V_{CC} & V_{REF})	6.0 V
Power control voltage ($V_{APC}1$ & $V_{APC}2$)	4.2 V
RF input power	15 dBm
Operating temperature	-40 °C to +85 °C
Storage temperature	-65 °C to +85 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

CAUTION: *Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.*

General DC Electrical Specifications

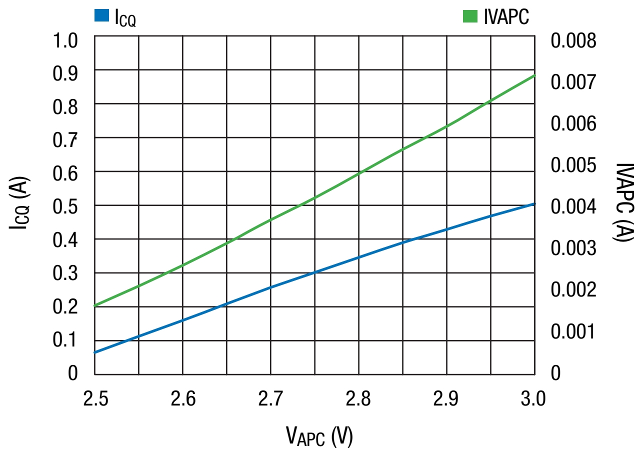
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}		2.7	3.2	4.2	V
Power control voltage	V_{APC}		0.1	2.6	2.8	V
Power control current	IVAPC				5	mA
Leakage current	S_{21}	P_{IN} < -30 dBm, $V_{APC}1$, 2 = 0.1 V			10	µA

General RF Transmit Electrical Specifications

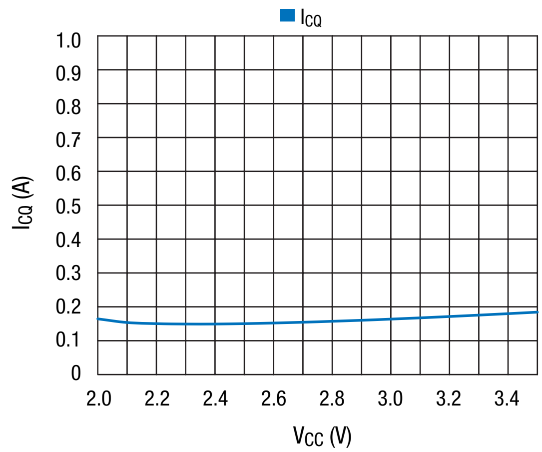
Conditions: V_{CC} = 3.2 V, V_{REF} = 3.2 V, V_{APC} = 2.6 V, T_A = 25 °C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F		900		928	MHz
Gain	S_{21}	Small signal		31.6		dB
Gain variation over frequency	ΔS_{21}	Small signal		0.26		dB
Input return loss	S_{11}	Small signal		-14.7		dB
Output return loss	S_{22}	Small signal		-5.7		dB
Quiescent current	I_{CQ}	(No RF signal)		0.16		A
Output $P_{1\ dB}$	$P_{1\ dB}$	CW		33.1		dBm
Current consumption	I_{CC}	Output $P_{1\ dB}$		1.3		A
Power added efficiency	PAE	Output $P_{1\ dB}$		50%		%
Second harmonic	F_2	Output P1dB		-55		dBc
Third harmonic	F_3	Output P1dB		-66		dBc
Ruggedness		Output VSWR = 10:1, All phase angles, V_{CC} = 4.2 V, P_{IN} = 10 dBm, V_{APC} = 2.6 V	No module damage or permanent performance degradation			
Stability		Output VSWR = 10:1, All phase angles, V_{CC} = 4.2 V, P_{IN} = 10 dBm, V_{APC} = 2.6 V		-36		dBm

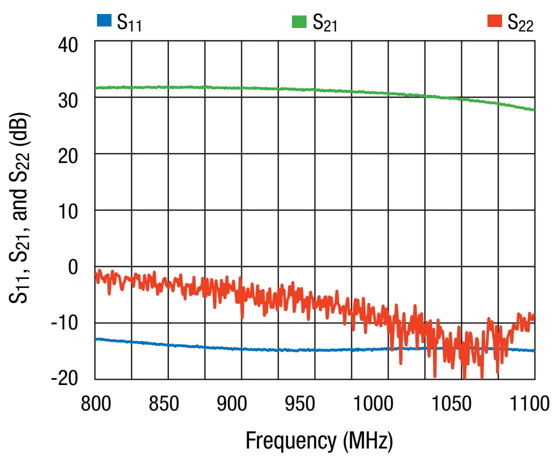
Typical Performance Data



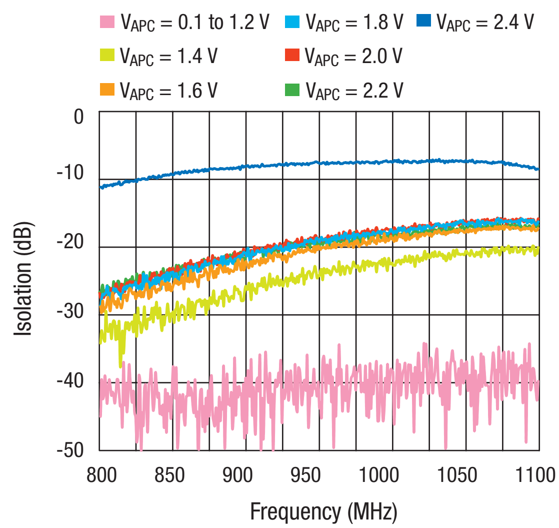
I_{CQ} and IVAPC vs. V_{APC}
Conditions: V_{CC} = 3.2 V, V_{REF} = 3.2 V, T_A = 25 °C



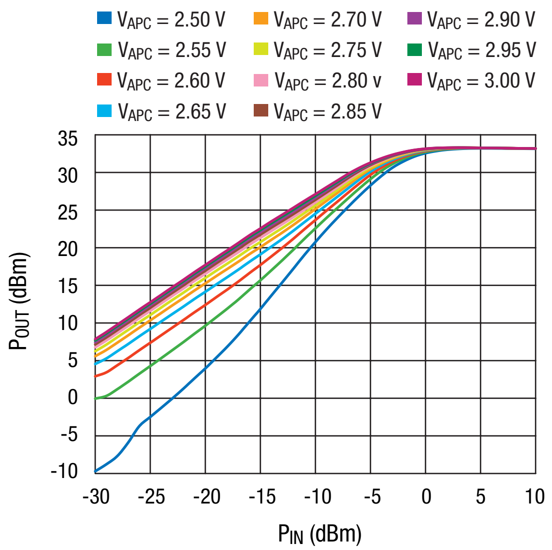
I_{CQ} vs. V_{CC}
Conditions: V_{APC} = 3.2 V, V_{REF} = 3.2 V, T_A = 25 °C



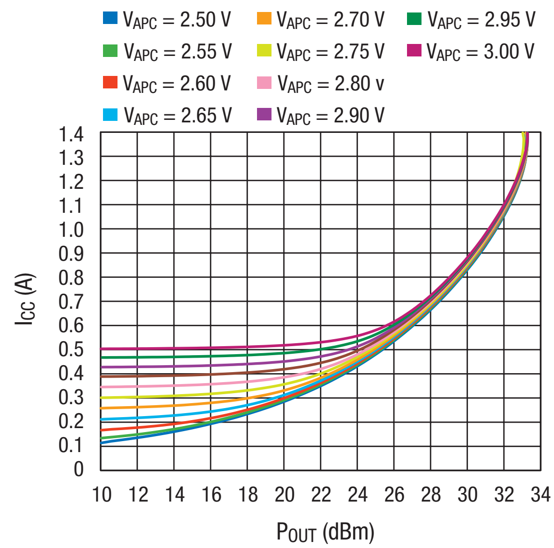
Small Signal Parameters
Conditions: V_{CC} = 3.2 V, V_{REF} = 3.2 V,
V_{APC} = 2.6 V, T_A = 25 °C



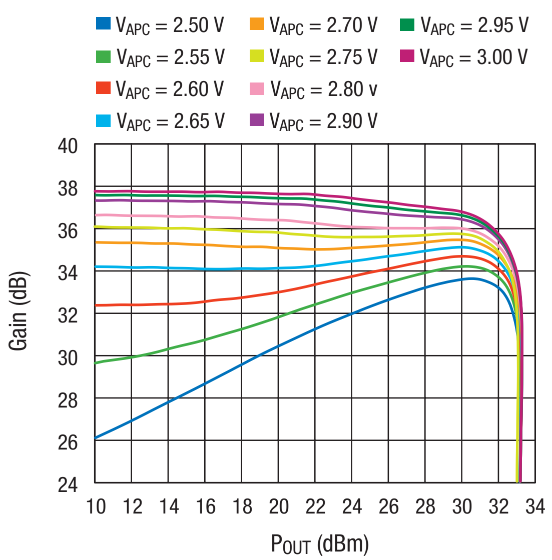
Forward Isolation
Conditions: V_{CC} = 3.2 V, V_{REF} = 3.2 V, T_A = 25 °C



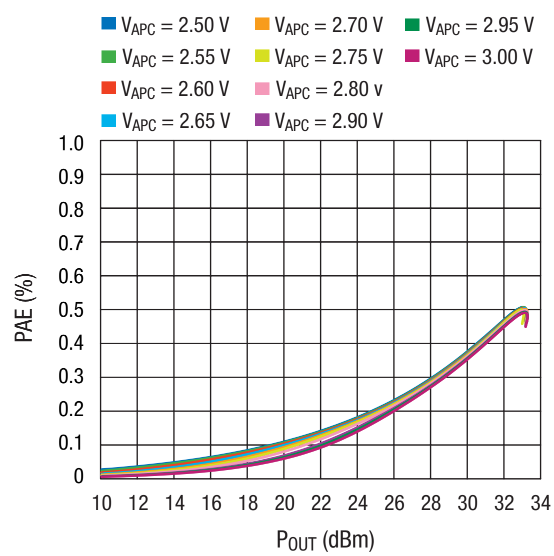
P_{IN} vs. P_{OUT} at V_{APC}
Conditions: CW, V_{CC} = 3.2 V, V_{REF} = 3.2 V,
F_C = 915 MHz, T_A = 25 °C



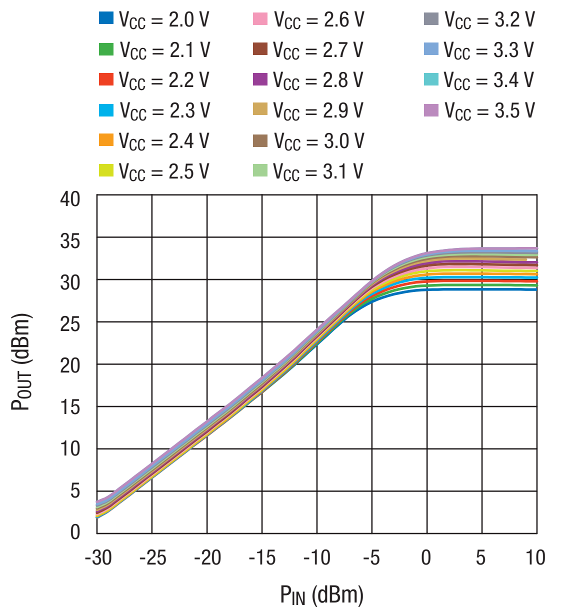
P_{OUT} vs. I_{CC} at V_{APC}
Conditions: CW, V_{CC} = 3.2 V, V_{REF} = 3.2 V,
F_C = 915 MHz, T_A = 25 °C



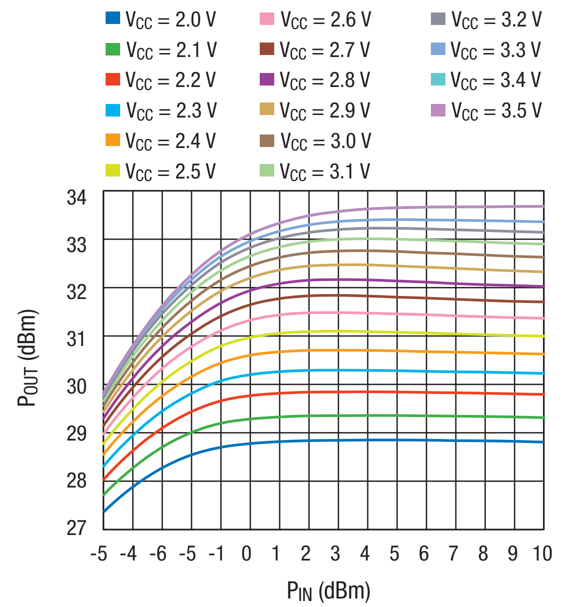
P_{OUT} vs. Gain at V_{APC}
Conditions: CW, V_{CC} = 3.2 V, V_{REF} = 3.2 V,
F_C = 915 MHz, T_A = 25 °C



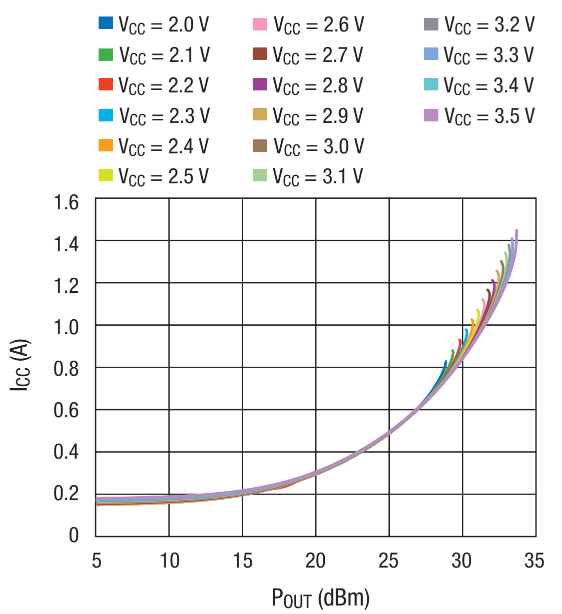
P_{OUT} vs. PAE at V_{APC}
Conditions: CW, V_{CC} = 3.2 V, V_{REF} = 3.2 V,
F_C = 915 MHz, T_A = 25 °C



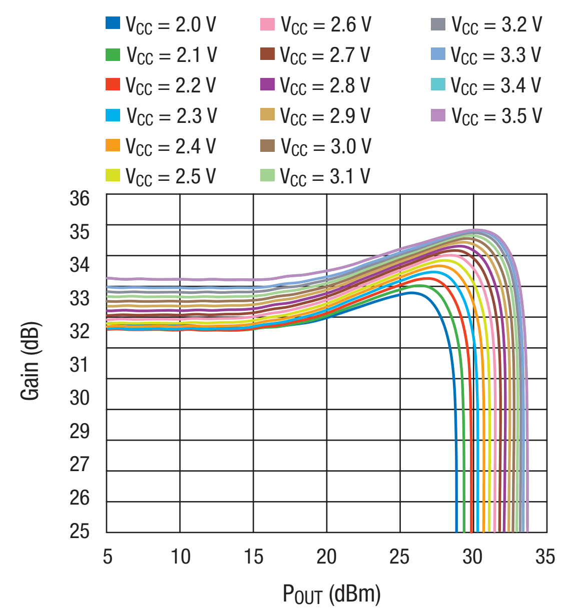
P_{IN} vs. P_{OUT} at V_{CC}
Conditions: CW, V_{APC} = 2.6 V, V_{REF} = 3.2 V,
F_C = 915 MHz, T_A = 25 °C



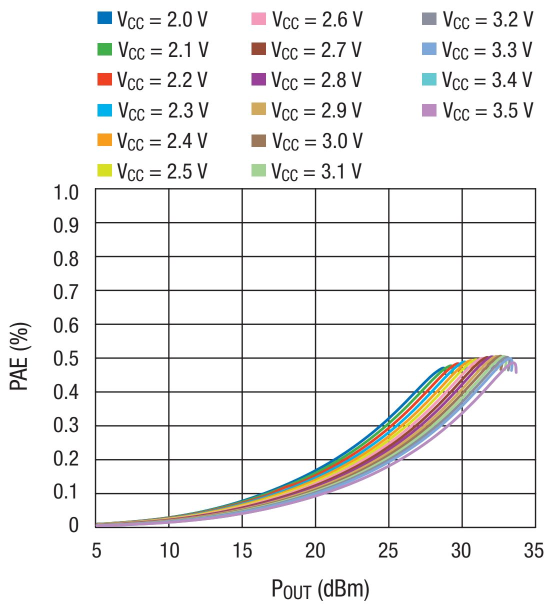
P_{IN} vs. P_{OUT} at V_{CC}
Conditions: CW, V_{APC} = 2.6 V, V_{REF} = 3.2 V,
F_C = 915 MHz, T_A = 25 °C



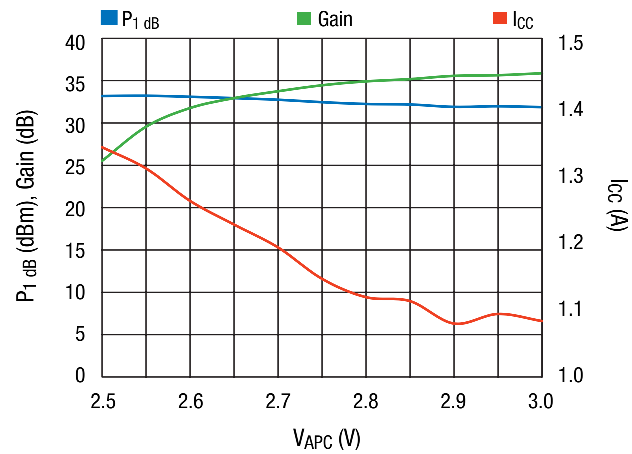
P_{OUT} vs. I_{CC} at V_{CC}
Conditions: CW, V_{APC} = 2.6 V, V_{REF} = V_{CC},
F_C = 915 MHz, T_A = 25 °C



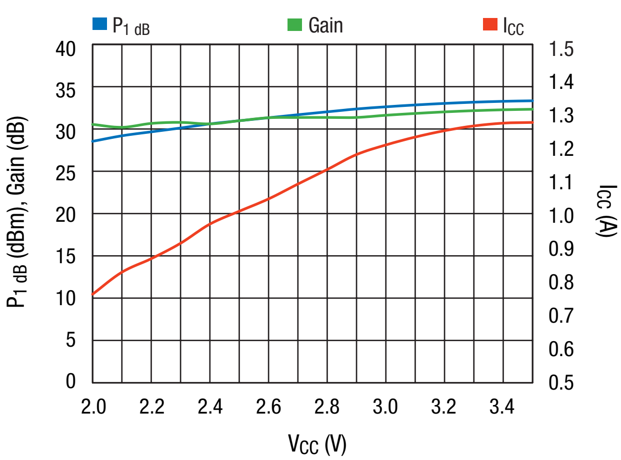
P_{OUT} vs. Gain at V_{CC}
Conditions: CW, V_{APC} = 2.6 V, V_{REF} = V_{CC},
F_C = 915 MHz, T_A = 25 °C



P_{OUT} vs. PAE at V_{CC}
Conditions: CW, V_{APC} = 2.6 V, V_{REF} = V_{CC},
F_C = 915 MHz, T_A = 25 °C



$P_{1\ dB}$, Gain, and I_{CC} vs. V_{APC}
Conditions: CW, V_{CC} = 3.2 V, V_{REF} = V_{CC},
F_C = 915 MHz, T_A = 25 °C



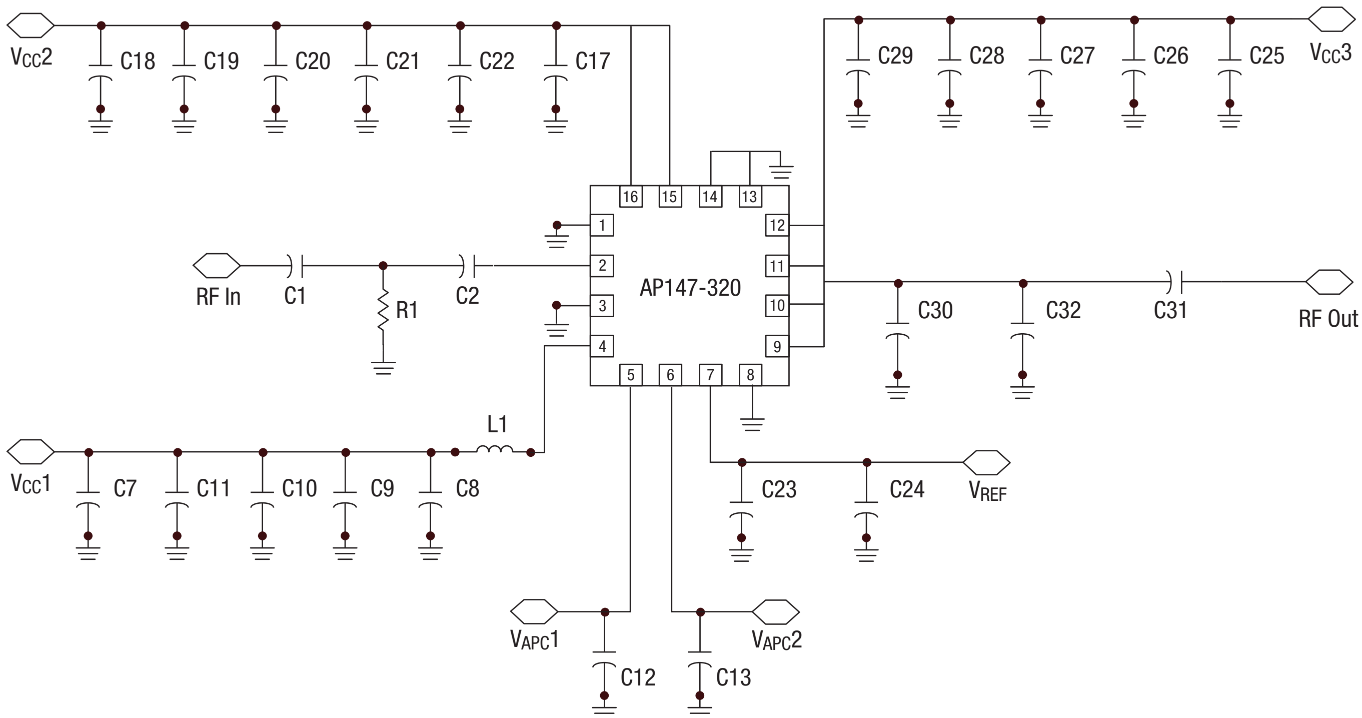
$P_{1\ dB}$, Gain, and I_{CC} vs. V_{CC}
Conditions: CW, V_{APC} = 2.6 V, V_{REF} = V_{CC},
F_C = 915 MHz, T_A = 25 °C

Bill of Material for Evaluation Board

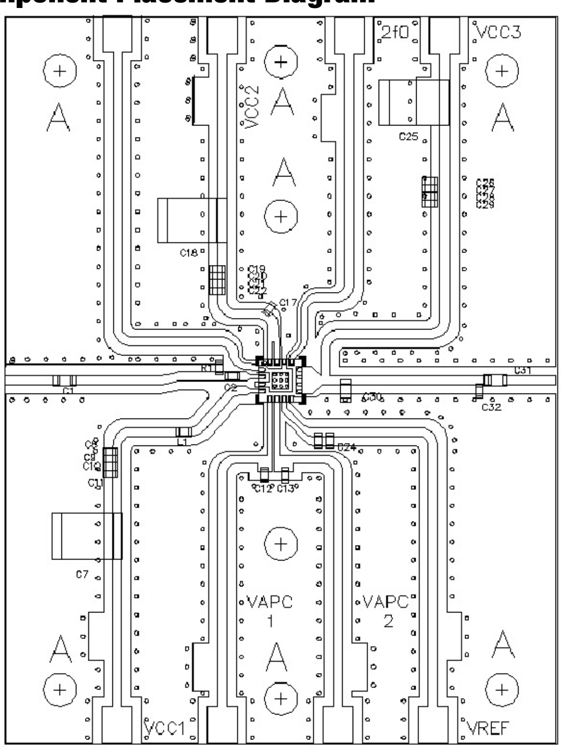
Part #	ID	Size	Value	Units	Manufacturer	Product Number
1	L_1	0402	1.8	nH	Johanson	L-07C1N8ST
2	R_1	0402	180	Ω	Panasonic*	ERJ2GEJ181X
3	C_1	0402	100	pF	Murata	GRM1555C1H101JD83E
4	C_2	0402	18	pF	Murata	GRM1555C1H180JZ35E
5	C_3	0402	DO NOT PLACE			
6	C_4	0402	DO NOT PLACE			
7	C_5	0402	DO NOT PLACE			
8	C_6	0402	DO NOT PLACE			
9	C_7	1206	10	μF	AVX	TAJA106M006R
10	C_8	0402	100	pF	Murata	GRM1555C1H101JD83E
11	C_9	0402	1	nF	Murata	GRM155R71H102KA01*
12	C_{10}	0402	10	nF	Murata	GRM155R71E103KA01*
13	C_{11}	0402	100	nF	Murata	GRM155R71A104KA01*
14	C_{12}	0402	100	pF	Murata	GRM1555C1H101JD83E
15	C_{13}	0402	100	pF	Murata	GRM1555C1H101JD83E
16	C_{14}	0402	DO NOT PLACE			
17	C_{15}	0402	DO NOT PLACE			
18	C_{16}	0402	DO NOT PLACE			
19	C_{17}	0402	68	pF	Murata	GRM1555C1H680JD83*
20	C_{18}	1206	10	μF	AVX	TAJA106M006R
21	C_{19}	0402	100	nF	Murata	GRM155R71A104KA01*
22	C_{20}	0402	10	nF	Murata	GRM155R71E103KA01*
23	C_{21}	0402	1	nF	Murata	GRM155R71H102KA01*
24	C_{22}	0402	100	pF	Murata	GRM1555C1H101JD83E
25	C_{23}	0402	100	pF	Murata	GRM1555C1H101JD83E
26	C_{24}	0402	10	nF	Murata	GRM155R71E103KA01*
27	C_{25}	1206	10	uF	AVX	TAJA106M006R
28	C_{26}	0402	100	nF	Murata	GRM155R71A104KA01*
29	C_{27}	0402	10	nF	Murata	GRM155R71E103KA01*
30	C_{28}	0402	1	nF	Murata	GRM155R71H102KA01*
31	C_{29}	0402	100	pF	Murata	GRM1555C1H101JD83E
32	C_{30}	0402	15	pF (Hi-Q)	Murata	GJM1555C1H150JB01E
33	C_{31}	0402	100	pF	Murata	GRM1555C1H101JD83E
34	C_{32}	0402	4.7	pF (Hi-Q)	Murata	GJM1555C1H4R7CB01E
35	SMA Connector, 50 Ω (X2)				AEP	9114-9113-000
36	PCB					

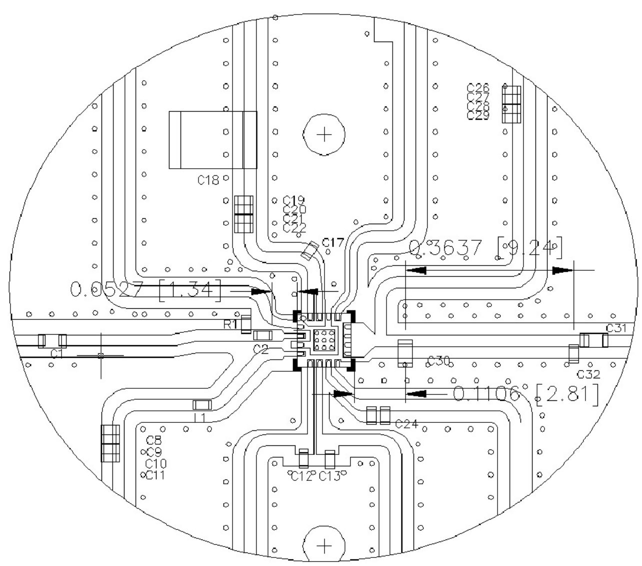
* Panasonic is Skyworks preferred vendor, however any suitable equivalent will do.

Application Circuit



Component Placement Diagram





Coplanar spacing: 0.026 inches.
Transmission line width: 0.025 inches.

Application Circuit Notes

RF Input, Pin 2, uses a 100 pf (C_1) DC blocking capacitor, a 180 Ω (R_1) resistor, and a 18 pF (C_2) tuning capacitor. The length of the line between the 18 pF capacitor and the amplifier is important to the input VSWR of the device. This distance is indicated below.

V_{CC}1, Pin 4, is the collector bias for stage 1. Capacitors of 10 uF (C_7), 100 pF (C_8), 1.0 nF (C_9), 10 nF (C_{10}), 100 nF (C_{11}), and an inductor of 1.8 nH (L_1) are used for cleaning up the power supply input signal and RF bypassing.

V_{CC}2, Pin 15, is the collector bias for stage 2. Tuning is accomplished, in conjunction with pin 16, with a 68 pF (C_{17}), 1.0 nF (C_{21}), and a 100 pF (C_{22}) capacitor on the collector bias line. Capacitors of 10 μF (C_{18}), 100 pF (C_{19}), and 10 nF (C_{20}) are used to clean up the power supply input signal.

V_{CC}2, Pin 16, is the collector bias for stage 2. Tuning is accomplished, in conjunction with pin 15, with a 68 pF (C_{17}), 1.0 nF (C_{21}), and a 100 pF (C_{22}) capacitor on the collector bias line. Capacitors of 10 μF (C_{18}), 100 pF (C_{19}), and 10 nF (C_{20}) are used to clean up the power supply input signal.

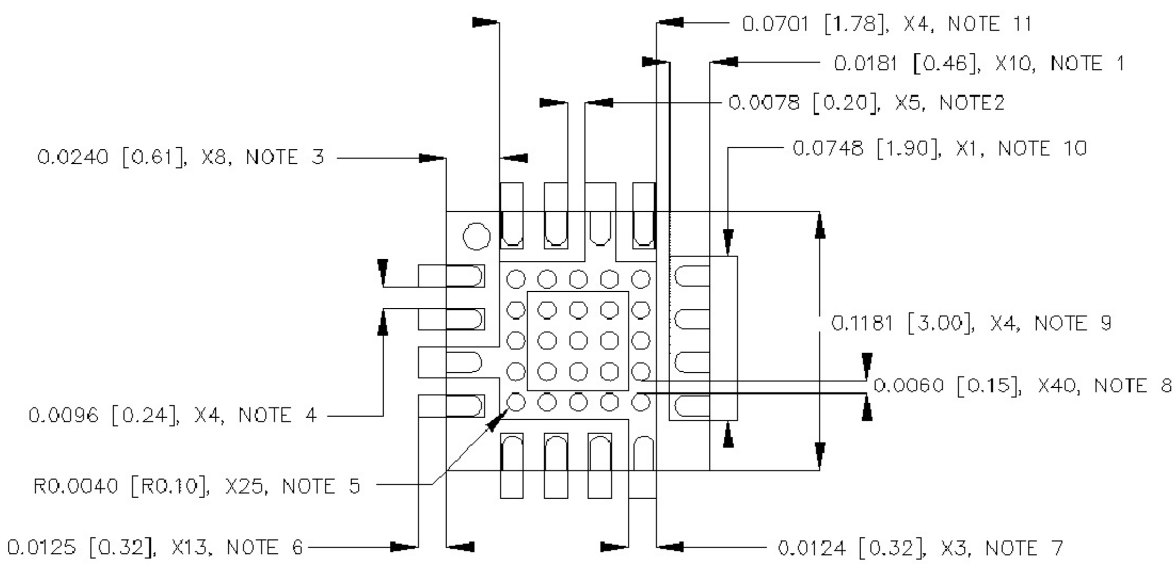
RF OUT/V_{CC}3, Pins (9–12), Tuning is accomplished with a 15 pF (C_{30}) high-Q capacitor and a 7.0 pF (C_{32}) high-Q capacitor on the RF output line. A length of transmission line and a bank of bypassing capacitors of 10 uF (C_{25}), 100 nF (C_{26}), 10 nF (C_{27}), 1.0 nF (C_{28}), and 100 pF (C_{29}) are required on the drain bias line for tuning and bias injection. A 100 pF (C_{31}) DC blocking capacitor is needed on the output line.

VAPC1, Pin 5, is the power control voltage for stages 1 and 2. A 100 pF (C_{13}) capacitor is required for biasing. Pin 5 and Pin 6 can be combined right at the amplifier by a jumper or a substrate connection between the two pads. In this configuration, a single 100 pF capacitor could be used for biasing.

VAPC6, Pin 6, is the power control voltage for stages 1 and 2. A 100 pF (C_{12}) capacitor is required for biasing. Pin 6 and pin 5 can be combined right at the amplifier by a jumper or a substrate connection between the two pads. In this configuration, a single 100 pF capacitor could be used for biasing.

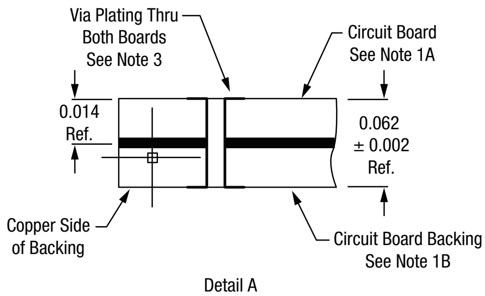
V_{REF}, Pin 7, is the control voltage for the bias control circuit. A combination of a 100 pF (C_{23}) and a 10 nF (C_{24}) capacitor is required for bypassing.

Package Footprint



NOTE: All units in inches [mm].
NOTE 1: Length of all non–grounded lands underneath the package.
NOTE 2: Width between grounded lands and non–grounded lands.
NOTE 3: Length of from ground pad to edge of package.
NOTE 4: Width between non–grounded lands.
NOTE 5: Radius of the vias.
NOTE 6: Length of all lands from the edge of the package.
NOTE 7: Width of the ground lands.
NOTE 8: Distance betwwen all vias.
NOTE 9: X and Y dimension of the package.
NOTE 10: Width of the land for RFOUT.
NOTE 11: Width of the land for the ground pad.

Evaluation Board Stack-Up



Application Board Bias Procedure

Step 1. Connect DC ground to the pad located in the top right-hand corner of the board as indicated below.

Step 2. Connect Stage 1 collector bias voltage, $V_{CC}1$, to the pad at the bottom left side of the board as indicated below. $V_{CC}1 = 3.2$ V

Step 3. Connect Stage 2 collector bias voltage, $V_{CC}2$, to the second pad in from the top left side of the board as indicated below. $V_{CC}2 = 3.2$ V

Step 4. Connect Stage 3 collector bias voltage, $V_{CC}3$, to the first pad at the top right side of the board as indicated below. $V_{CC}2 = 3.2$ V

Step 5. Connect the bias control voltage, V_{REF} to the pad at the bottom right of the board as indicated below. V_{REF} should be tied to the same line as $V_{CC}1$, $V_{CC}2$, and $V_{CC}3$ to obtain a single voltage supply.

NOTE: *It is important that the $V_{CC}1$, $V_{CC}2$, $V_{CC}3$, and V_{REF} voltage source be adjusted such that 3.2 V is measured at the board. The high drain currents will drop the drain voltage significantly if long leads are used. Adjust the bias voltage to compensate.*

Recommended Solder Reflow Profiles

Refer to the *"Recommended Solder Reflow Profile"* Application Note.

Tape and Reel Information

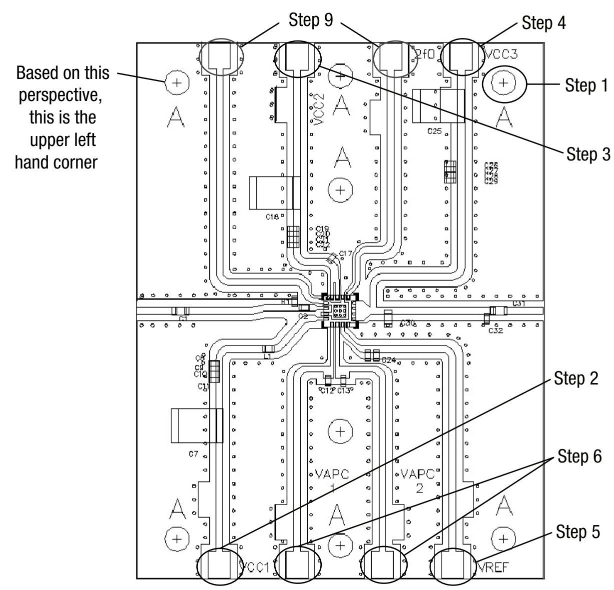
Refer to the *"Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation"* Application Note.

Step 6. Connect the power control voltages, $V_{APC}1$ and $V_{APC}2$, the middle two pads on the bottom of the board, as indicated below. This is done to obtain a single control voltage supply. $V_{APC} = 0$ V at this point.

Step 7. Apply RF at RF IN port at -20 dBm to start, then adjust power level to 0 to 5 dBm.

Step 8. The V_{APC} can be increased to 2.8 V max. or until desired output power level is achieved at RF OUT port.

Step 9. The pads in the upper left-hand corner, first from the left and third from the left, are to be grounded.



Branding Specifications