PROTEK DEVICES

PLCDA03C-6 thru PLCDA24C-6

LOW CAPACITANCE TVS ARRAY

APPLICATIONS

✔ Ethernet - 10/100 Base T
✔ FireWire
✔ SCSI
✔ Bluetooth & RF

IEC COMPATIBILITY (EN61000-4)

✔ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
✔ 61000-4-4 (EFT): 40A - 5/50ns
✔ 61000-4-5 (Surge): 24A, 8/20µs - Level 2(Line-Gnd) & Level 3(Line-Line)

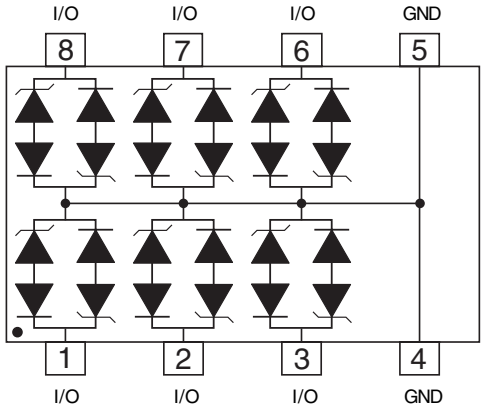
FEATURES

✔ 500 Watts Peak Pulse Power per Line (tp=8/20µs)
✔ Bidirectional Configuration
✔ Available in Multiple Voltage Types Ranging From 3.3V to 15V
✔ Protects Up to Six (6) Lines
✔ ESD Protection > 40 kilovolts
✔ Low Capacitance: 8pF
✔ RoHS Compliant

MECHANICAL CHARACTERISTICS

✔ Molded JEDEC SO-8
✔ Weight 70 milligrams (Approximate)
✔ Available in Lead-Free Pure-Tin Plating(Annealed)
✔ Solder Reflow Temperature:
Pure-Tin - Sn, 100: 260-270°C
✔ Consult Factory for Leaded Device Availability
✔ Flammability Rating UL 94V-0
✔ 12mm Tape and Reel Per EIA Standard 481
✔ Marking: Marking Code, Logo, Date Code & Pin One Defined By Dot on Top of Package

PIN CONFIGURATION



DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified			
PARAMETER	**SYMBOL**	**VALUE**	**UNITS**
Peak Pulse Power (t_p = 8/20µs) - See Figure 1	P_{PP}	500	Watts
Operating Temperature	T_L	-55 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified

PART NUMBER (See Notes 1)	DEVICE MARKING	RATED STAND-OFF VOLTAGE V_{WM} VOLTS	MINIMUM BREAKDOWN VOLTAGE @ 1mA $V_{(BR)}$ VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ I_P = 1A V_C VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @8/20µs V_C @ I_{PP}	MAXIMUM LEAKAGE CURRENT @V_{WM} I_D µA	MAXIMUM CAPACITANCE (See Note 1) @0V, 1 MHz C pF
PLCDA03C-6	PRS	3.3	4.5	7.0	20.0V @ 35.0A	125	8
PLCDA05C-6	PRT	5.0	6.0	9.8	24.0V @ 42.0A	20	8
PLCDA08C-6	PRW	8.0	8.5	13.4	26.0V @ 34.0A	10	8
PLCDA12C-6	PRV	12.0	13.3	19.0	33.0V@21.0A	2	8
PLCDA15C-6	PRU	15.0	16.7	22.0	39.0V @ 17.0A	2	8

Note 1: Capacitance between I/O pins and ground (pins 4 & 5) is typically 8pF. Capacitance between I/O pins is typically 4 pF.

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

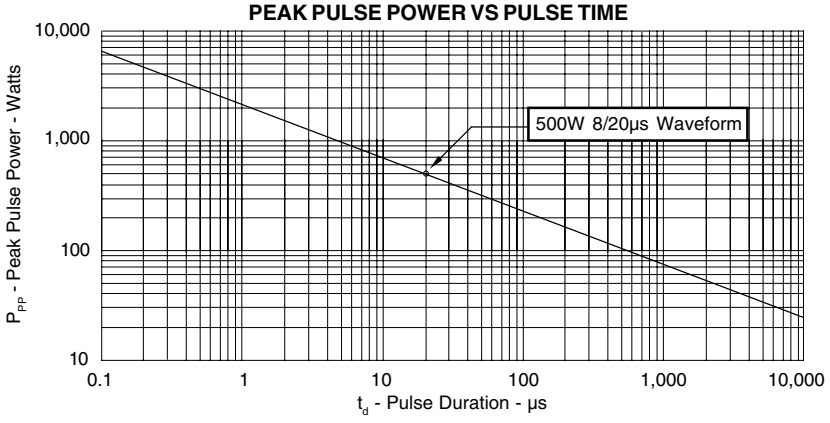
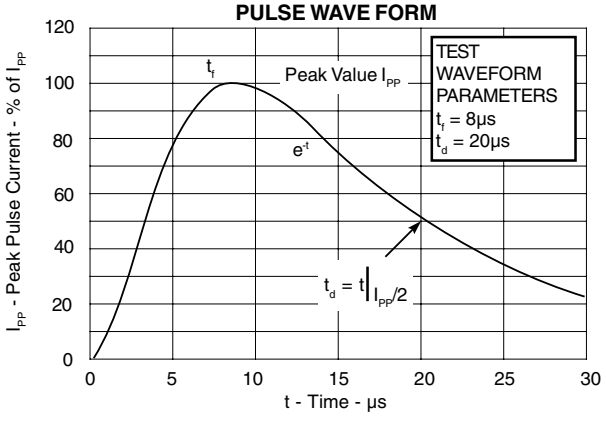


FIGURE 2
PULSE WAVE FORM



GRAPHS

FIGURE 3
POWER DERATING CURVE

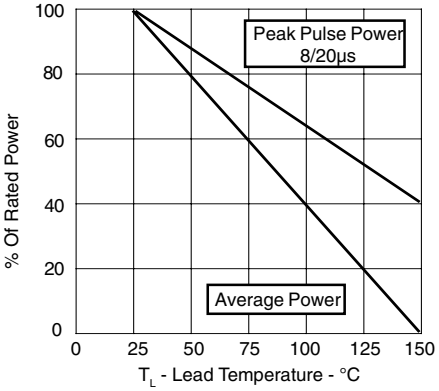
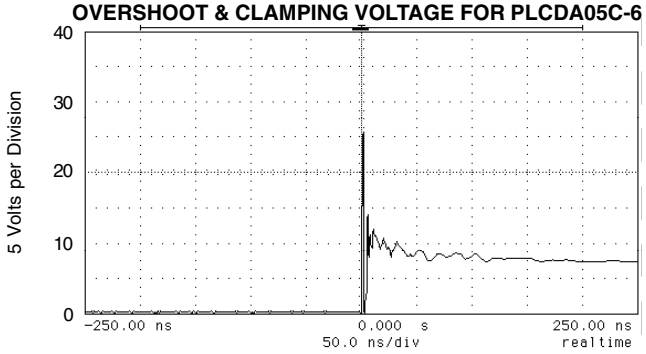


FIGURE 4
OVERSHOOT & CLAMPING VOLTAGE FOR PLCDA05C-6



ESD Test Pulse: 25 kilovolt, 1/30ns (waveshape)

FIGURE 5
TYPICAL CLAMPING VOLTAGE VS PEAK PULSE CURRENT FOR PLCDA05C-6

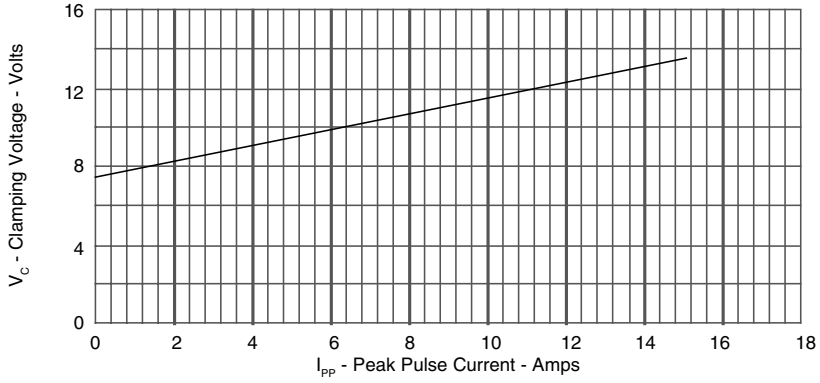


FIGURE 6
INSERTION LOSS - PLCDA05C-6

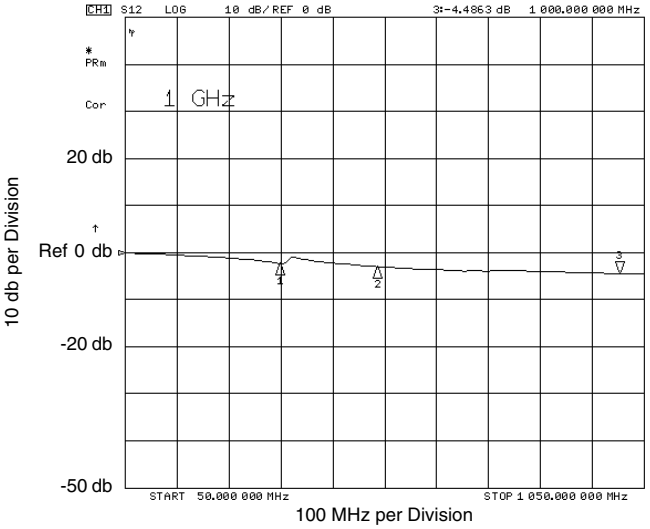
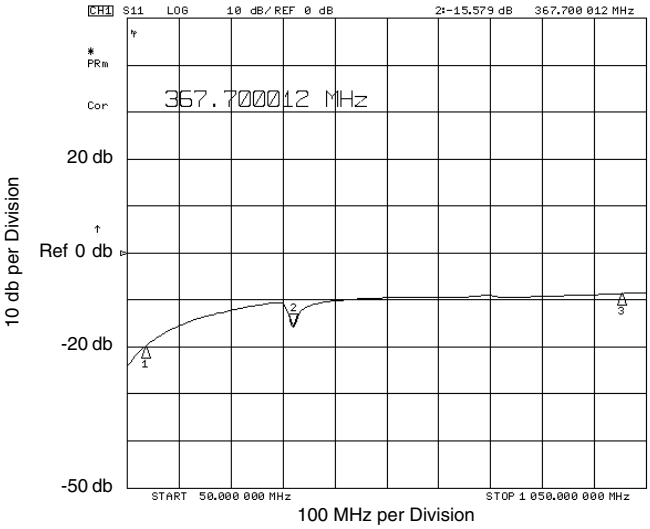


FIGURE 7
RETURN LOSS - PLCDA05C-6



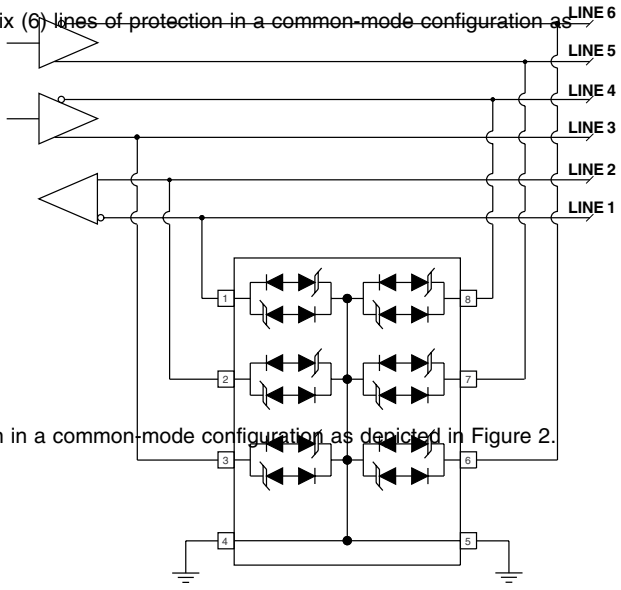
APPLICATION NOTE

The PLCDAxxC-6 Series are low capacitance, bidirectional TVS arrays that are designed to protect I/O or high speed data lines from the damaging effects of ESD or EFT. This product series has a surge capability of 500 Watts P_{PP} per line for an 8/20µs waveshape and offers ESD protection > 40kv.

BIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 1)

Figure 1: Typical Transceiver Protection Circuit

Ideal for use multimode transceiver I/O lines, the PLCDAxxC-6 Series provides up to six (6) lines of protection in a common-mode configuration as depicted in Figure 1.



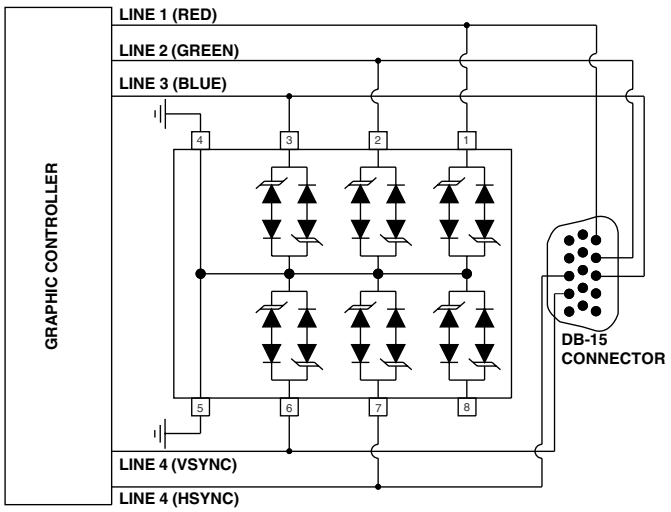
Circuit connectivity is as follows:
- ✔ Line 1 is connected to Pin 1.
- ✔ Line 2 is connected to Pin 2.
- ✔ Line 3 is connected to Pin 3.
- ✔ Line 4 is connected to Pin 8.
- ✔ Line 5 is connected to Pin 7.
- ✔ Line 6 is connected to Pin 6.
- ✔ Pins 4 and 5 are connected to Ground.

BIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 2)

The PLCDAxxC-6 Series also provides video line applications six (6) lines of protection in a common-mode configuration as depicted in Figure 2.

Circuit connectivity is as follows:
- ✔ Line 1 (Red) is connected to Pin 1.
- ✔ Line 2 (Green) is connected to Pin 2.
- ✔ Line 3 (Blue) is connected to Pin 3.
- ✔ Line 4 (VSYNC) is connected to Pin 6.
- ✔ Line 5 (HSYNC) is connected to Pin 7.
- ✔ Pins 4 and 5 are connected to Ground.

Figure 2: Typical Video Line Protection Circuit



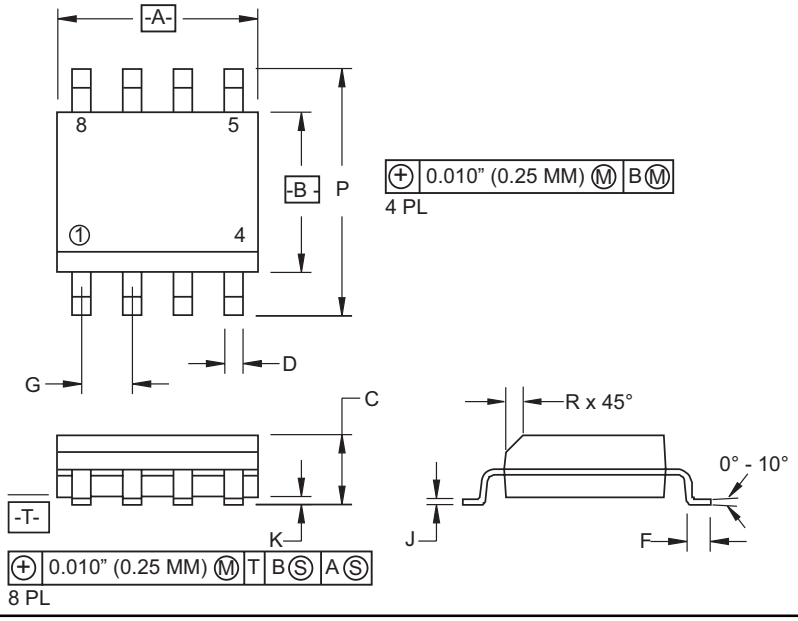
CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

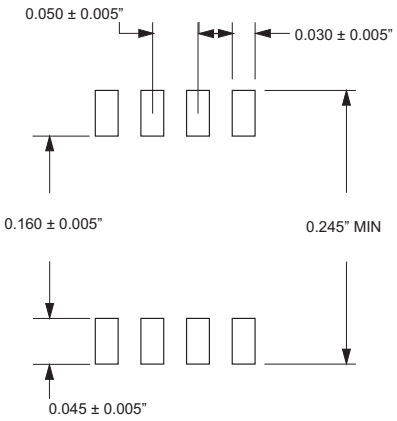
- ✔ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✔ The path length between the TVS device and the protected line should be minimized.
- ✔ All conductive loops including power and ground loops should be minimized.
- ✔ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✔ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

SO-8 PACKAGE OUTLINE & DIMENSIONS

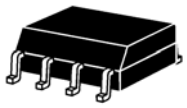
PACKAGE OUTLINE



MOUNTING PAD



SO-8



PACKAGE DIMENSIONS

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.250	0.016	0.049
G	1.27 BSC	1.27 BSC	0.05 BSC	0.05 BSC
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.008
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES

1. - T - = Seating Plane and Datum Surface.
2. Dimensions "A" and "B" are Datum.
3. Dimensions "A" and "B" do not include mold protrusion.
4. Maximum mold protrusion is 0.015" (0.380 mm) per side.
5. Dimensioning and tolerances per ANSI Y14.5M, 1982.
6. Dimensions are exclusive of mold flash and metal burrs.

TAPE & REEL/BULK ORDERING NOMENCLATURE

1. Surface mount product is taped and reeled in accordance with EIA-481.
2. Suffix-T7 = 7 Inch Reel - 1,000 pieces per 12mm tape, i.e. PLCDA05C-6-T7.
3. Suffix-T13 = 13 Inch Reel - 2,500 pieces per 12mm tape, i.e., PLCDA05C-6-T13.
4. Suffix - LF = Lead-Free, Pure-Tin Plating, i.e., PLCDA05C-6-LF-T7.
5. No Suffix = Product Shipped in Tubes of 98 pcs per Tube.

ProTek Devices
2929 South Fair Lane, Tempe, AZ 85282
Tel: 602-431-8101 Fax: 602-431-2288
E-Mail: sales@protekdevices.com
Web Site: www.protekdevices.com