

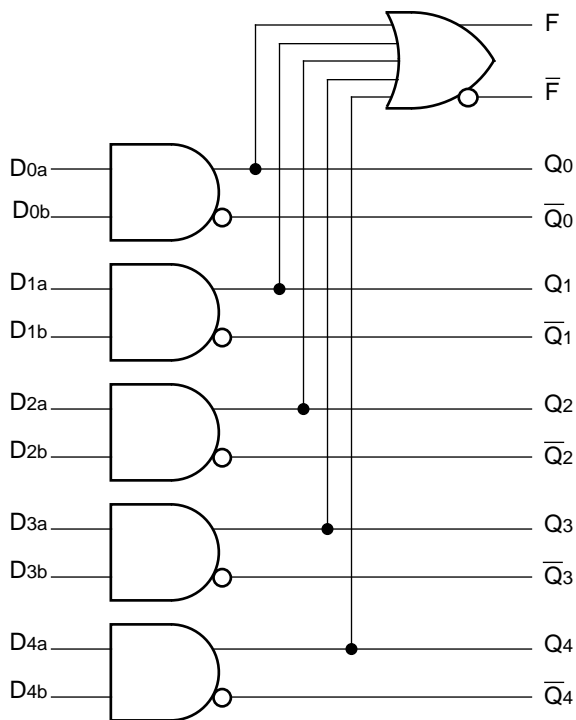
FEATURES

- 600ps max. propagation delay
- Extended 100E VEE range of -4.2V to -5.5V
- True and complementary outputs
- OR/NOR function outputs
- Fully compatible with Industry standard 10KH, 100K I/O levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E104
- Available in 28-pin PLCC package

DESCRIPTION

The SY10/100E104 are quint 2-input AND/NAND gates designed for use in new, high-performance ECL systems. The E104 also features a function output, F, which is the OR of all five AND gate outputs, while \bar{F} is the NOR. Both true and complementary outputs are provided.

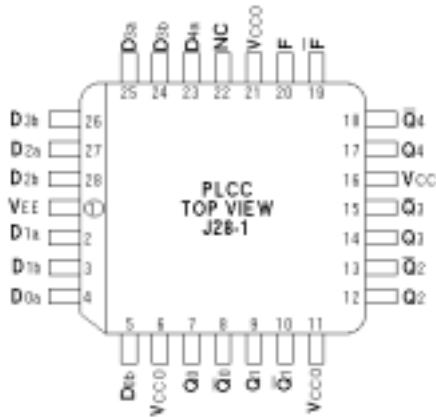
BLOCK DIAGRAM



PIN NAMES

Pin	Function
Dna, Dnb	Data Inputs
Q0-Q4	AND Outputs
$\bar{Q}_0-\bar{Q}_4$	NAND Outputs
F	OR Output
\bar{F}	NOR Output
Vcco	Vcc to Output

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E104JI	J28-1	Industrial	SY10E104JI	Sn-Pb
SY10E104JITR ⁽²⁾	J28-1	Industrial	SY10E104JI	Sn-Pb
SY100E104JI	J28-1	Industrial	SY100E104JI	Sn-Pb
SY100E104JITR ⁽²⁾	J28-1	Industrial	SY100E104JI	Sn-Pb
SY10E104JC	J28-1	Commercial	SY10E104JC	Sn-Pb
SY10E104JCTR ⁽²⁾	J28-1	Commercial	SY10E104JC	Sn-Pb
SY100E104JC	J28-1	Commercial	SY100E104JC	Sn-Pb
SY100E104JCTR ⁽²⁾	J28-1	Commercial	SY100E104JC	Sn-Pb
SY10E104JY ⁽³⁾	J28-1	Industrial	SY10E104JY with Pb-Free bar-line indicator	Matte-Sn
SY10E104JYTR ^(2, 3)	J28-1	Industrial	SY10E104JY with Pb-Free bar-line indicator	Matte-Sn
SY100E104JY ⁽³⁾	J28-1	Industrial	SY100E104JY with Pb-Free bar-line indicator	Matte-Sn
SY100E104JYTR ^(2, 3)	J28-1	Industrial	SY100E104JY with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

LOGIC EQUATION

$$F = (D0a \cdot D0b) + (D1a \cdot D1b) + (D2a \cdot D2b) + (D3a \cdot D3b) + (D4a \cdot D4b)$$

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

$V_{EE} = V_{EE} (\text{Min.})$ to $V_{EE} (\text{Max.})$; $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I _{IH}	Input HIGH Current	—	—	200	—	—	200	—	—	200	—	—	200	μA
I _{EE}	Power Supply Current	10E	38	46	38	46	38	46	38	46	38	46	46	mA
		100E	38	46	38	46	38	46	38	46	44	53		

Note:

1. Specification for packaged product only.

AC ELECTRICAL CHARACTERISTICS⁽²⁾

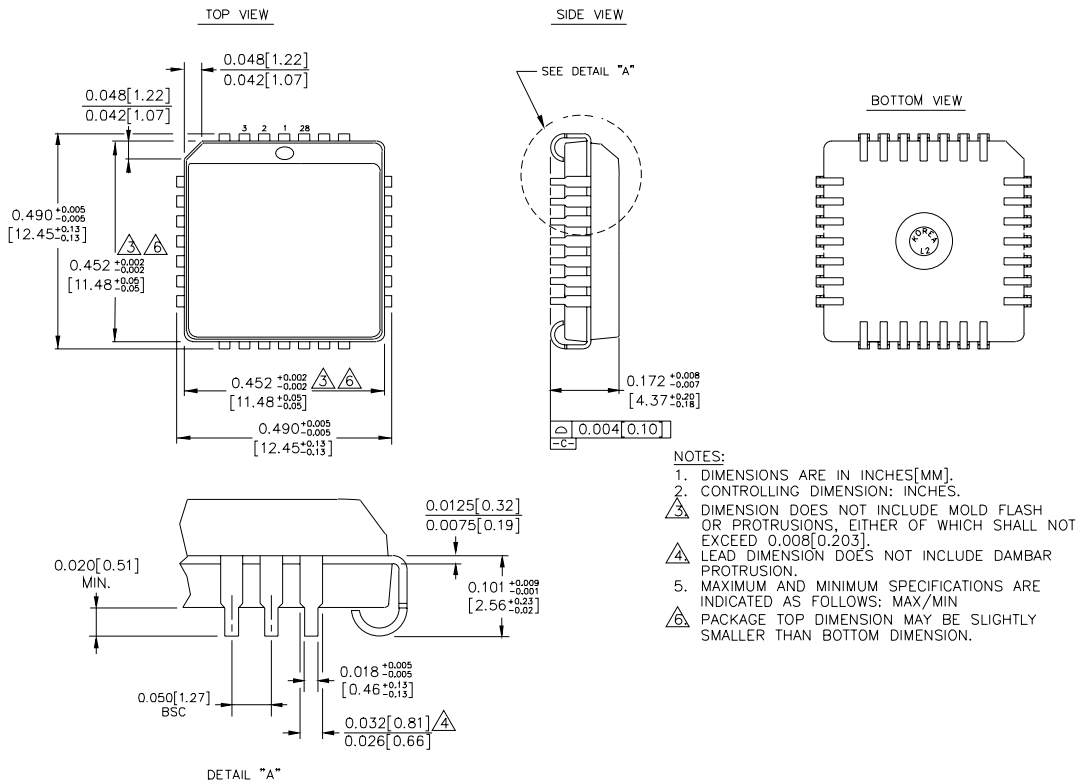
$V_{EE} = V_{EE} (\text{Min.})$ to $V_{EE} (\text{Max.})$; $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{PD}	Propagation Delay to Output	D to Q	225	385	600	225	385	600	225	385	600	225	385	600	ps
		D to F	500	725	1000	500	725	1000	500	725	1000	500	725	1000	
t _{skew}	Within-Device Skew, D to Q ⁽¹⁾	—	75	—	—	75	—	—	75	—	—	75	—	ps	
t _r t _f	Rise/Fall Time 20% to 80%	Q	275	425	700	275	425	700	275	425	700	275	425	700	ps
		F	300	475	700	300	475	700	300	475	700	300	475	700	

Notes:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Specification for packaged product only.

28-PIN PLCC (J28-1)



Rev. 03

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