STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCT NAME BU7285GU

FUNCTION Serial Interface for Mobile Phone
MSDL(Mobile Shrink Data Link) Tranceiver

FEATURE
- MSDL Technology be able to reduce the 24 wires to 7 wires.(Max Rate is 160Mbps)
- Low signal amplitude about 40mV using current mode drive realize low power consumption and low EMI.

○ Table1. Absolute maximum ratings

Parameter	Symbol	Rated values	Unit	Remarks
Power supply voltage	VDD	-0.3 ～ +4.5	V	-
Input Voltage	VIN	-0.3 ～ VDD+0.3	V	-
Output Voltage	VOUT	-0.3 ～ VDD+0.3	V	-
Input Current	IIN	-20 ～ +20	mA	-
Output Current	IOUT	-70 ～ +70	mA	-
Preservation Temperature	Tstg	-55 ～ +125	℃	-

○ Table2. Recommend operating conditions (Ta = 25℃)

Parameter	Symbol	MIN	TYP	MAX	Unit	Remarks
Power Supply Voltage(V18)	V18	1.70	1.85	3.15	V	V18≦V28
Power Supply Voltage(V28)	V28	2.55	2.85	3.15	V	V18≦V28
Operating Clock Frequency	fpclk	3.0	6.6	7.3	MHz	-
Operating Temperature Range	Topr	-25	25	85	℃	-
External Register Value	DRV_R		18±5%		kΩ	-

※ About shape / delivery forms of this product, please refer to "Specification of Chip Shipment"
※ About detailed function explanation of this product, please refer to "Function Description Guide"

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○ Block diagram

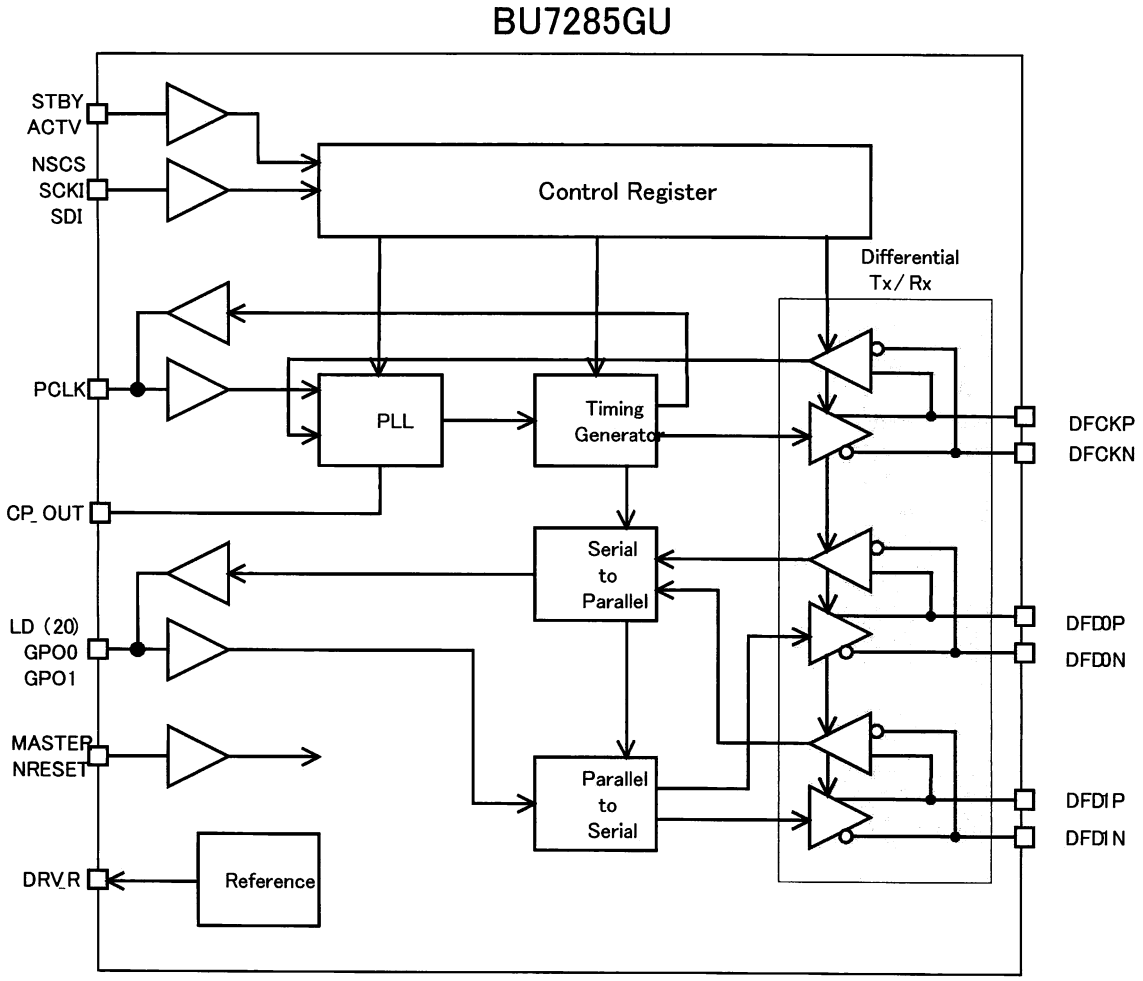

Figure1. Block Diagram

○ Electrical characteristics

DC characteristics

Table3. Parallel Interface

(Ta=-25℃, V18=1.85V, V28=2.85V, unless otherwise specified)

Parameter		Symbol	Limit			Unit	Conditions
			MIN	TYP	MAX		
"H" input voltage		VIH	0.7V18	-	V18	V	-
"L" input voltage		VIL	0	-	0.3V18	V	-
"H" output voltage		VOH	V18-0.5	-	V18	V	IOH=1.0mA
"L" output voltage		VOL	0	-	0.5	V	IOL=1.0mA
Input leak current		IIZ	-5	-	5	uA	VI=0～V18
Output leak current		IOZ	-10	-	10	uA	-
Master Mode Operating current	V18	Ioprm18	-	0.06	10	mA	fpclk=6MHz DRV_R=18kΩ
	V28	Ioprm28	-	2.33	10	mA	
Slave Mode Operating current	V18	Ioprs18	-	0.29	10	mA	fpclk=6MHz DRV_R=18kΩ
	V28	Ioprs28	-	6.07	10	mA	
Standby current	V18	IST18	-	0.1	10	uA	Sleep mode
	V28	IST28	-	0.1	10		

Table4. Differential Serial Interface

(Ta=-25℃, V18=1.85V, V28=2.85V, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		MIN	TYP	MAX		
"H" Sink Current	I_{SH}	-	620	-	uA	Master Mode DRV_R=18kΩ
"L" Sink Current	I_{SL}	-	240	-	uA	Master Mode DRV_R=18kΩ
Output Terminal Voltage	V_{OMIN}	1.7	1.9	2.1	V	-
DFCK Short Term Jitter	T_{JITTER}	-	300	-	pS	fpclk=6MHz
Input Leak Current	I_{LDF}	-	-	10	uA	Sleep Mode
Bandgap Voltage	V_{bg}	-	1.23	-	V	-

AC characteristics

Table5. Register Control Serial Interface

(Ta=-25℃, V18=1.85V, V28=2.85V, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		MIN	TYP	MAX		
SCKI cycle time	t_{CYC_SCK}	50	-	-	ns	-
SCKI "H" time	t_{WHC_SCK}	22	-	-	ns	-
SCKI "L" time	t_{WLC_SCK}	22	-	-	ns	-
SDI setup time	t_{DSU}	10	-	-	ns	-
SDI hole time	t_{DH}	10	-	-	ns	-
NSCS setup time	t_{SCSS}	10	-	-	ns	-
NSCS hole time	t_{HCSS}	10	-	-	ns	-

*Show timing chart at Figure2

Table6. Parallel Interface (Master Mode, Input)

(Ta=-25℃, V18=1.85V, V28=2.85V, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		MIN	TYP	MAX		
PCLK cycle time	t_{CYC_PCK}	125	151.5	1000	ns	-
PCLK "H" time	t_{WHC_PCK}	56	-	-	ns	t_{CYC_PCK}=151.5[ns]
PCLK "L" time	t_{WLC_PCK}	56	-	-	ns	t_{CYC_PCK}=151.5[ns]
LD hold time	t_{DH_LD}	30	-	-	ns	t_{CYC_PCK}=151.5[ns]
LD setup time	t_{DSU_LD}	40	-	-	ns	t_{CYC_PCK}=151.5[ns]

*Show timing chart at Figure3

Table7. Parallel Interface (Slave Mode, Output)

(Ta=-25℃, V18=1.85V, V28=2.85V, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		MIN	TYP	MAX		
PCLK cycle time	t_{CYC_PCKO}	125	151.5	1000	ns	CL=10[pF]
PCLK"H"time	t_{WHC_PCK}	56	-	-	ns	t_{CYC_PCKO}=151.5[ns] CL=10[pF]
PCLK"L"time	t_{WLC_PCK}	56	-	-	ns	t_{CYC_PCKO}=151.5[ns] CL=10[pF]
LD output delay	t_{DLY_LD}	-	-	10	ns	t_{CYC_PCKO}=151.5[ns] CL=10[pF]

*Show timing chart at Figure4

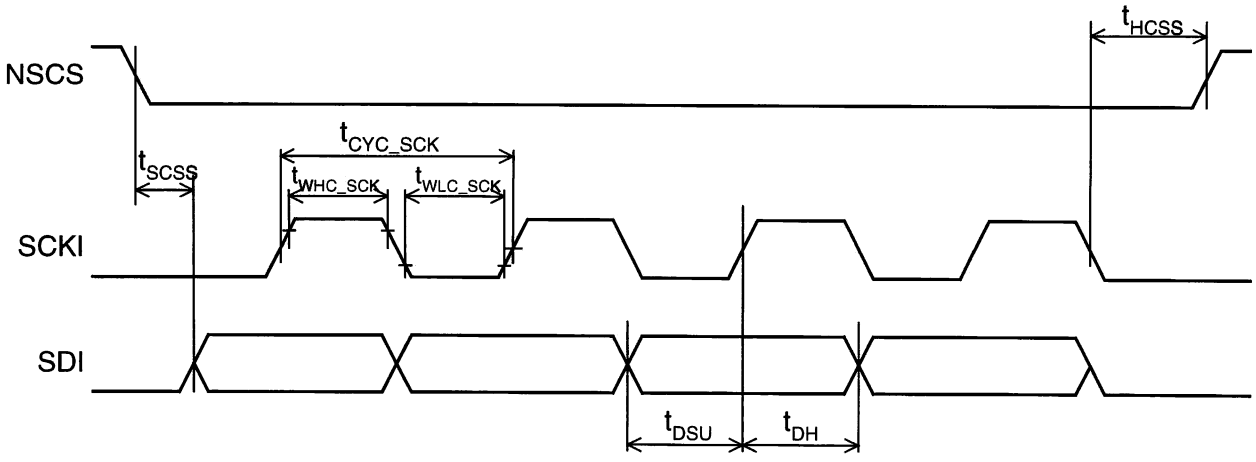

Figure2. AC Characteristics of Register Control Serial Interface

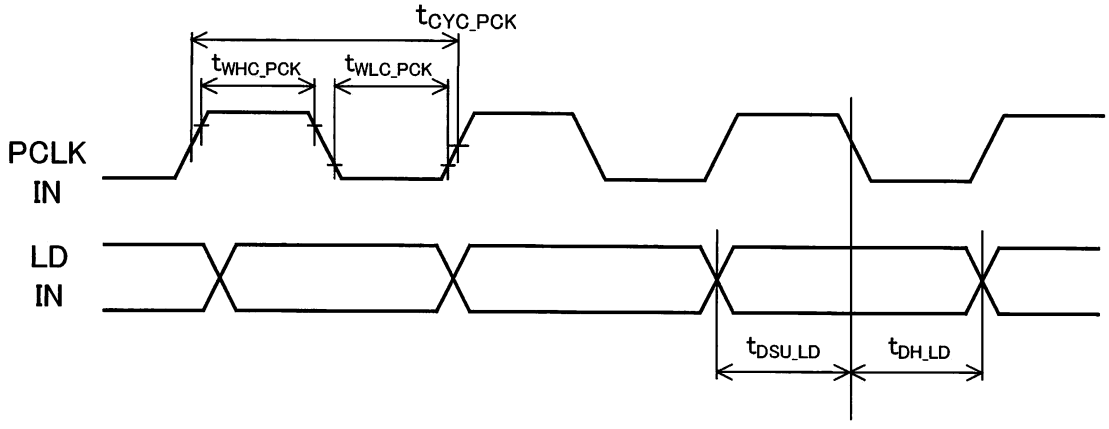

Figure3. AC Characteristics of Parallel Interface (Master Mode, Input)

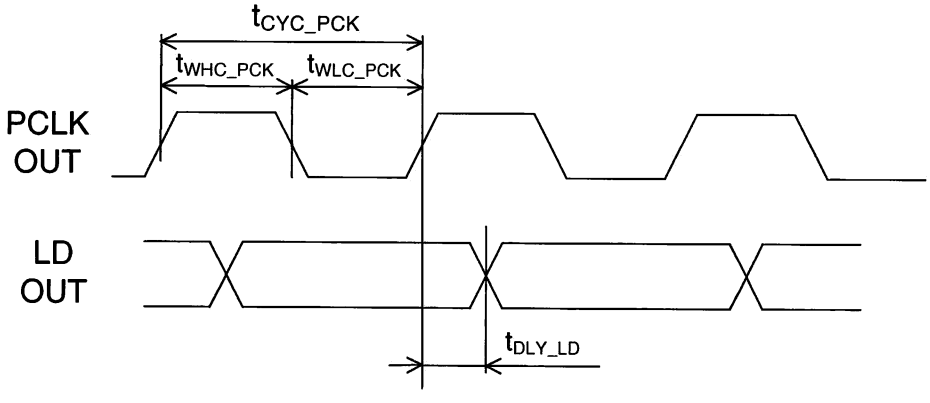

Figure4. AC Characteristics of Parallel Interface (Slave Mode, Output)

Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operatingconditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

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As of 18th. April 2005