NIMD6302R2

HDPlus Dual N-Channel Self-protected Field Effect Transistors with 1:200 Current Mirror FET

HDPlus devices are an advanced HDTMOS™ series of power MOSFET which utilize ON's latest MOSFET technology process to achieve the lowest possible on−resistance per silicon area while incorporating smart features. They are capable of withstanding high energy in the avalanche and commutation modes. The avalanche energy is specified to eliminate guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

This HDPlus device features an integrated Gate−to−Source clamp for ESD protection. Also, this device features a mirror FET for current monitoring.

- ±3.5% Current Mirror Accuracy in Linear Region
- ±15% Current Mirror Accuracy in Low Current Saturation Region
- IDSS Specified at Elevated Temperature
- Avalanche Energy Specified
- Current Sense FET
- ESD Protected on the Main and the Mirror FET

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

MAIN MOSFET MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	30	Vdc
Drain−to−Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	30	Vdc
Gate−to−Source Voltage	V_{GS}	±16	Vdc
Drain Current − Continuous @ T_A = 25°C − Continuous @ T_A = 100°C (Note 3) − Pulsed ($t_p \le 10$ μs)	 I_D I_D I_{DM}	 6.5 4.4 33	 Adc Adc Apk
Total Power Dissipation @ T_A = 25°C (Note 1) Total Power Dissipation @ T_A = 25°C (Note 2)	P_D P_D	1.3 1.67	W
Thermal Resistance Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2)	 $R_{\theta JA}$ $R_{\theta JA}$	 96 75	°C/W
Single Pulse Drain−to−Source Avalanche Energy (Note 3) (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, V_{DS} = 20 Vdc, I_L = 15 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	250	mJ

1. Mounted onto min pad board.
2. Mounted onto 1″ pad board.
3. Switching characteristics are independent of operating junction temperatures.

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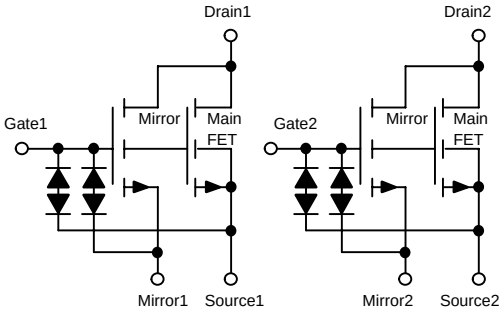
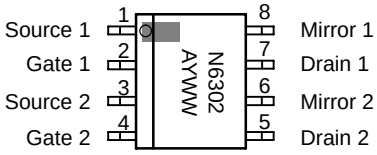
5.0 AMPERES
30 VOLTS
$R_{DS(on)}$ = 50 mΩ

ISOLATED DUAL PACKAGING



SOIC−8
CASE 751
STYLE 19

MARKING DIAGRAM



(Top View)

N6302 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NIMD6302R2	SOIC−8	2500/Tape & Reel

MAIN MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−to−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	30 20	35 23	− 30	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 125°C) (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 175°C)	I_{DSS}	− − −	0.065 0.2 11	10 100 100	μAdc
Gate−Body Leakage Current (V_{GS} = 12 Vdc, V_{DS} = 0 Vdc) (V_{GS} = 3.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	− −	11 12	18 100	μAdc nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) (V_{DS} = V_{GS}, I_D = 250 μAdc, T_J = 75°C) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	1.0 1.1 −	1.33 1.17 3.8	2.0 − 4.6	Vdc mV/°C
Static Drain−to−Source On−Resistance (Note 4) (V_{GS} = 10 Vdc, I_D = 3.0 Adc, T_J @ 25°C) (V_{GS} = 10 Vdc, I_D = 3.0 Adc, T_J @ 125°C) (V_{GS} = 10 Vdc, I_D = 3.0 Adc, T_J @ 175°C)	$R_{DS(on)}$	− − −	35 57 69	50 65 90	mΩ
Forward Transconductance (Note 4) (V_{DS} = 6.0 Vdc, I_D = 15 Adc)	g_{FS}	14.5	19.8	25	Mhos
DYNAMIC CHARACTERISTICS (Note 5)					
Input Capacitance	(V_{DS} = 6.0 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	−	301	600	pF
Output Capacitance		C_{oss}	−	265	350	
Transfer Capacitance		C_{rss}	−	82	200	
SWITCHING CHARACTERISTICS (Note 5)					
Turn−On Delay Time	(V_{DD} = 6.0 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc, R_G = 2.5 Ω)	$t_{d(on)}$	−	9.2	9.6	ns
Rise Time		t_r	−	56.5	75.3	
Turn−Off Delay Time		$t_{d(off)}$	−	35.9	40	
Fall Time		t_f	−	36.3	40.6	
Turn−On Delay Time	(V_{DD} = 6.0 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 2.5 Ω)	$t_{d(on)}$	−	6.3	7.0	ns
Rise Time		t_r	−	2.7	3.1	
Turn−Off Delay Time		$t_{d(off)}$	−	66.5	70.5	
Fall Time		t_f	−	36.5	39.4	
Gate Charge	(V_{DS} = 6.0 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc)	Q_T	−	3.91	4.5	nC
		Q_1	−	1.0	1.25	
		Q_2	−	1.59	1.95	
		Q_3	−	1.48	1.64	
Gate Charge	(V_{DS} = 6.0 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	−	8.03	13.6	nC
		Q_1	−	1.06	1.36	
		Q_2	−	1.75	2.82	
		Q_3	−	1.54	1.75	

4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
5. Switching characteristics are independent of operating junction temperatures.

MAIN MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage (Notes 6 & 7)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc) (I_S = 3.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C) (I_S = 3.0 Adc, V_{GS} = 0 Vdc, T_J = 175°C)	V_{SD}	− − −	0.79 0.65 0.58	0.86 0.72 0.64	Vdc
Reverse Recovery Time (Note 7)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	−	30.8	41	ns
		t_a	−	14.6	18	
		t_b	−	15.2	20.2	
Reverse Recovery Stored Charge (Note 7)		Q_{RR}	−	0.020	0.03	μC
MIRROR MOSFET CHARACTERISTICS (T_J = 25°C unless otherwise noted)						
Main/Mirror MOSFET Current Ratio Operating in the Saturation Region	(V_{DS} = 6.0 Vdc, I_{Dmain} = 5.0 mA) (V_{DS} = 6.0 Vdc, I_{Dmain} = 5.0 mA, T_A = 125°C)	I_{RAT}	170 167	200 196	230 225	−
Main/Mirror Current Ratio Variation versus Temperature Operating in the Saturation Region	(V_{DS} = 6.0 Vdc, I_{Dmain} = 5.0 mA, T_A = 25 to 125°C)	$I_{\Delta RAT}$	170	200	230	−
Main/Mirror MOSFET Current Ratio Operating in the Linear Region	(V_{GS} = 3.0 Vdc, I_{Dmain} = 1.0 A) (V_{GS} = 3.0 Vdc, I_{Dmain} = 1.0 A, T_A = 175°C)	I_{RAT}	166 165	172 171	178 177	−
Main/Mirror Current Ratio Variation versus Temperature Operating in the Linear Region	(V_{GS} = 3.0 Vdc, I_{Dmain} = 1.0 A, T_A = −40 to +175°C)	$I_{\Delta RAT}$	166	172	184	−
Main/Mirror MOSFET Current Ratio Operating in the Linear Region	(V_{GS} = 5.0 Vdc, I_{Dmain} = 1.0 A) (V_{GS} = 5.0 Vdc, I_{Dmain} = 1.0 A, T_A = 175°C)	I_{RAT}	150 155	155 161	160 166	−
Main/Mirror Current Ratio Variation versus Temperature Operating in the Linear Region	(V_{GS} = 5.0 Vdc, I_{Dmain} = 1.0 A, T_A = −40 to +175°C)	$I_{\Delta RAT}$	150	155	166	−
Main/Mirror MOSFET Current Ratio Operating in the Linear Region	(V_{GS} = 10 Vdc, I_{Dmain} = 1.0 A) (V_{GS} = 10 Vdc, I_{Dmain} = 1.0 A, T_A = 175°C)	I_{RAT}	141 148	146 153	155 157	−
Main/Mirror Current Ratio Variation versus Temperature Operating in the Linear Region	(V_{GS} = 10 Vdc, I_{Dmain} = 1.0 A, T_A = −40 to +175°C)	$I_{\Delta RAT}$	141	146	157	−

MAIN AND SENSE MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Electro−Static Discharge (ESD) Capability	Main FET Sense FET	_ _	1800 1800	− −	− −	V
Charge Device Model (CDM) Capability	Main/Sense FET	_	2000	−	−	V

6. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
7. Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

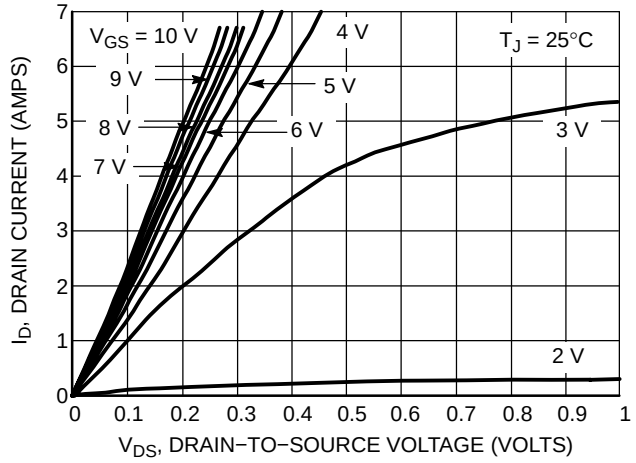


Figure 1. On−Region Characteristics

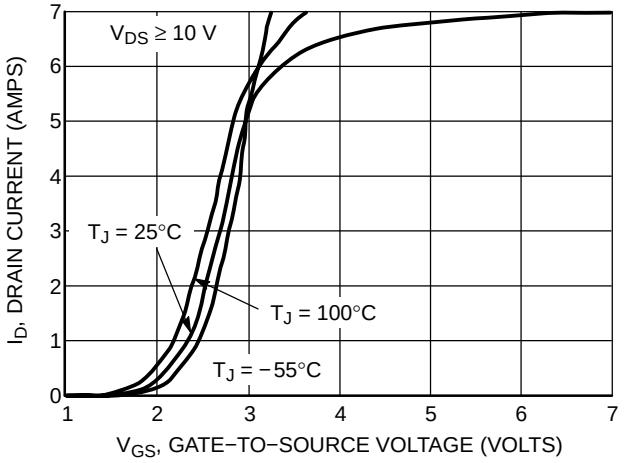


Figure 2. Transfer Characteristics

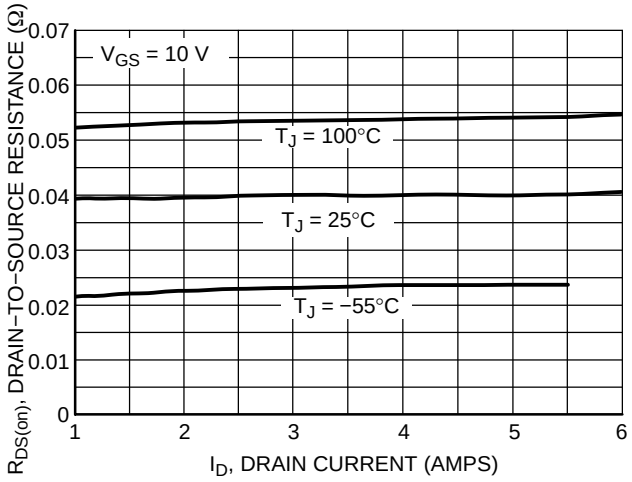


Figure 3. On−Resistance versus Drain Current and Temperature

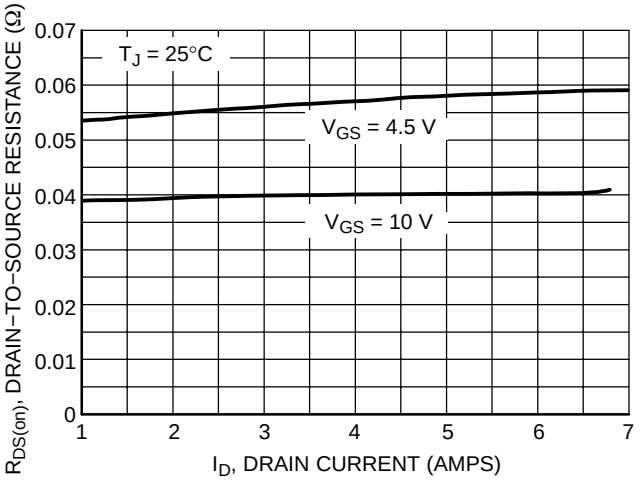


Figure 4. On−Resistance versus Drain Current and Gate Voltage

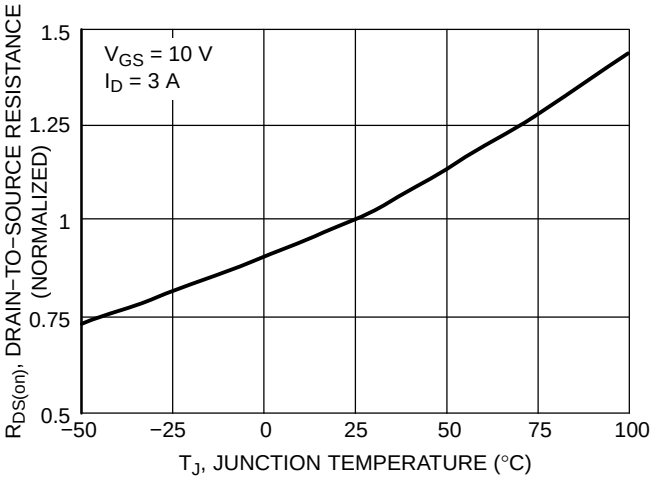


Figure 5. On−Resistance Variation with Temperature

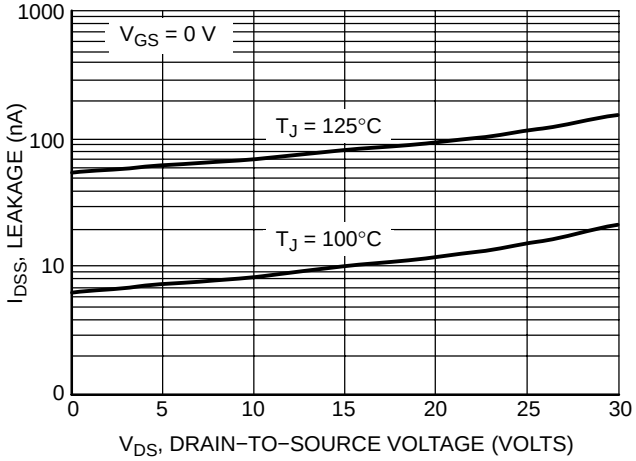


Figure 6. Drain−To−Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain−gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn−on and turn−off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \text{ In } [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \text{ In } (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off−state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on−state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

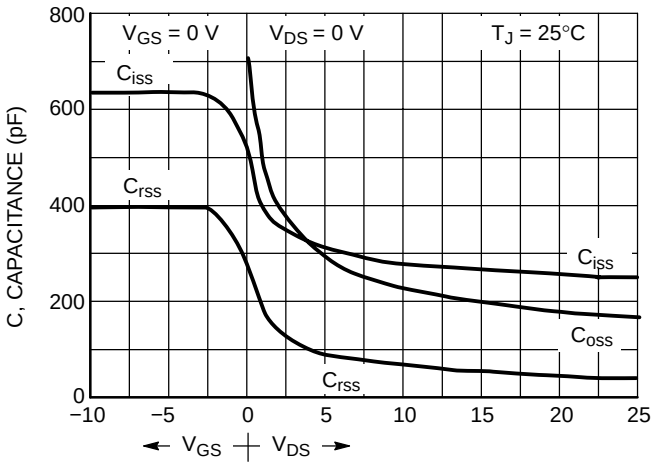


Figure 7. Capacitance Variation

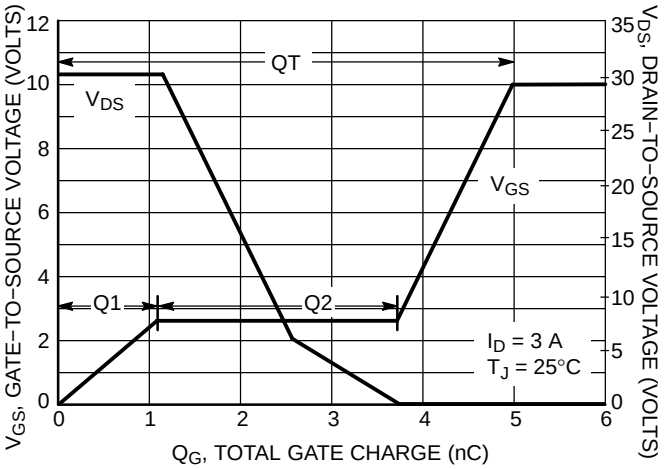


Figure 8. Gate−To−Source and Drain−To−Source Voltage versus Total Charge

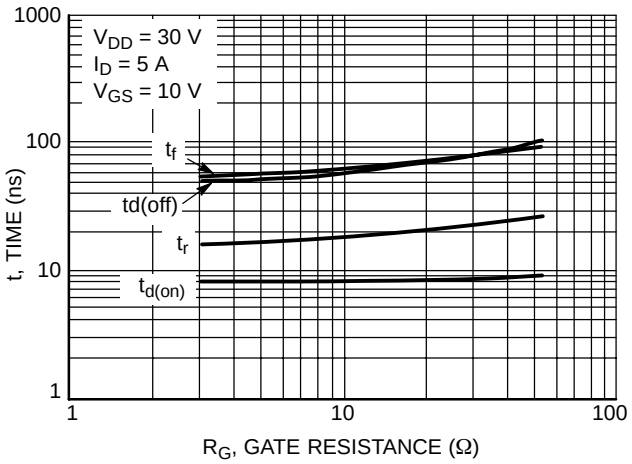


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN−TO−SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 14. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

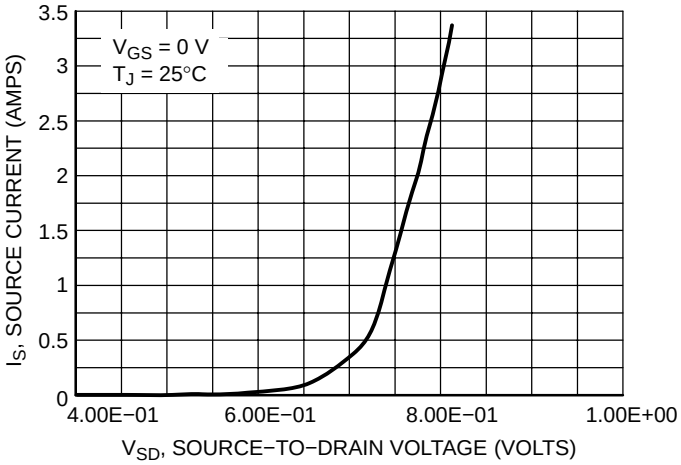


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain−to−source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance − General Data and Its Use.”

Switching between the off−state and the on−state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E−FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non−linearly with an increase of peak current in avalanche and peak junction temperature.

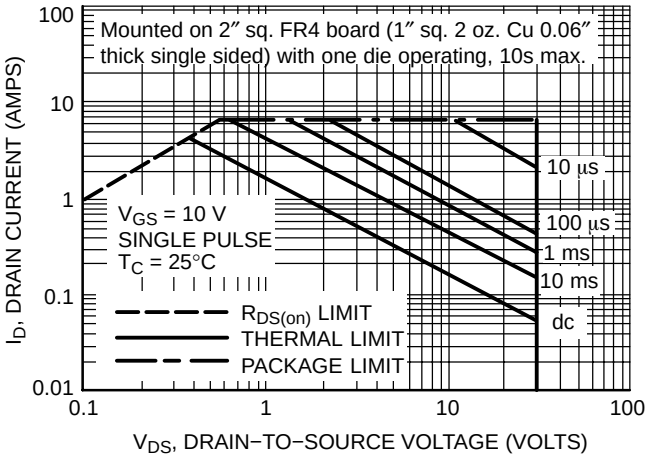


Figure 11. Maximum Rated Forward Biased Safe Operating Area

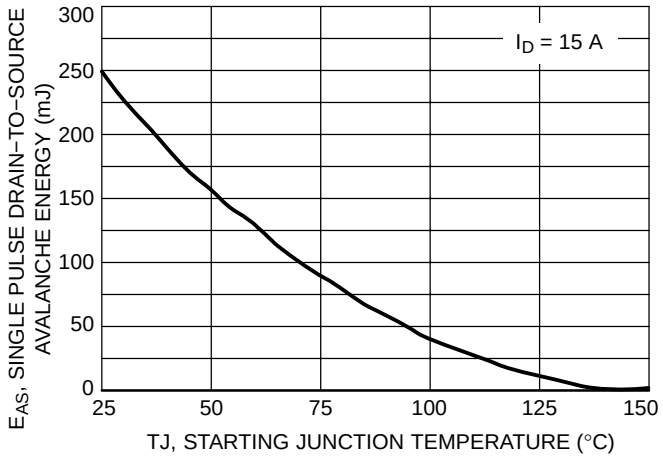


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

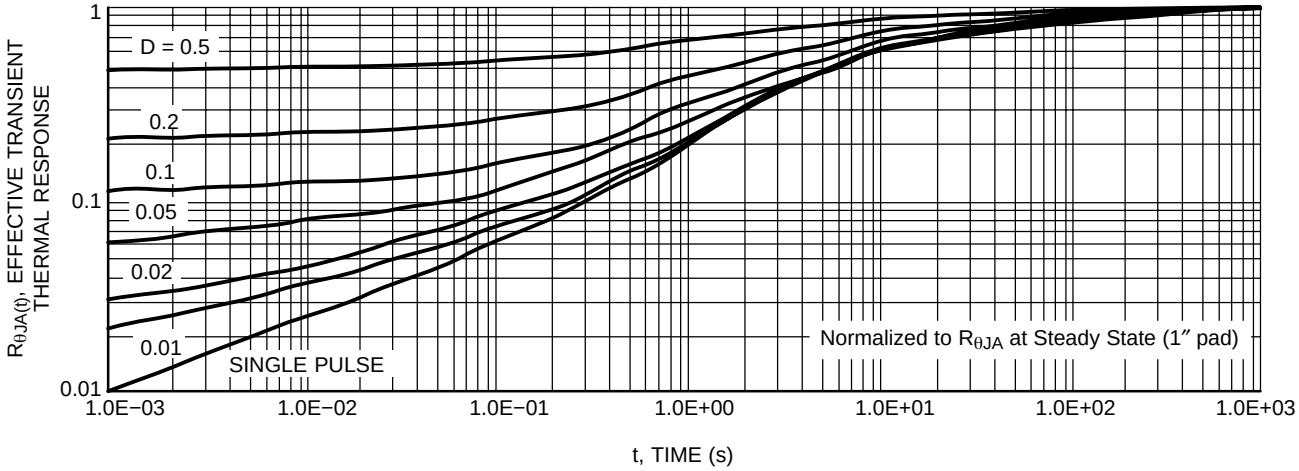


Figure 13. FET Thermal Response

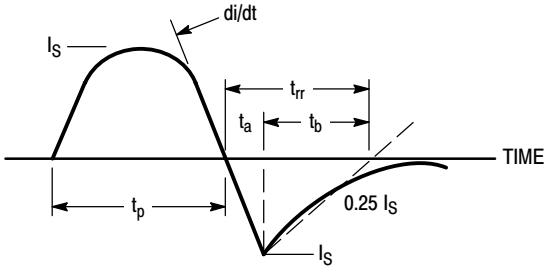
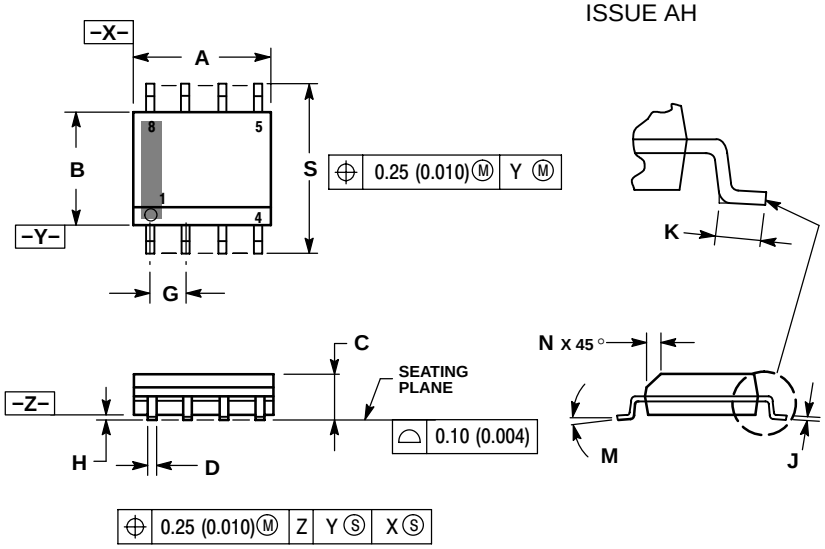


Figure 14. Diode Reverse Recovery Waveform

NIMD6302R2

PACKAGE DIMENSIONS

SOIC−8
CASE 751−07
ISSUE AH

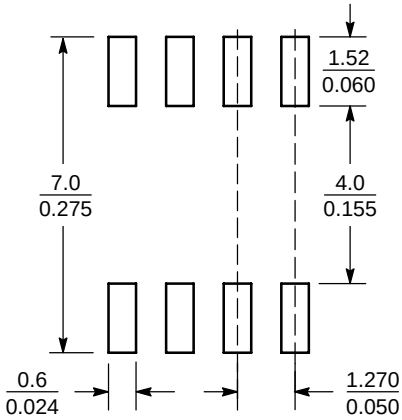


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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