YAMAHA

YSS950

DAP1

Digital Audio Processor

■ Outline

The YSS950 (DAP1) is a DSP (Digital Signal Processor) for sound field processing, which features a high-speed/ high-precision 32-bit floating point DSP.

■ Features

- 32-bit floating point DSP achieves high-speed/high-precision operations
  - Operation frequency: Approximately 166 MHz
  - Data bus width: 32 bits (24-bit mantissa, 8-bit exponent)
  - Multiplier/adder: 32 bits × 32 bits + 55 bits → 55 bits (47-bit mantissa, 8-bit exponent)
- 48 KB (12 Kword) preset command code firmware area
- 24 KB (6 Kword) download command code firmware area (maximum)
- 104 KB (26 Kword) data RAM area (maximum)
- High-speed command code/coefficient data firmware download (burst transfer)
- Download coefficients data firmware without any interruption of sound (runtime transfer)
- Firmware's placement order can be changed
- Firmware's number of execution channels can be changed (up to 16 channels)
- Multiple firmware calls are enabled
- Audio I/O
  - 32 bits × 16 channels, TDM
  - Fixed point decimal format and floating point decimal format (IEEE Standard 754, two's complement)
  - Sampling frequency range is 32 to 192 kHz
  - Audio clock division/switch
  - Input/output muting
  - Input/output channel switching
- External memory not required
- General I/O ports (4)
- On-chip PLL
- Power supply voltage: 1.2 V (core), 3.3 V (pin)
- Low power consumption: Approximately 130mW (typical value)
- Si-gate CMOS process
- Lead-free 64-pin SQFP package (YSS950-SZ)

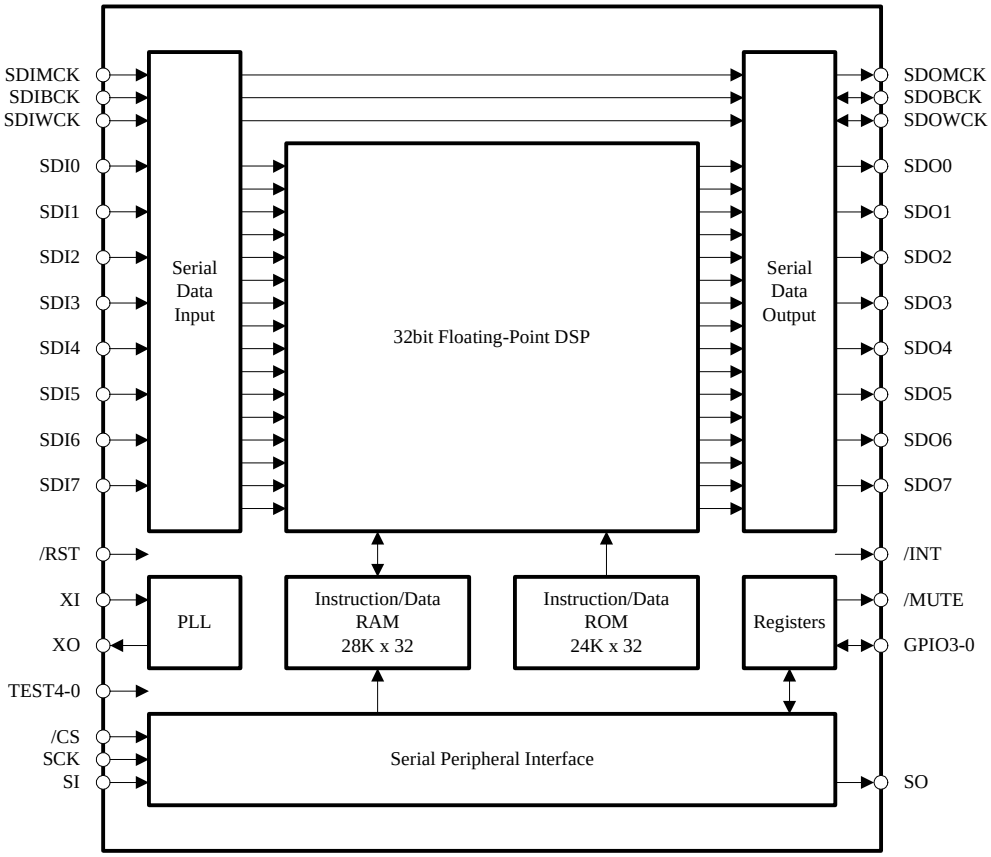
■ Applications

- Home theater systems
- Car audio

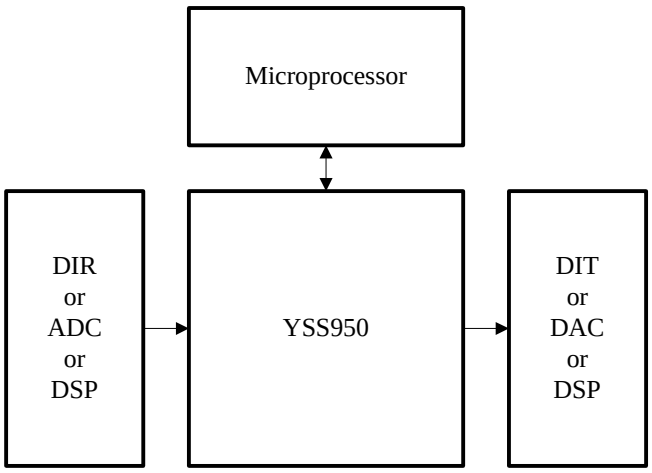
YAMAHA CORPORATION

YSS950 CATALOG
CATALOG No.: LSI-4SS950A22
2006.10

■ Block Diagram



■ System Configuration Example



■ Application Firmware

The application firmware of YSS950(DAP1) provides a variety of functions that can be used in home theater systems, car audio systems, and many other applications. This application firmware can be combined to implement signal flow for up to 16 channels.

Firmware Name	Abbr.	Function
Bass manager	BM	Distributes the optimum low-range signal for the playback environment.
Channel divider	CD	Divides bandwidth for multi-way.
Delay	DLY	Adds delay to individual channels.
Down sampler	DS	Down samples to 1/2.
Dynamic range controller	DRC	Controls dynamic range.
Format converter	FMT	Converts signal format.
Generator	GEN	Generates a noise signal or impulse signal.
High frequency regenerator	HR	Complements high frequency components.
Headphone surround	HS	Reproduces 5.1 channel surround on headphones.
IIR1x2	I12	A cascade of two 1st-order IIR filters.
IIR2x2	I22	A cascade of two 2nd-order IIR filters.
IIR2x3	I23	A cascade of three 2nd-order IIR filters.
IIR2x8	I28	A cascade of eight 2nd-order IIR filters.
Mixer	MIX	Signal gain can be applied freely.
Sound field	SF	Sounds reverb richly.
Virtual surround	VS	Reproduces 5.1 channel surround on only the front speaker.
Volume controller	VOL	Overall and channel-specific volume adjustments.
Acoustic Field Analyzer	AFA	Measurement of audio characteristics. for Automatic Acoustic Field Calibration system.
Dolby Pro Logic II	PLII	Dolby Pro Logic II decoder.
Dolby Pro Logic IIx	PLIIx	Dolby Pro Logic IIx decoder.

・Up to 24 application firmware modules can operate at the same time.

・The information shown above is subject to revision. Check with Yamaha or an authorized sales agency for the latest information before using this product..

■ Development/Evaluation Kits

Development/Evaluation Kits are prepared for the evaluation and the firmware development of YSS950.

Development/ Evaluation Kit Name	Category	Description	
DMB-DAP1	Evaluation Board	Evaluation board.	
		Curcuit_Diagram of evaluation board.	
	Program Tools	EVBDSP	EVBDSP is a control program that controls an evaluation board from a personal computer , via a USB connection. This program can be used to evaluate the YSS950's functions.
		DAP1Mapper	DAP1Mapper is a tool that determines memory map of the YSS950 (DAP1) firmware.
		Fltcnvc	Fltcnvc is a command line tool that converts tool between two's complement floating point format and real number format.
		iirdgn	iirdgn is a command line tool that calculates the coefficients of typical IIR filters.
		DRCDesigner	DRCDesigner is an Excel file that is used to create sample files for the dynamic range controller firmware.
		DAP1AFC	The DAP1AFC is a tool that works with firmware (AFA[1]) on the DAP1 evaluation board (hereafter, "evaluation board") to measure audio characteristics at the listening point, and automatically makes calibration to set the specified characteristics.
	Application Firmware	BM	
		CD	
		DLY	
		DS	
		DRC	
		FMT	
		GEN	
		HR	
		HS	
		I12	
		I22	
		I23	
		I28	
		MIX	
		SF	
		VS	
		VOL	
		AFA	
AS-DAP1-PLII	Application Firmware	PLII	
AS-DAP1-PLIIx	Application Firmware	PLII	
AS-DAP1-AFA	Automatic Acoustic Field Calibration system	Automatic Acoustic Field Calibration Coefficient Calculation Program.	
		AFA	The same as firmware AFA included in DAP1AFC.

[Caution]
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[Caution]
"Dolby", "Dolby Pro Logic II", and "Dolby Pro Logic IIx" are trademarks of Dolby Laboratories.
"DTS", "DTS-ES", "DTS-96/24", and "DTS Neo:6" are trademarks of Digital Theater Systems, Inc.

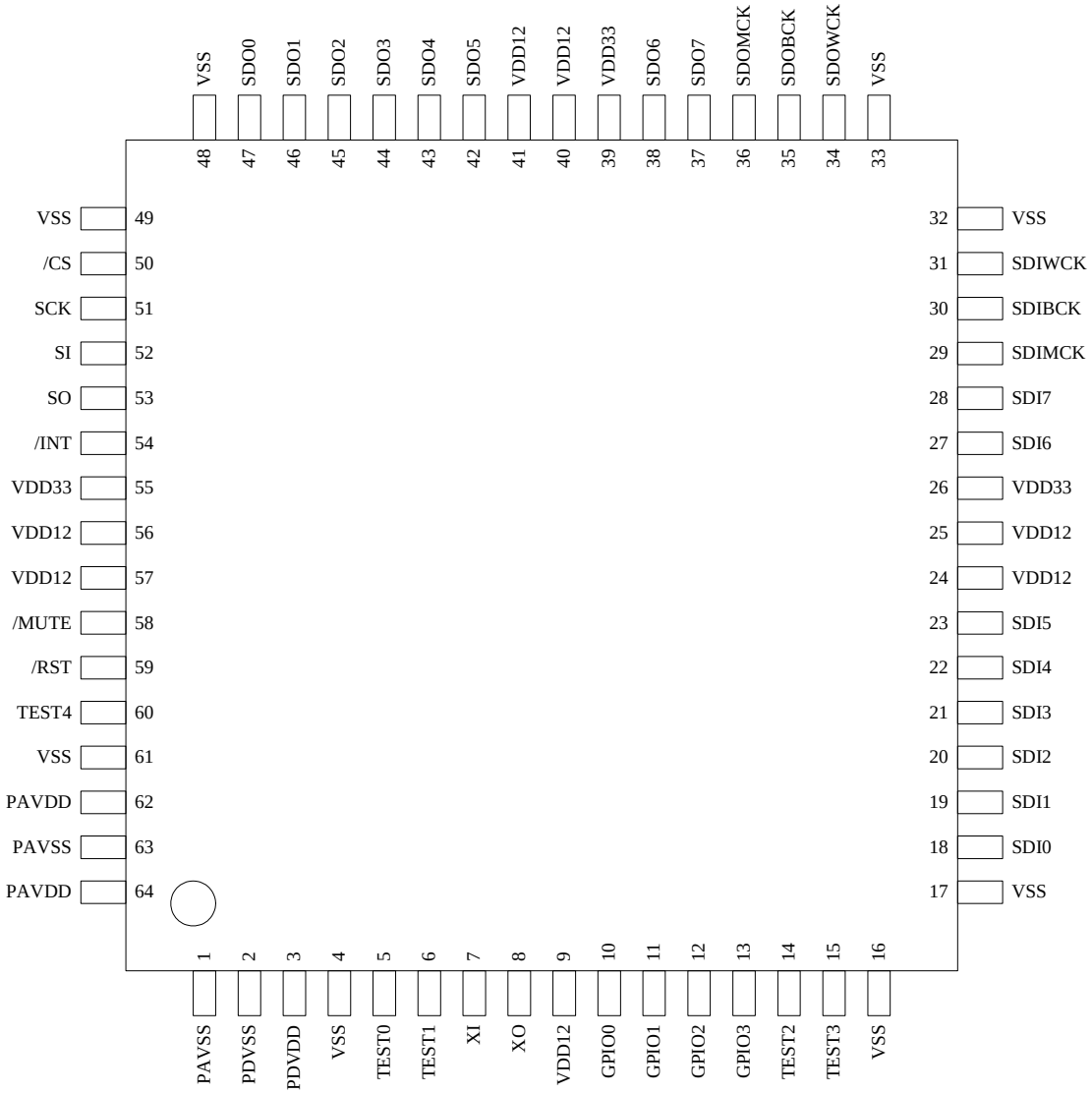
[1] AFA: Acoustic Field Analyzer

■ Comparison of Yamaha audio DSP

	Chip Name / Function	DAP1	ADAMB			EVE
		YSS950	YSS944	YSS943	YSS940	YSS920B
Firmware	Dolby digital decoding	N	Y			N
	Dolby Digital EX decoding	N	Y			N
	AAC decoding	N	Y			N
	PCM input playback	Y (up to 16 channels)	Y (up to 8 channels)			Y (up to 16 channels)
	Dolby Pro Logic II decoding	Y	Y			N
	Dolby Pro Logic IIx decoding	Y	Y			N
	DTS decoding	N	Y	Y	N	N
	DTS 96/24 decoding	N	Y	Y	N	N
	DTS-ES decoding	N	Y	N	N	N
	DTS Neo:6 decoding	N	Y	N	N	N
	Tone control	Y	Y			Y
	Bass management	Y	Y			Y
	Volume adjustment	Y	Y			Y
	Noise generation	Y	Y			Y
	Impulse generation	Y	Y			Y
	Dynamic range controller	Y	Y			Y
	Harmonics regenerator	Y	N			N
	Nch surround	Y (Mixer)	Y			Y(Channel Distributor)
	Sound field	Y	Y			Y
	Virtual surround	Y	Y			Y
	Headphone surround	Y	Y			N
	Parametric equalizer	Y (8ch x 8Band x X)	Y (8ch x 5Band)			Y (5ch x 3Band)
	Graphic equalizer	Y (PEQ implementation)	Y (PEQ implementation)			Y(2ch x 10band)
	Channel divider	Y	Y			Y
	Automatic acoustic calibration	Y	Y			N
	Down mixing	Y (Mixer)	Y			Y
	Mixer	Y	N			Y
	Down sampling	Y (16 channels)	Y (2 channels)			N
	Modification of firmware placement	Y	N			N
	Multiple firmware calls	Y	N			N
	User programmability	Y (design with module)	N			Y(design with assembler)
	Precision of calculations	Internal data bus:32-bit floating point (24-bit mantissa, 8-bit exponent), Coefficient : 32-bit floating point				Internal data bus:32-bit floating point (28-bit mantissa, 4-bit exponent), Coefficient : 16-bit fixed point
Hardware	Microcontroller interface	Four-wire serial interface				
	Firmware download	Y	Y			Y
	Digital audio interface	24 bits (fixed) or 32 bits (floating) × 16 channels, TDM (4 channels or 8 channels) is enabled	24 bits (fixed) ×8 channels			24 bits (fixed) or 32 bits (floating) × 16 channels
	Audio data channel switching control	Y (input and output)	Y (output)			N
	Bypass	Y	Y			Y (realize by firmware)
	User mute	Y (input and output)	Y (output)			Y (output)
	External memory interface	N	SRAM (4Mbit)			DRAM or SRAM (4Mbit)
	Input delay (lip sync)	Y	Y			Y
	Output delay	Y	Y			Y
	Stream detection	N	Y			N
	Auto mute	Y	Y			N
	Status port	Auto mute, interrupt	Zero detection, auto mute, interrupt			Zero detection, etc
	General-purpose I/O ports	4	8			20
	Internal operation clock generator	Y	Y			Y
	Power-up/power-down	Y	Y			N
	Operation frequency	165.888 MHz	178.176MHz			50MHz
	Power supply voltage	1.2V (core), 3.3V (pin)				2.5V (core), 3.3V (pin)
	Power consumption (Typ.)	130 mW	211mW (Dolby Digital decoding)			165mW
	Package	SQFP64	LQFP144			SQFP100
	Lead-free	Y	Y			Y

[Caution]

■ Pin Configuration



< 64-pin SQFP top view >

■ Pin Function List

Type	Pin No.	Pin Name	I/O Note 1)	Function
Serial peripheral interface (SPI)	50	/CS	Is	SPI chip select input
	51	SCK	Is	SPI clock input
	52	SI	I	SPI address/data input
	53	SO	Ot	SPI data output Connect this pin to a pull-up resistor.
Serial data interface	29	SDIMCK	Is	Master clock input
	30	SDIBCK	Is	Bit clock input for serial data input
	31	SDIWCK	I	Word clock input for serial data input
	18	SDI0	I	Serial data input Connect unused pins to a ground.
	19	SDI1		
	20	SDI2		
	21	SDI3		
	22	SDI4		
	23	SDI5		
	27	SDI6		
	28	SDI7		
	36	SDOMCK	Ot	Master clock output
	35	SDOBCK	Is/O	Bit clock I/O for serial data output Input during slave mode and output during master mode.
	34	SDOWCK	I/O	Word clock I/O for serial data output Input during slave mode and output during master mode.
	47	SDO0	O	Serial data output Connect unused pins to a ground.
	46	SDO1		
	45	SDO2		
	44	SDO3		
	43	SDO4		
	42	SDO5		
	38	SDO6		
	37	SDO7		
Status	54	/INT	O	Interrupt report output
	58	/MUTE	O	Auto mute report output
General-purpose I/O ports	10	GPIO0	I+/O	General-purpose I/O ports Register settings are used to switch between input and output mode. Pull-up during input, no pull-up during output. Connect unused pins to a ground.
	11	GPIO1		
	12	GPIO2		
	13	GPIO3		
System	59	/RST	Is	Hardware reset input This LSI is initialized when at low level.
	7	XI	I	Clock input Connect this pin to a 12.288 MHz crystal oscillator, such as in the part of the circuit example indicated by Note 2. If a crystal oscillator has not been connected, input a 12.288 MHz clock to the XI pin.
	8	XO	O	Clock output Connect as shown by Note 2 in the circuit example. If inputting a clock directly to the XI pin (without connecting a crystal oscillator), do not connect anything to the XO pin. Do not use the XO pin for any purpose other than clock oscillation.
Test	5	TEST0	Is	Test input Connect to a ground.
	6	TEST1		
	14	TEST2		
	15	TEST3		
	60	TEST4		

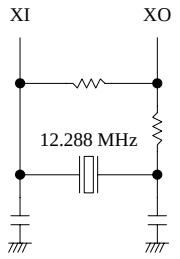
Type	Pin No.	Pin Name	I/O Note 1)	Function
Power supply	26	VDD33	–	Digital power supply for pin block (Typ. 3.3 V)
	39			
	55			
	9	VDD12	–	Digital power supply for Core block (Typ. 1.2 V)
	24			
	25			
	40			
	41			
	56			
	57			
	62	PAVDD	–	Power supply for PLL analog block (Typ. 1.2 V) Insert a 0.1 μF capacitor between the PAVDD and PAVSS pins.
	64			
	3	PDVDD	–	Power supply for PLL digital block (Typ. 1.2 V) Insert a 0.1 μF capacitor between the PDVDD and PDVSS pins.
	4	VSS	–	Digital ground
	16			
	17			
	32			
	33			
	48			
	49			
	61			
	1	PAVSS	–	PLL analog ground Insert a 0.1 μF capacitor between the PAVDD and PAVSS pins.
	63			
	2	PDVSS	–	PLL digital ground Insert a 0.1 μF capacitor between the PDVDD and PDVSS pins.

Note 1) I/O symbols

- I: Input
- Is: Schmitt trigger input
- I+: Built in pull-up circuit (*)
- O: Output
- Ot: 3-state output

* Built in pull-up circuit cannot be used for Hi-level output of the LSI, because of this ability is only keep Hi-level for input pin when it is open.

Note 2) Example of circuit connected to crystal oscillator



* The above resistor and capacitor values vary depending on a crystal oscillator. Be sure to meet the specifications for the crystal oscillator to be used.

■ Register list

Address	Byte Name	Access	Default Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	ChipAdr	R/W	0x00	CAE	0	0	0	CA[3:0]			
0x01	OpMod	R/W	0x00	SWRSTN	PD	0	0	HWRST[3:0]			
0x02	PLL0	R/W	0x36	PLLF[7:0]							
0x03	PLL1	R/W	0x84	PLLOD[1:0]		0	PLLR[4:0]				
0x04	GPIODir	R/W	0x00	0	0	0	0	GPIOD[3:0]			
0x05	GPOSel	R/W	0x00	0	0	0	0	GPOSEL[3:0]			
0x06	GPI	R	Undefined	0	0	0	0	GPI[3:0]			
0x07	GPO	R/W	0x00	0	0	0	0	GPO[3:0]			
0x08	DSPCtl	R/W	0x00	BYPASS	DSPMOD	0	RAMCNFG	0	0	ICHCNFG[1:0]	
0x09	OMA0	R/W	0x00	OMA	0	0	OMAA[20:16]				
0x0A	OMA1	R/W	0x00	OMAA[15:8]							
0x0B	OMA2	R/W	0x00	OMAA[7:0]							
0x0C	RTCtl0	R/W	0x00	RTREQ	0	0	0	0	0	0	0
0x0D	RTCtl1	R/W	0x00	0	0	RTCNT[5:0]					
0x0E	SDIClk	R/W	0x00	0	0	SDIWCKS[1:0]		SDIBCKS[3:0]			
0x0F	SDIFmt0	R/W	0x00	SDITMOD[1:0]		SDITFMT[1:0]		SDIBIT[1:0]		SDIWCKP	SDIBCKP
0x10	SDIFmt1	R/W	0x00	SDI3DFMT[1:0]		SDI2DFMT[1:0]		SDI1DFMT[1:0]		SDI0DFMT[1:0]	
0x11	SDIFmt2	R/W	0x00	SDI7DFMT[1:0]		SDI6DFMT[1:0]		SDI5DFMT[1:0]		SDI4DFMT[1:0]	
0x12	SDIMute0	R/W	0x00	SDI3RMTN	SDI3LMTN	SDI2RMTN	SDI2LMTN	SDI1RMTN	SDI1LMTN	SDI0RMTN	SDI0LMTN
0x13	SDIMute1	R/W	0x00	SDI7RMTN	SDI7LMTN	SDI6RMTN	SDI6LMTN	SDI5RMTN	SDI5LMTN	SDI4RMTN	SDI4LMTN
0x14	SDISel0	R/W	0x10	SDI01SEL[3:0]				SDI00SEL[3:0]			
0x15	SDISel1	R/W	0x32	SDI03SEL[3:0]				SDI02SEL[3:0]			
0x16	SDISel2	R/W	0x54	SDI05SEL[3:0]				SDI04SEL[3:0]			
0x17	SDISel3	R/W	0x76	SDI07SEL[3:0]				SDI06SEL[3:0]			
0x18	SDISel4	R/W	0x98	SDI09SEL[3:0]				SDI08SEL[3:0]			
0x19	SDISel5	R/W	0xBA	SDI11SEL[3:0]				SDI10SEL[3:0]			
0x1A	SDISel6	R/W	0xDC	SDI13SEL[3:0]				SDI12SEL[3:0]			
0x1B	SDISel7	R/W	0xFE	SDI15SEL[3:0]				SDI14SEL[3:0]			
0x1C	SDOClk0	R/W	0x00	SDOMCKD	0	0	0	0	SDOMCKS[2:0]		
0x1D	SDOClk1	R/W	0x00	SDOBWCKD	0	SDOWCKS[1:0]		SDOBCKS[3:0]			
0x1E	SDOFmt0	R/W	0x00	SDOTMOD[1:0]		SDOTFMT[1:0]		SDOBIT[1:0]		SDOWCKP	SDOBCKP
0x1F	SDOFmt1	R/W	0x00	SDO3DFMT[1:0]		SDO2DFMT[1:0]		SDO1DFMT[1:0]		SDO0DFMT[1:0]	
0x20	SDOFmt2	R/W	0x00	SDO7DFMT[1:0]		SDO6DFMT[1:0]		SDO5DFMT[1:0]		SDO4DFMT[1:0]	
0x21	SDOMute0	R/W	0x00	SDO3RMTN	SDO3LMTN	SDO2RMTN	SDO2LMTN	SDO1RMTN	SDO1LMTN	SDO0RMTN	SDO0LMTN
0x22	SDOMute1	R/W	0x00	SDO7RMTN	SDO7LMTN	SDO6RMTN	SDO6LMTN	SDO5RMTN	SDO5LMTN	SDO4RMTN	SDO4LMTN
0x23	SDOSel0	R/W	0x10	SDO0RSEL[3:0]				SDO0LSEL[3:0]			
0x24	SDOSel1	R/W	0x32	SDO1RSEL[3:0]				SDO1LSEL[3:0]			
0x25	SDOSel2	R/W	0x54	SDO2RSEL[3:0]				SDO2LSEL[3:0]			
0x26	SDOSel3	R/W	0x76	SDO3RSEL[3:0]				SDO3LSEL[3:0]			
0x27	SDOSel4	R/W	0x98	SDO4RSEL[3:0]				SDO4LSEL[3:0]			
0x28	SDOSel5	R/W	0xBA	SDO5RSEL[3:0]				SDO5LSEL[3:0]			
0x29	SDOSel6	R/W	0xDC	SDO6RSEL[3:0]				SDO6LSEL[3:0]			
0x2A	SDOSel7	R/W	0xFE	SDO7RSEL[3:0]				SDO7LSEL[3:0]			
0x2B	IMsk	R/W	0x00	IMSERR	0	IMMTBEG	IMMTEND	IMFW[3:0]			
0x2C	IReq	R/W	0x00	IRSERR	0	IRMTBEG	IRMTEND	IRFW[3:0]			
0x2D	Mute	R/W	0x00	MUTEN	0	0	0	0	0	SDOMTSET	SDIMTSET
0x2E	SDIFs	R	0x00	SDIFS[7:0]							
0x2F	SDOFs	R	0x00	SDOFS[7:0]							

Address	Byte Name	Access	Default Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x30 : 0x38	FWCtl	R/W	0x00	This is used for firmware control. For details, see the firmware manual.							
0x39	OMASum	R/W	0x00	OMASUM[7:0]							
0x3A : 0x79	FWCtl	R/W	0x00	This is used for firmware control. For details, see the firmware manual.							
0x7A	Reserved	R	0x00	0	0	0	0	0	0	0	0
0x7B	Reserved	R	0x00	0	0	0	0	0	0	0	0
0x7C	Reserved	R	0x00	0	0	0	0	0	0	0	0
0x7D	Rserved	R	0x00	0	0	0	0	0	0	0	0
0x7E	DevID0	R	0x09	DEVID[15:8]							
0x7F	DevID1	R	0x50	DEVID[7:0]							

[Note]

	Indicates area that is accessible during the normal operation mode, the software reset mode, and the power-down mode.
	Indicates area that is accessible during the normal operation mode and the software reset mode.
0	Reserved area. When writing, write only “0” to this area. Undefined when read.

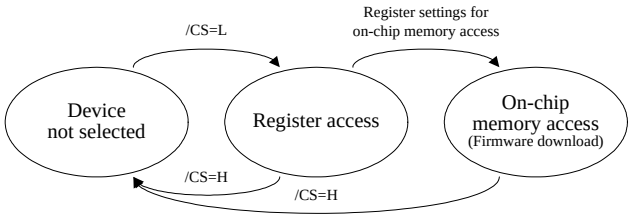
■ FUNCTION DESCRIPTION

（1） Serial Peripheral Interface

This LSI provides a four-wire serial peripheral interface (SPI) for the /CS, SK, SI, and SO pins. The microcontroller accesses the following via this serial peripheral interface

- Register address
- On-chip memory access (firmware download)

The following is a status transition diagram for the serial peripheral interface.

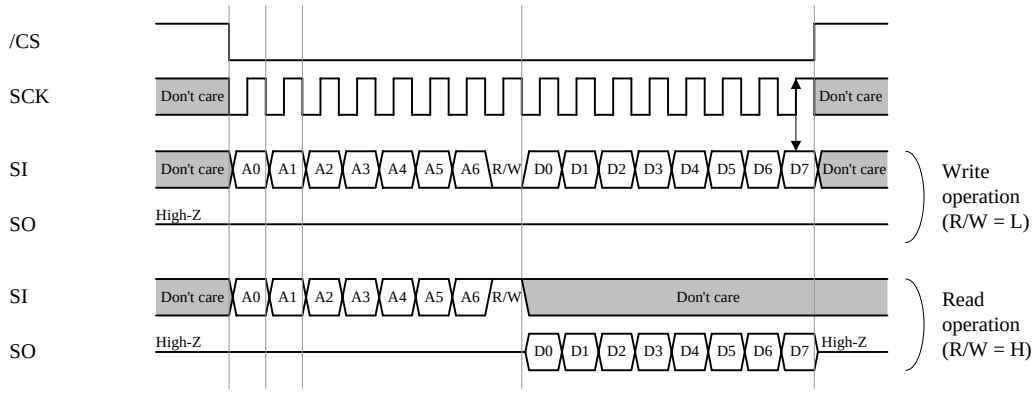


[Note]

In this manual, “register access” is the means of accessing on-chip memory, and should be considered as functionally similar to “firmware download”.

(a) Register access

Register access is performed in 16-bit units via the serial peripheral interface. SI is used to specify the register address (7 bits: A6 to A0) and the read/write setting (1 bit: R/W). During a write operation (R/W = L), data (8 bits: D7 to D0) should be written to SI, and during a read operation (R/W = H), 8-bit data should be read from SO. The write data is stored internally at the rising edge of SCK in the last data bit (D7 in the diagram). The serial peripheral interface sequence during register access is illustrated below.



[Note]

- SO is in output mode only during data read operations when /CS = L. Otherwise, high impedance output is set, so that SCK, SI, and SO can be shared with other devices that have a similar interface.
- Continuous register access is enabled when /CS = L. There is no need to set /CS = H between access times.
- During a hardware reset (/RST = L), keep /CS to high level (/CS = H)..
- If /CS = H is set during register access, access is stopped. Any write operation that occurs prior to the rising edge of the 16th SCK signal (SI’s D7 data capture clock) is invalid. SO is set to high impedance.

(b) On-chip memory access

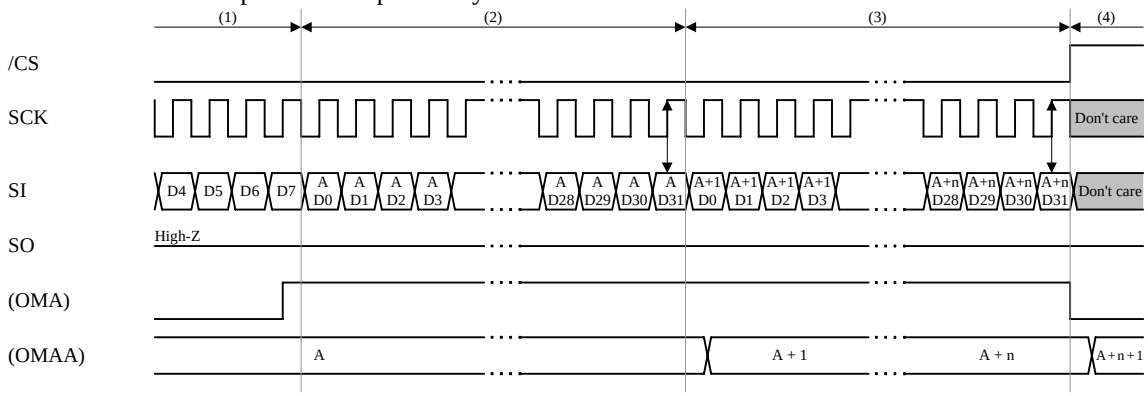
Access to on-chip memory is performed in 32-bit units via the serial peripheral interface. Also, on-chip memory access can be performed with register access. The following describes the two operation modes that are provided for this LSI.

1) Burst transfer mode

Burst transfer mode can be used to download instruction code/coefficient data firmware. By using this mode, a large amount of data can be downloaded at high speeds when initialization is executed or when the sampling frequency is changed. The features of the burst transfer mode are as follows.

- Stops signal processing during high-speed transfers
- Muting is automatically effected during transfer period.
- Transfers from microcontrollers can be accepted immediately, without handshaking
- Both instruction code firmware and coefficient data firmware can be downloaded.

The burst transfer steps for on-chip memory access are illustrated below.



<1> Setup:
- Initialize the checksum as necessary. (OMASUM[7:0]=0)
- Set the on-chip memory access start address (example: OMAA[20:0] = A).
- Change the serial peripheral interface pin function from register access to on-chip memory access (OMA = 1).

<2> Start:
- Data is transferred LSB first, in 32-bit units.
- Data is captured at the rising edge of SCK in the 32nd data bit (D31).

<3> Continuation:
- Next, transfer data at consecutive address in 32-bit units.
- The on-chip memory address (OMAA[20:0]) is automatically incremented each time 32 bits of data are written.

<4> Completion and post-completion processing:
- On-chip memory access ends (OMA = 0) automatically when /CS = H is set.
- OMAA[20:0] is notified of the start address and transfer data number. (E.G. OMAA[20:0]= A+n+1)
- OMASUM[7:0] is notified of the checksum of the transferred data.

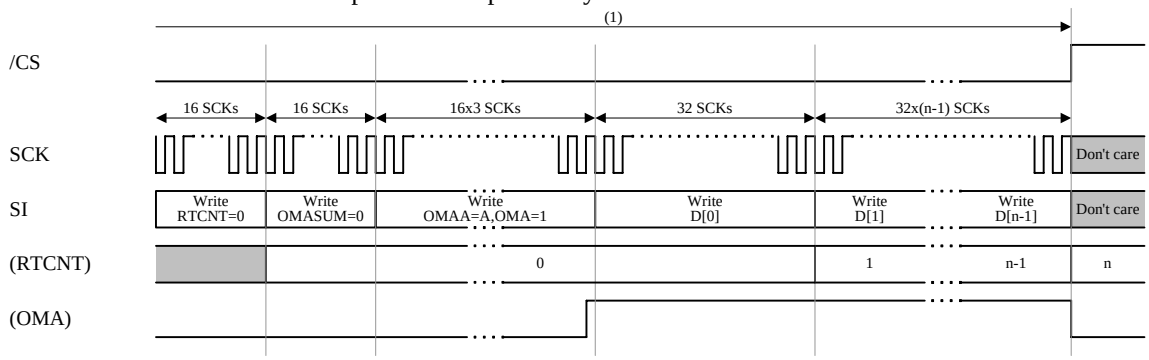
[Note]
- Burst transfer can be interrupted by setting /CS to high level.
  If burst transfer is interrupted before the rising edge of SCK in the 32nd data bit, the write operation is not performed.
- When transferring to non-consecutive addresses or when re-executing after a transfer has been interrupted, start from step (1) above.
- When data is at consecutive addresses, the data at the transfer start address should be transferred with the start bit incremented each time according to the address order.

2) Runtime transfer mode

During runtime transfer mode, coefficient data firmware can be downloaded. This mode enables the coefficient to be changed without jitter, even during signal processing. The runtime processing mode's features are listed below.

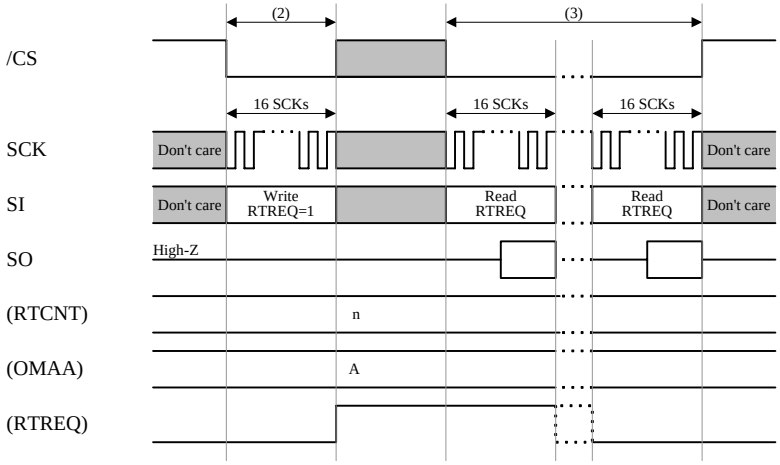
- Transfers are performed while signal processing is continued. Auto mute is not set during the transfer period.
- Up to 32 words of transfer data is buffered and written to on-chip memory as a batch.
- Downloading of coefficient data firmware is supported.

The runtime transfer mode's steps for on-chip memory access are illustrated below.



<1> Setup (transfer to on-chip buffer)

- Initialize the transfer data count (RTCNT[5:0] = 0).
- Initialize the checksum as necessary. (OMASUM[7:0]=0)
- Set the start address for on-chip memory (example: 0MAA[20:0] = A).
- Change the serial peripheral interface's pin function from register access to on-chip memory access (OMA = 1).
- The specified amount of data at consecutive addresses is transferred in 32-bit units, and in LSB first sequence.
- The transfer data count (RTCNT[5:0]) is automatically incremented each time 32 bits of data are written.
- Transfer of data to on-chip buffers ends when /CS = H is set.



<2> Start (transfer from on-chip buffer to on-chip memory)

- Start of data transfer is requested (RTREQ = 1).

<3> End

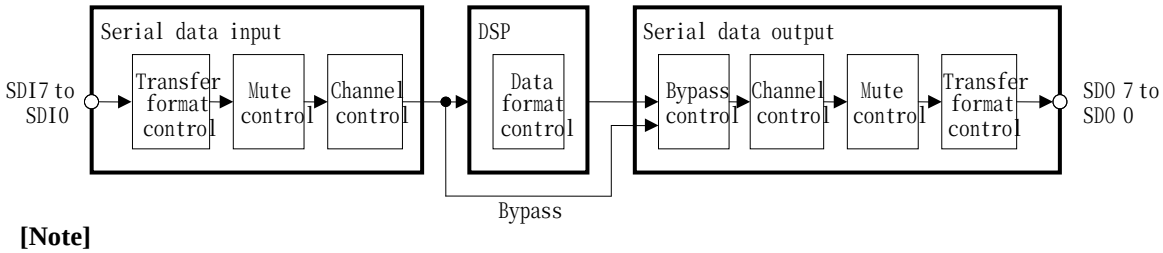
- End of data transfer is confirmed (RTREQ = 0, IRFW[0]=1).
- OMASUM[7:0] is notified of the checksum of the transferred data.

[Note]

- On-chip buffer transfer can be interrupted by setting /CS to high level. If a transfer is interrupted before the rising edge of SCK in the 32nd data bit, the write operation is not performed.
- When transferring to non-consecutive addresses or when re-executing after the on-chip buffer transfer has been interrupted, start from step (1) above.

- When data is at non-consecutive addresses, the data at the transfer start address should be transferred with the start bit incremented each time according to the address order.
- Up to 32 words of data can be transferred as data at consecutive addresses. When transferring more than 32 words of data to consecutive addresses, stop after each 32 words and resume from step (1) above.
- OMAA[20:0] is not automatically incremented.

（2） Serial Data Interface

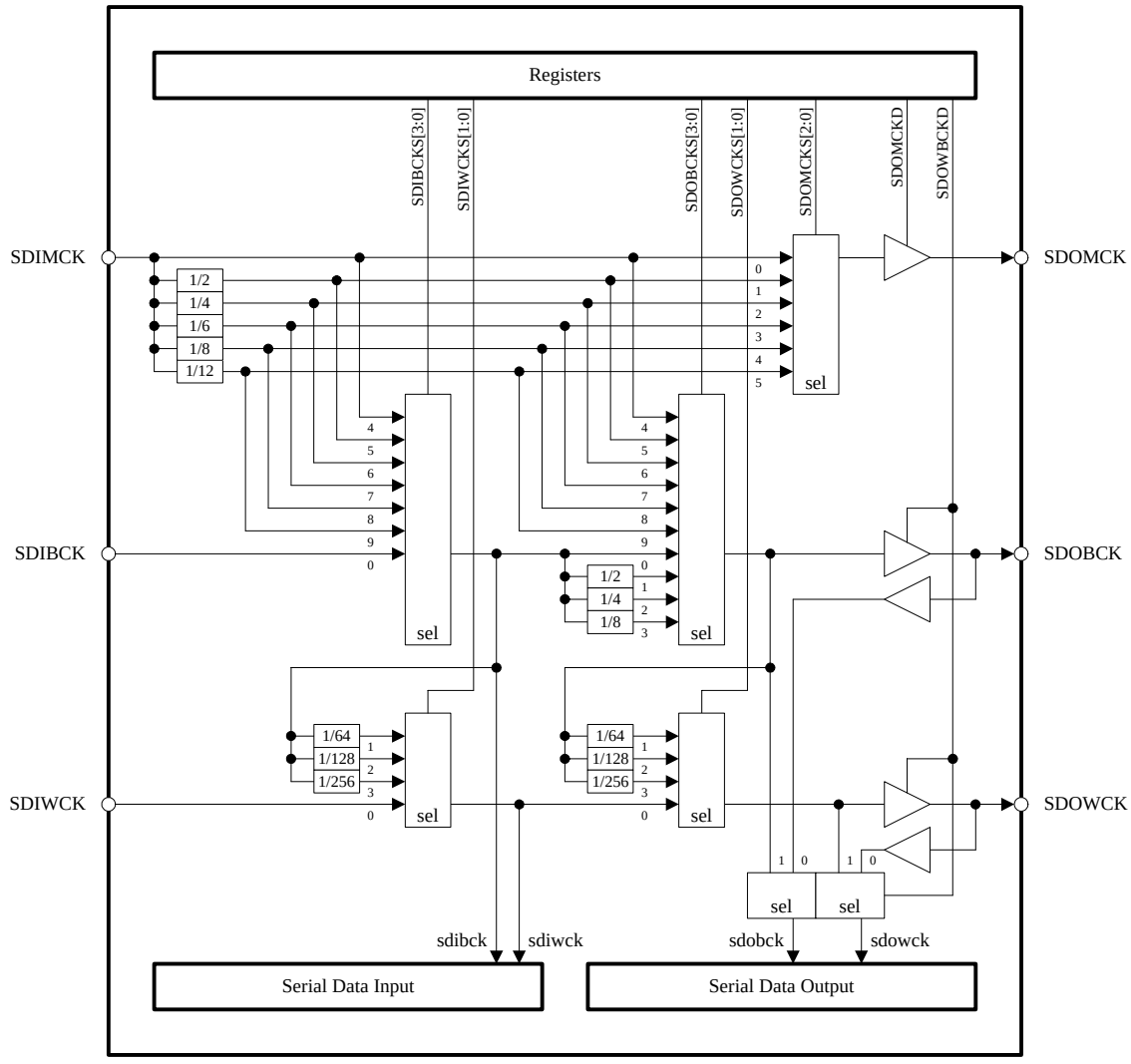


[Note]

The following serial data interface control register (addresses 0x0E to 0x2A, except SD*MTN) and ICHCNFG[1:0] (address 0x08) should be set in the software reset mode. If changes are required when in the normal operation mode, perform the following steps to prevent abnormal sounds.

<1> Set mute (SD*MTN = 1→0, SD*MTSET = 1).
<2> Set the DSP mode to on-chip memory access burst transfer mode (DSPMOD = 1→0).
<3> Set serial data interface control register /ICHCNFG[1:0].
<4> Wait for at least 1024 samples.
<5> Set the DSP mode to signal processing mode (DSPMOD = 0→1).
<6> Cancel mute (SD*MTN = 0→1, SD*MTSET = 1).

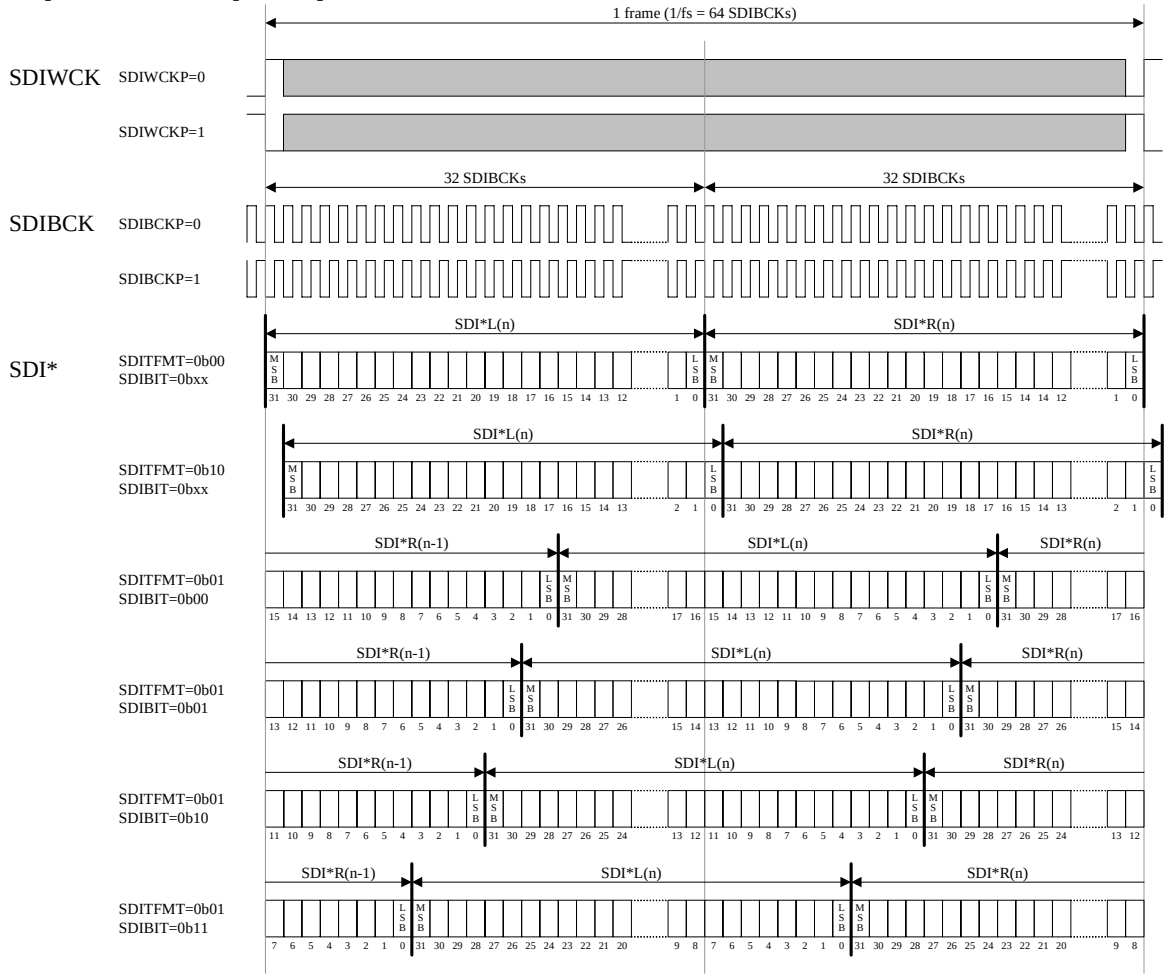
(a) Interface clock control



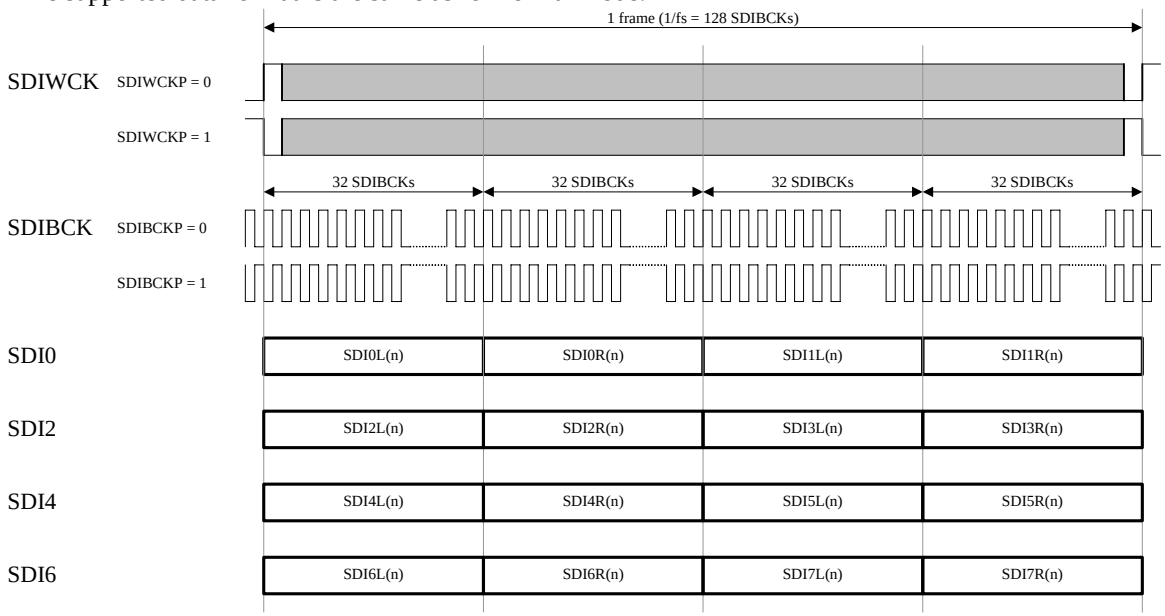
(b) Interface format

1) Input format

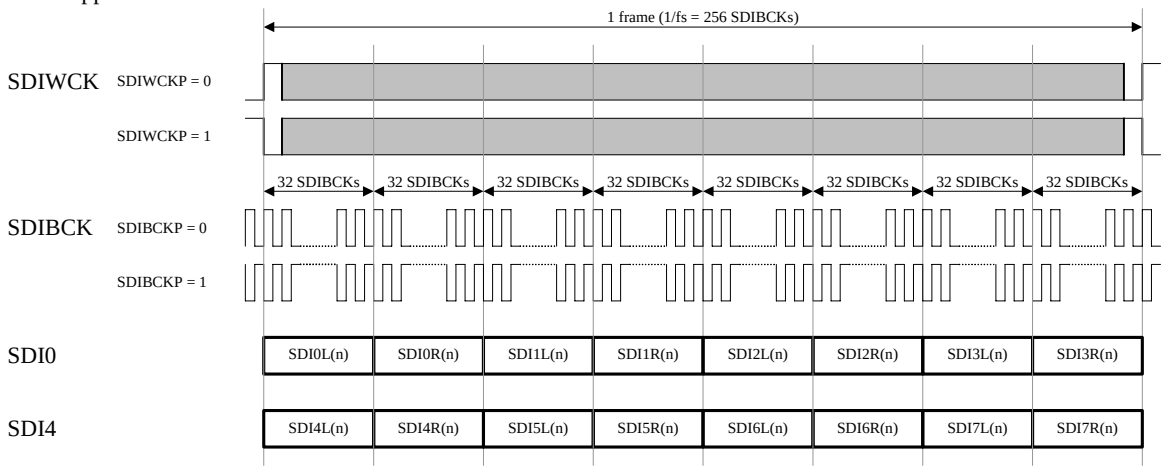
The normal mode timing is illustrated below. 32-bit data can be input via the two channels from SDI0, SDI1, SDI2, SDI3, SDI4, SDI5, SDI6, and SDI7. (n) indicates the current frame input sample and (n – 1) indicates the previous frame input sample.



The TDM 4ch mode timing is illustrated below. 32-bit data can be input via the four channels from SDI0, SDI2, SDI4, and SDI6.
The supported data format is the same as for normal mode.

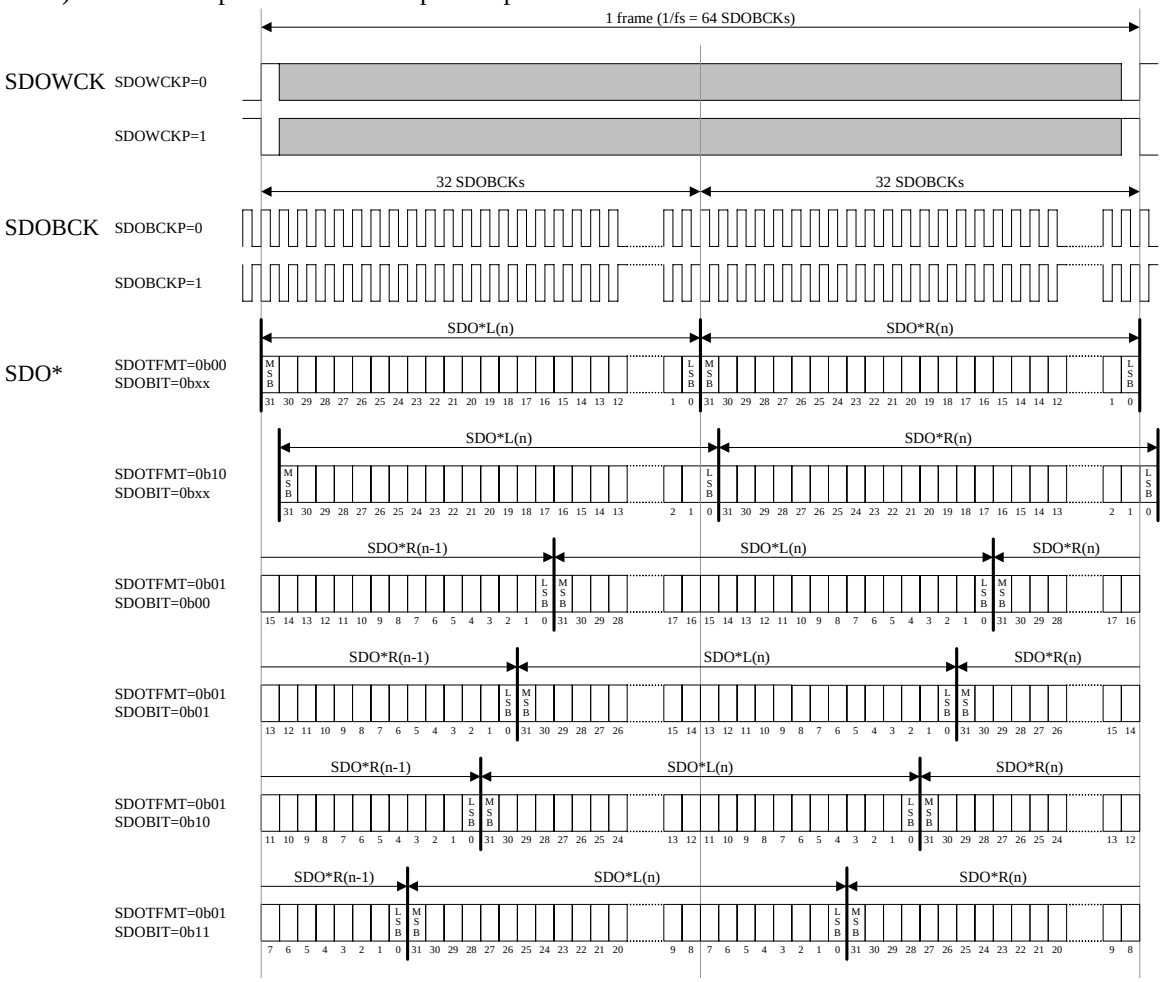


The TDM 8ch mode timing is illustrated below. 32-bit data can be input via the eight channels from SDI0 and SDI4.
The supported data format is the same as for normal mode.

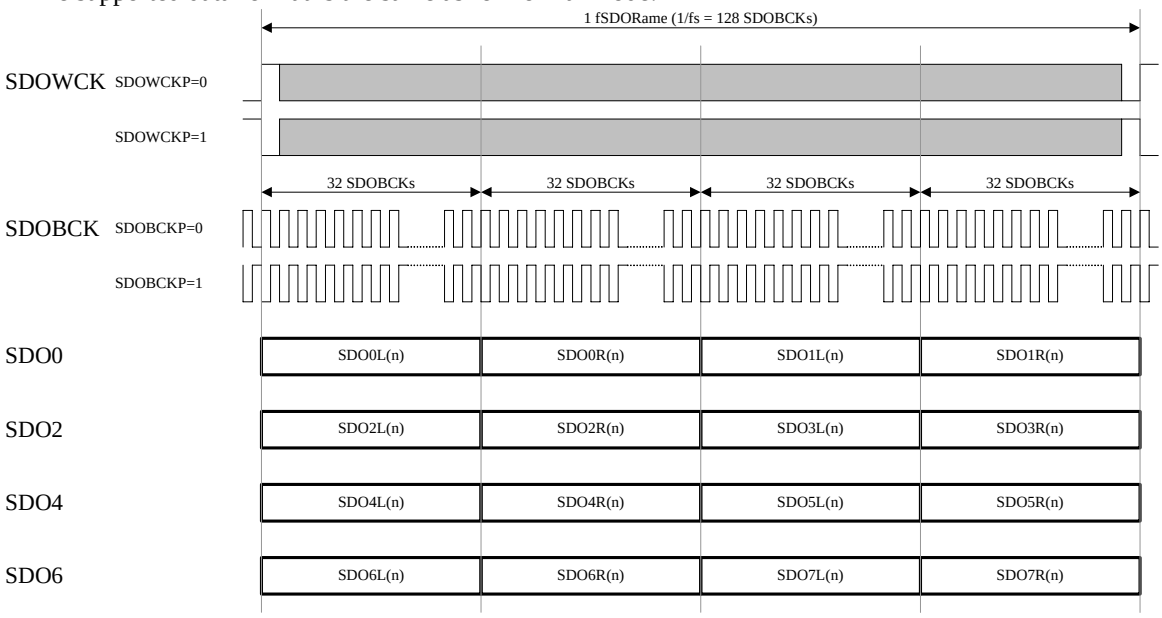


2) Output format

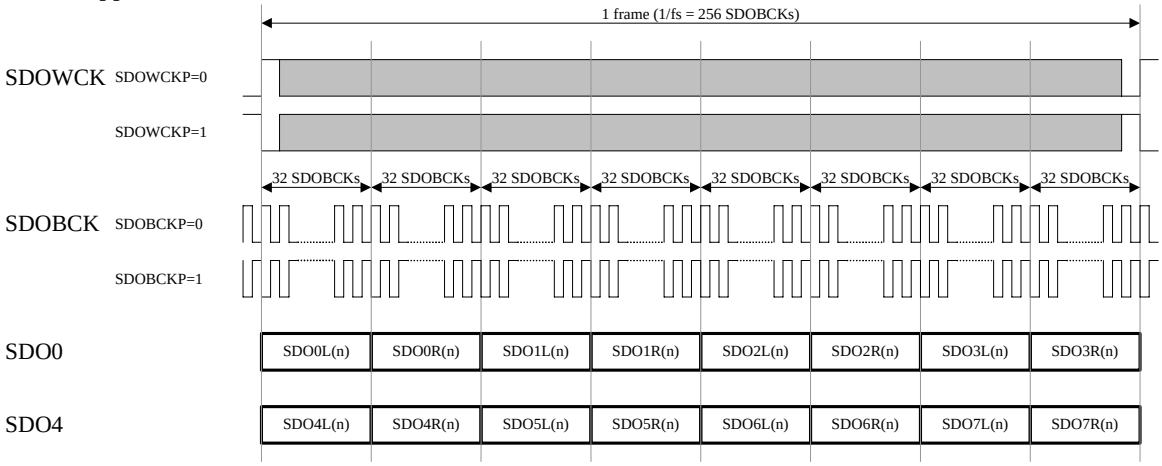
The normal mode timing is illustrated below. 32-bit data can be output via the two channels from SDO0, SDO1, SDO2, SDO3, SDO4, SDO5, SDO6, and SDO7. (n) indicates the current frame input sample and (n – 1) indicates the previous frame output sample.



The TDM 4ch mode timing is illustrated below. 32-bit data can be output via the four channels from SDO0, SDO2, SDO4, and SDO6.
The supported data format is the same as for normal mode.



The TDM 8ch mode timing is illustrated below. 32-bit data can be output via the eight channels from SDO0 and SDO4.
The supported data format is the same as for normal mode.



（3） Status

These informations are notified from LSI.

<1> Interrupt report

<2> Auto mute report

<3> Sampling frequency report

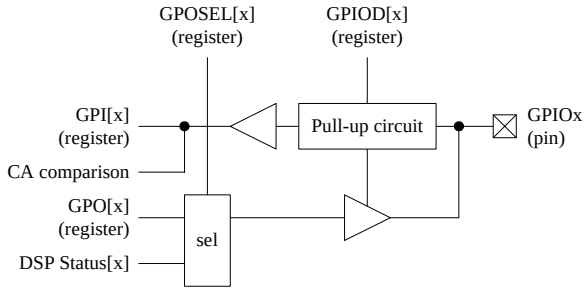
（4） General-Purpose I/O Ports

General-purpose I/O ports GPIO3 to GPIO0 implement the following functions. I/O polarity switching is performed by GPIOD[3:0].

<1> Input port:
Pin status is read via GPI[3:0].

<2> Output port:
GPO[3:0] or DSP status is output to a pin. Switching of output contents is performed by GPOSEL[3:0].

<3> Chip address port:
The port is used as chip address input for selection of a chip to share (CAE=1)..



■ ELECTRICAL CHARACTERISTICS

(1) Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage 1 (3.3 V)	VDD33	**[Note 1]**	–0.5		4.6	V
Power supply voltage 2 (1.2 V)	VDD12	**[Note 1]**	–0.5		1.68	V
	PAVDD	**[Note 1]**				
	PDVDD	**[Note 1]**				
Input voltage 1	V_{I1}	**[Notes 1 and 2]**	–0.5		5.5	V
Input voltage 2	V_{I2}	**[Notes 1 and 3]**	–0.5		4.6	V
Storage temperature	T_{STG}		–50		125	°C

[Note 1] All GND pins (VSS, PAVSS, and PDVSS) are 0 V.
[Note 2] Applies to all input pins other than XI (5 V tolerant).
[Note 3] Applies to the XI pin.

(2) Recommend Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage 1 (3.3 V)	VDD33	**[Note 1]**	3.0	3.3	3.6	V
Power supply voltage 2 (1.2 V)	VDD12	**[Note 1]**	1.1	1.2	1.3	V
	PAVDD	**[Note 1]**				
	PDVDD	**[Note 1]**				
Operating temperature	T_{OP}		–40	25	85	°C

[Note 1] All GND pins (VSS, PAVSS, and PDVSS) are 0 V.

(3) Current Consumption

(a) During normal operation mode

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power consumption	**[Notes 1 and 2]**		130	207	mW
VDD33 current consumption	**[Notes 1 and 2]**		7	10	mA
VDD12 + PAVDD + PDVDD current consumption	**[Notes 1 and 2]**		89	131	mA

[Note 1] Typical values are typical under the recommended operation conditions. Maximum values are maximum values under the recommended operation conditions.
However, the input pin's high-level voltage value is VDD33 and the low-level input voltage value is VSS.
[Note 2] This depends on the sampling frequency and firmware. The firmware used in this case requires a processing load of approximately 150 MHz at a sampling frequency of 48 kHz.

(b) During power-down mode

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power consumption	**[Notes 1]**		1	22	mW
VDD33 current consumption	**[Notes 1]**		6	200	µA
VDD12 + PAVDD + PDVDD current consumption	**[Notes 1]**		1	16	mA

[Note 1] Typical values are typical under the recommended operation conditions. Maximum values are maximum values under the recommended operation conditions.
However, the input pin's high-level voltage value is VDD33 and the low-level input voltage value is VSS.
[Note 2] The current consumption increases at higher temperatures.

(4) DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level input voltage 1	V_{IH1}	**[Note 1]**	2.0		5.25	V
Low level input voltage 1	V_{IL1}	**[Note 1]**			0.8	V
High level input voltage 2	V_{IH2}	**[Note 2]**	0.8VDD33		VDD33	V
Low level input voltage 2	V_{IL2}	**[Note 2]**			0.2VDD33	V
High level output voltage	V_{OH}	**[Note 3]**	2.4			V
Low level output voltage	V_{OL}	**[Note 4]**			0.4	V
Input leakage current 1	I_{I1}	**[Note 5]**			±10	μA
Input leakage current 2	I_{I2}	**[Note 6]**			+10/-125	μA
Capacitance of input pin	C_I			5		pF

[Note 1] Applies to all input pins other than XI (5 V tolerant).
[Note 2] Applies to XI pin.
[Note 3] (Output level is not rated.) Applies to all input pins other than XO. However, IOH = –1.0 mA.
[Note 4] (Output level is not rated.) Applies to all output pins other than XO. However, IOL = 1.0 mA.
[Note 5] Applies to all input pins other than GPIO.
[Note 6] Applies to GPIO pin.

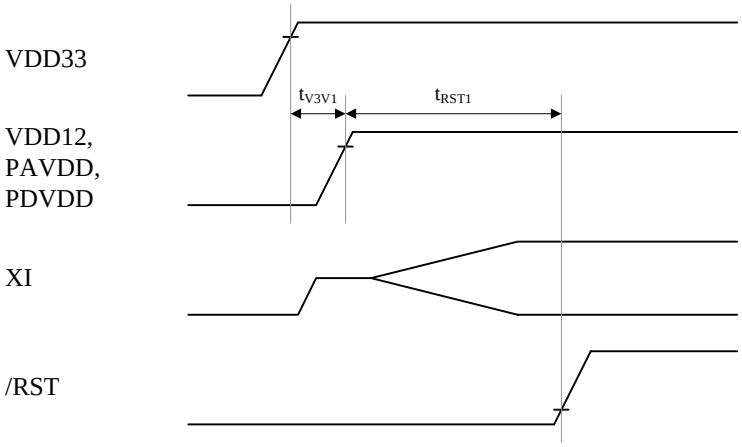
（5） AC Characteristics

(a) System

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power-on and power-off time	t_{V3V1}	**[Note 1]**	–1		1	s
XI clock frequency	f_{XI}			12.288		MHz
XI clock duty factor	d_{XI}		40		60	%
Internal clock frequency	f_{CLK}			165.888		MHz
/RST time 1	t_{RST1}	**At power-on**	5			ms
/RST time 2	t_{RST2}	**During normal operation**	1			μs

[Note 1] The power on/off interval between systems with 3.3 V power supplies and systems with 1.2 V power supplies should be within one second. The LSI can be damaged if either type of power supply is left on while turning on the other.

1) At power-on



- If a crystal oscillator is connected, this includes the time between power supply stabilization and oscillation stabilization.
- Turn on the power when /RST = L.

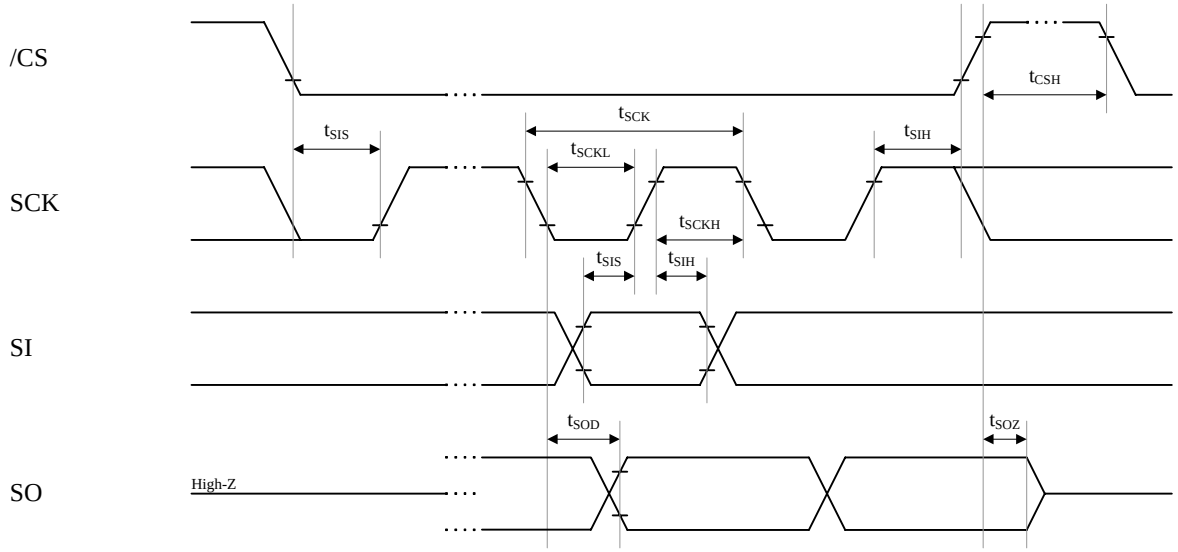
2) During normal operation

- This condition is that both XI input and the power supply must be stabilized.
- If XI oscillation stops while initializing in the power-down mode, some time is needed to stabilize oscillation again.

(b) Serial peripheral interface

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCK cycle	t_{SCK}		80			ns
SCK high level time	t_{SCKH}		40			ns
SCK low level time	t_{SCKL}		40			ns
/CS high level time	t_{CSH}		80			ns
/CS and SI setup time	t_{SIS}	**[Note 1]**	10			ns
/CS and SI hold time	t_{SIH}	**[Note 1]**	10			ns
SO delay time	t_{SOD}	CL = 50 pF			30	ns
SO disable time	t_{SOZ}	CL = 50 pF			20	ns

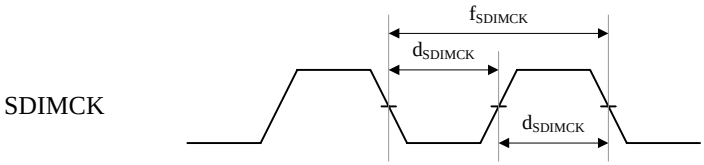
[Note 1] Satisfy the setup time/hold time (vs. SCK) on starting or ending transfer, with /CS = L.



(c) Serial data interface

1) SDIMCK

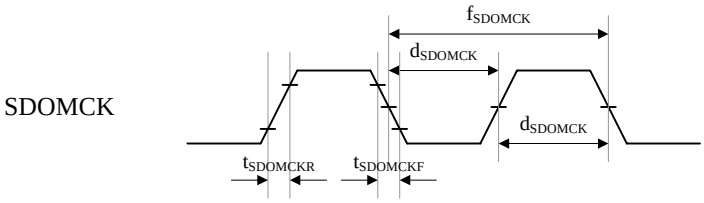
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SDIMCK input frequency	f_{SDIMCK}				40	MHz
SDIMCK duty factor	d_{SDIMCK}			50		%



2) SDOMCK

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SDOMCK output frequency	f_{SDOMCK}				40	MHz
SDOMCK duty factor	d_{SDOMCK}	**[Note 1]**		50		%
SDOMCK rise time	$t_{SDOMCKR}$	CL = 50 pF			10	ns
SDOMCK fall time	$t_{SDOMCKF}$	CL = 50 pF			10	ns

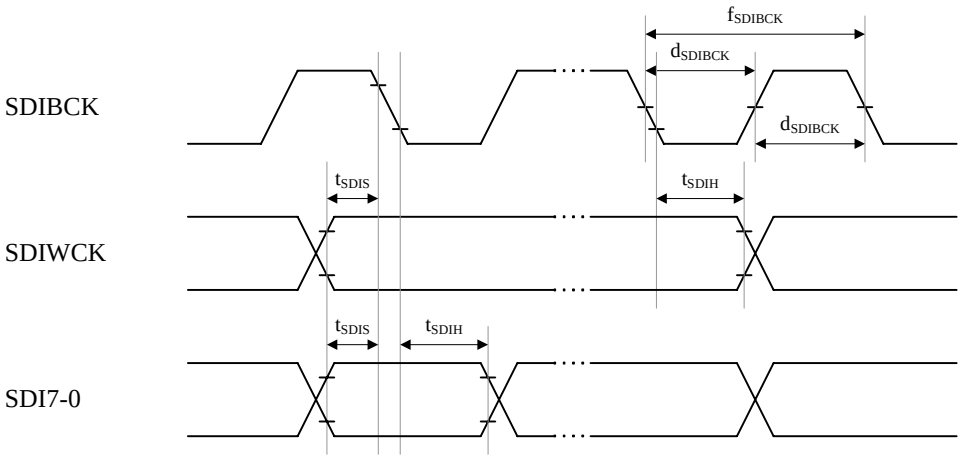
[Note 1] When SDOMCKS[2:0] = 0b00 has been set and "through" has been selected for SDIMCK, it is affected by the SDIMCK duty factor.



3) SDIBCK, SDIWCK, SDI7 to SDI0 (slave mode)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SDIBCK input frequency	f_{SDIBCK}				12.5	MHz
SDIBCK duty factor	d_{SDIBCK}	**[Note 1]**		50		%
SDIWCK, SDI7 to SDI0 setup time	t_{SDIS}		10			ns
SDIWCK, SDI7 to SDI0 hold time	t_{SDIH}		15			ns

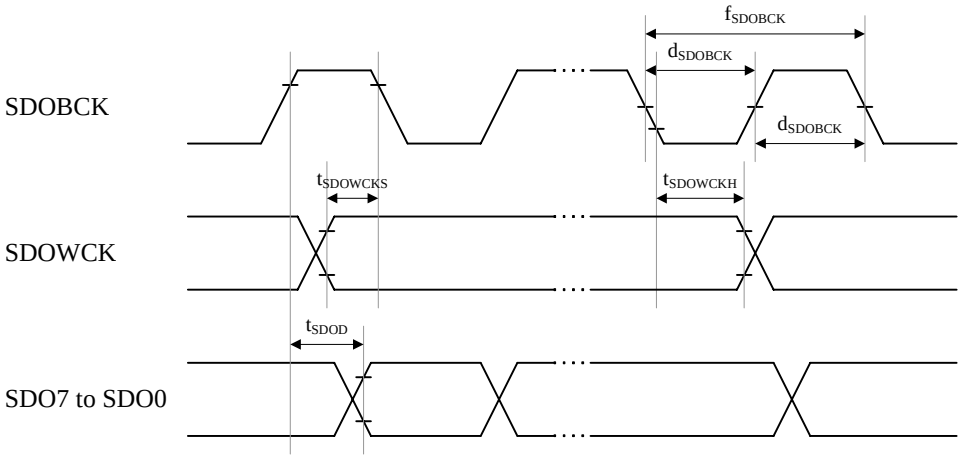
[Note 1] The polarity of SDIBCK can be changed by SDIBCKP. In the following figure, SDIBCKP = 0.



4) SDOBCK, SDOWCK, SDO7 to SDO0 (slave mode)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SDOBCK input frequency	f_{SDOBCK}				12.5	MHz
SDOBCK duty factor	d_{SDOBCK}	**[Note 1]**		50		%
SDOWCK setup time	$t_{SDOWCKS}$		10			ns
SDOWCK hold time	$t_{SDOWCKH}$		10			ns
SDO7 to SDO0 delay time	t_{SDOD}	CL = 50pF			30	ns

[Note 1] The polarity of SDOBCK can be changed by SDOBCKP. In the following figure, SDOBCKP = 0.



5) SDOBCK, SDOWCK, SDO7 to SDO0 (master operation)

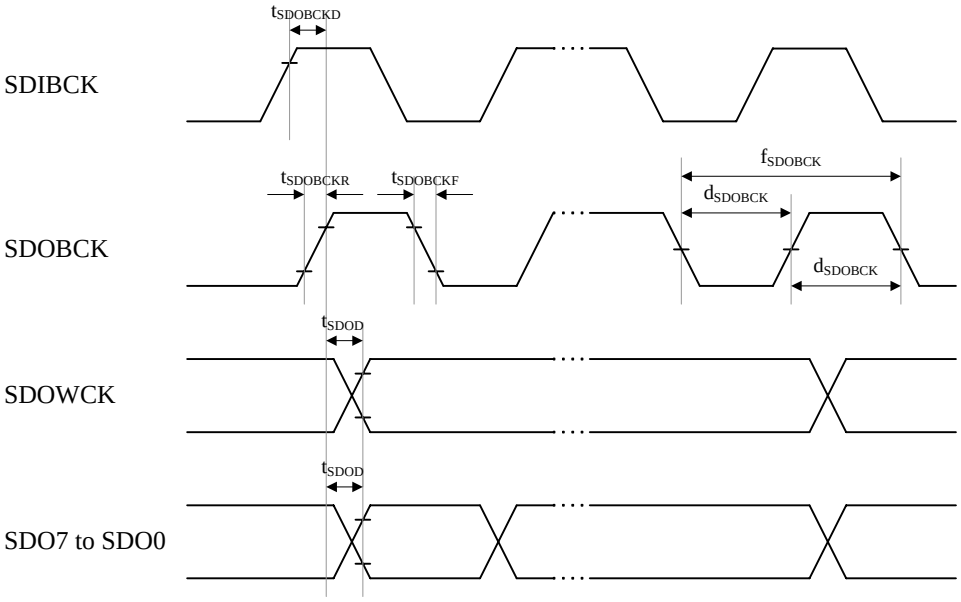
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SDOBCK output frequency	f_{SDOBCK}	**[Note 2]**			12.5	MHz
SDOBCK duty factor	d_{SDOBCK}	**[Note 1, 3]**		50		%
SDOBCK rise time	$t_{SDOBCKR}$	CL = 50 pF			15	ns
SDOBCK fall time	$t_{SDOBCKF}$	CL = 50 pF			15	ns
SDOWCK, SDO7 to SDO0 delay time	t_{SDOD}	CL = 50 pF	–15		15	ns
SDIBCK → SDOBCK delay time	$t_{SDOBCKD}$	CL = 50 pF **[Note 4]**	0		30	ns

[Note 1] The polarity of SDIBCK and SDOBCK can be changed by SDIBCKP and SDOBCKP. In the following figure, SDIBCKP = SDOBCKP = 0.

[Note 2] Although output divided from SDIMCK can be selected for SDOBCK via SDOBCKS[2:0], operation is not guaranteed if SDIMCK's frequency exceeds the range noted above.

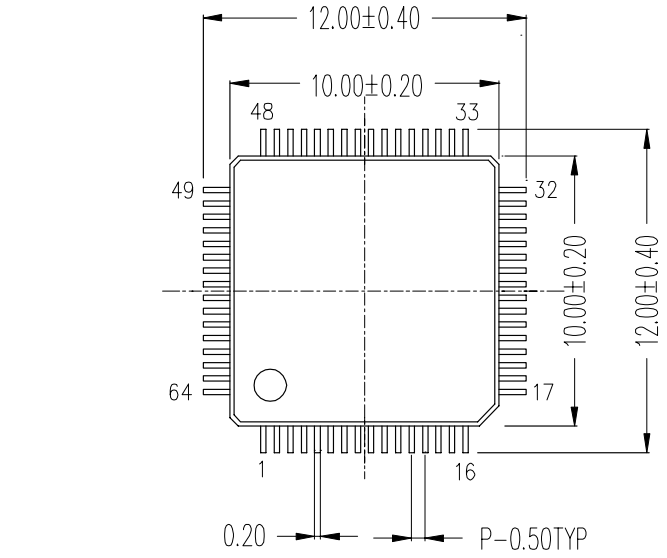
[Note 3] When SDIBCKS through has been selected by SDIBCKS[3:0] = SDOBCKS[3:0] = 0b0000, output is affected by the SDIBCK duty factor.

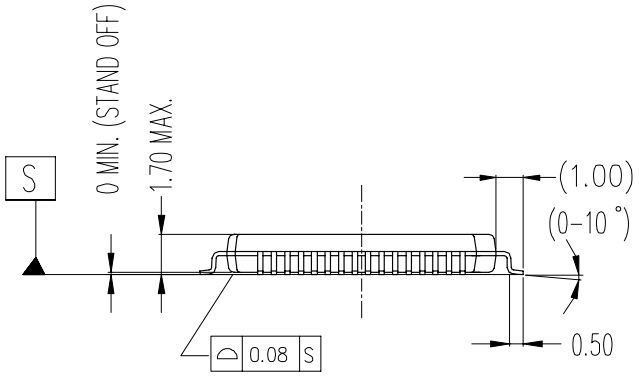
[Note 4] When SDIBCKS through has been selected by SDIBCKS[3:0] = SDOBCKS[3:0] = 0b0000.



■ PACKAGE DIMENSIONS

C-PK64SP-3





端子厚さ/Lead Thickness : 0.145 or 0.17

モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位： mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせください。

Note: The storage and soldering of LSIs for surface mounting need special consideration.
For detailed information, please contact your local Yamaha agent.

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7. INFORMATION DESCRIBED IN THIS DOCUMENT: APPLICATION CIRCUITS AND ITS CONSTANTS AND CALCULATION FORMULAS, PROGRAMS AND CONTROL PROCEDURES ARE PROVIDED FOR THE PURPOSE OF EXPLAINING TYPICAL OPERATION AND USAGE. THEREFORE, PLEASE EVALUATE THE DESIGN SUFFICIENTLY AS WHOLE SYSTEM UNDER THE CONSIDERATION OF VARIOUS EXTERNAL OR ENVIRONMENTAL CONDITIONS AND DETERMINE THEIR APPLICATION AT THE CUSTOMER'S OWN RISK. YAMAHA SHALL ASSUME NO RESPONSIBILITY FOR CLAIMS, DAMAGES, COSTS AND EXPENSES CAUSED BY THE CUSTOMER OR ANY THIRD PARTY, OWING TO THE USE OF THE ABOVE INFORMATION.

Notice The specifications of this product are subject to improvement changes without prior notice.

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