Ordering number : ENA0651

SANYO Semiconductors
DATA SHEET

Bi-CMOS LSI

LV4900HR — Class-D Audio Power Amplifier BTL 10W×2ch

Overview

The LV4900HR is a 10W per channel stereo digital power amplifier that takes analog inputs. The LV4900H uses unique SANYO-developed feedback technology to achieve excellent audio quality despite being a class D amplifier and can be used to implement high quality flat display panel (FDP) based systems.

Features

- Supports circuit designs that do not require output LC filters
- BTL output, class D amplifier system
- Unique SANYO-developed feedback technology achieves superb audio quality
- High-efficiency class D amplifier
- Soft muting function reduces impulse noise at power on/off
- Full complement of built-in protection circuits : overcurrent protection, thermal protection, and low power supply voltage protection circuits
- Built-in bootstrap diodes
- Internal oscillator frequencies : channel 1 = 325kHz, channel 2 = 300kHz

Functions

- 10W output (At VD = 12V, R_L = 8Ω, THD + N = 10%)
- 15W output (At VD = 12V, R_L = 4Ω, THD + N = 10%)
- Efficiency : 88% (VD = 12V, R_L = 8Ω, fin = 1kHz, P_O = 10W)
- Low THD + N : 0.15% (VD = 12V, R_L = 8Ω, fin = 1kHz, P_O = 1W, Filter : AES17)
- Noise : 100μVrms (Filter : A-weight)

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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VD	Externally applied voltage	15	V
Maximum output current	I_O peak		3.75	A/ch
Allowable power dissipation	Pd max	Independent package	886	mW
Operating temperature	Topr		-25 to +75	°C
Storage temperature	Tstg		-50 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Recommended supply voltage range	VD	Externally applied voltage	10	12	14	V
Recommended load resistance	R_L	Speaker load	4	8		Ω

Electrical Characteristics at Ta = 25°C, VD = 12V, R_L = 8Ω, L = 22μH, C = 0.33μF

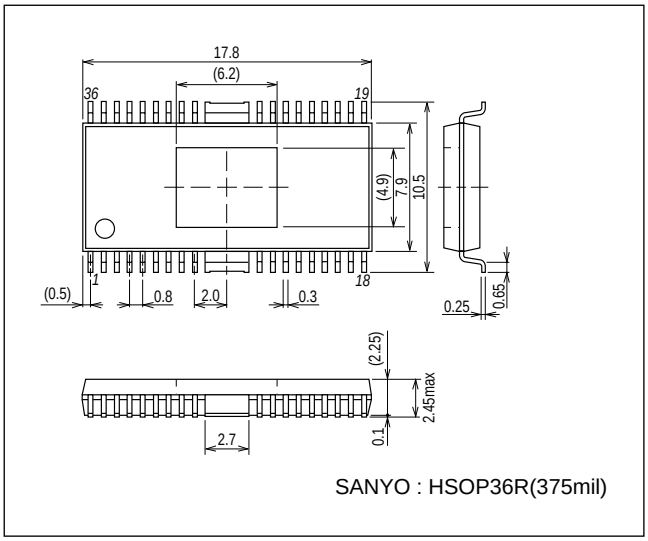
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby current	Ist	$\overline{STBY}$ = L, $\overline{MUTE}$ = L		13	25	μA
Muting current	Imute	$\overline{STBY}$ = H, $\overline{MUTE}$ = L		13.5	20	mA
Quiescent current	I_{CCO}	$\overline{STBY}$ = H, $\overline{MUTE}$ = H		60	70	mA
Voltage gain	VG	fin = 1kHz, V_O = 0dBm	27	29	31	dB
Output offset voltage	Voffset	Rg = 0	-150		150	mV
Total harmonic distortion	THD@1W	P_O = 1W, fin = 1kHz, AES17		0.15	0.5	%
Maximum output	P_O1@10%	THD+N = 10%, AES17	8	10		W
Channel separation	CH sep.	Rg = 0, V_O = 0dBm, DIN AUDIO	55	70		dB
Ripple rejection ratio	SVRR	fr = 100Hz, Vr = 0dBm, Rg = 0, A-weight	50	65		dB
Noise	V_{NO}	Rg = 0, A-weight		100	300	μVrms
High-level output voltage	V_{IH}	STBY pin and MUTE pin	3			V
Low-level output voltage	V_{IL}	STBY pin and MUTE pin			1	V
Power supply voltage drop protection circuit upper limit value	UV_UPPER	VD pin voltage monitor		8.0		V
Power supply voltage drop protection circuit lower limit value	UV_LOWER	VD pin voltage monitor		7.0		V

Note : The values of these characteristics were measured in the SANYO test environment. The actual values in an end system will vary depending on the printed circuit board pattern, the external components actually used, and other factors.

Package Dimensions

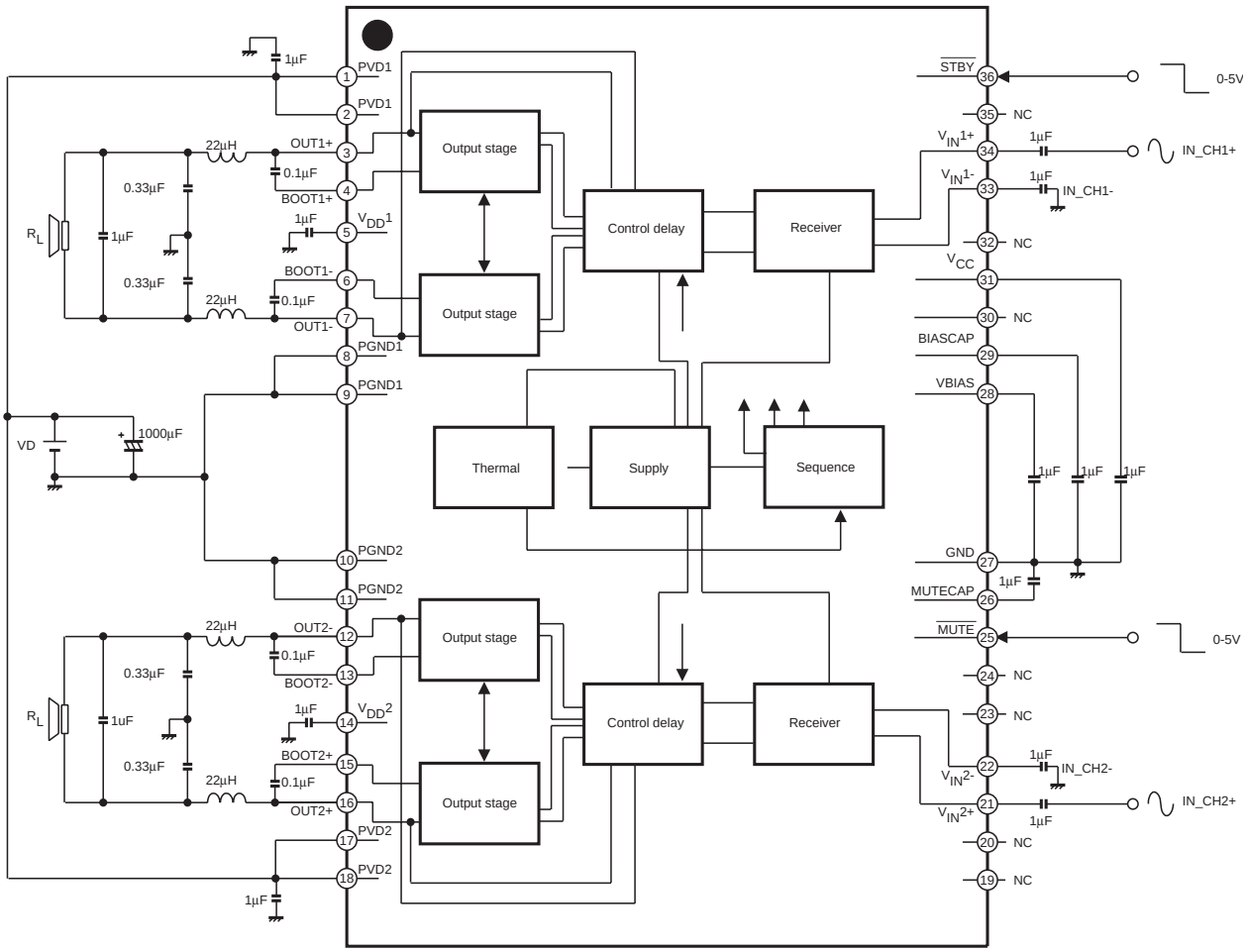
unit : mm (typ)

3251

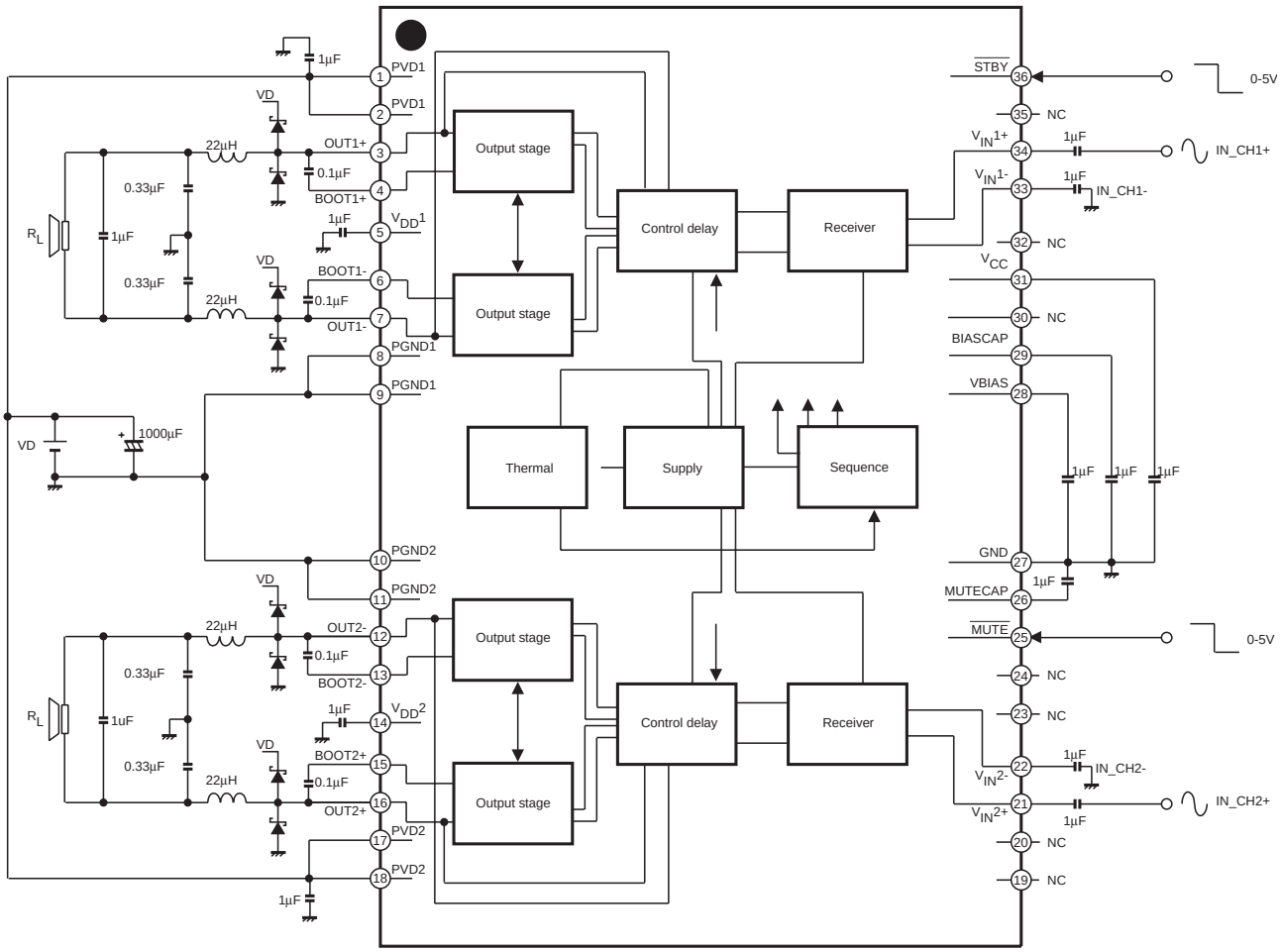


SANYO : HSOP36R(375mil)

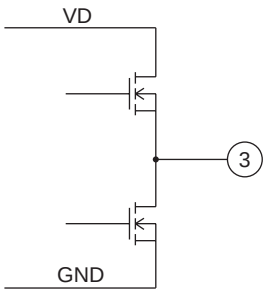
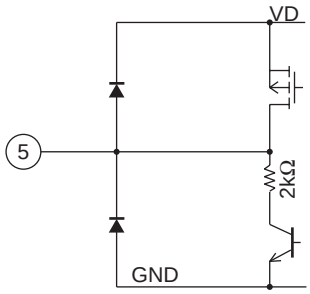
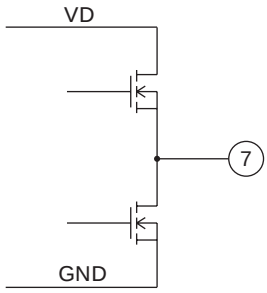
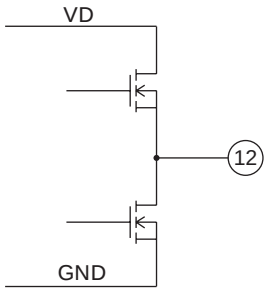
Block Diagram and Application Circuit Example 1 ($R_L = 8\Omega$)



Application Circuit Example 2 (R_L = 4Ω)



Pin Equivalent Circuit

Pin No.	Pin	I/O	Description	Equivalent Circuit
1	PVD1		Channel 1 power system power supply	
2	PVD1		Channel 1 power system power supply	
3	OUT1+	O	Channel 1 high side output	
4	BOOT1+	I/O	Bootstrap I/O pin, channel 1 power supply high side	
5	$V_{DD}1$	O	Internal power supply decoupling capacitor connection	
6	BOOT1-		Bootstrap I/O pin, channel 1 power supply low side	
7	OUT1-	O	Channel 1 low side output	
8	PGND1		Channel 1 power system ground	
9	PGND1		Channel 1 power system ground	
10	PGND2		Channel 2 power system ground	
11	PGND2		Channel 2 power system ground	
12	OUT2-	O	Channel 2 low side output	
13	BOOT2-	I/O	Bootstrap I/O pin, channel 2 power supply low side	

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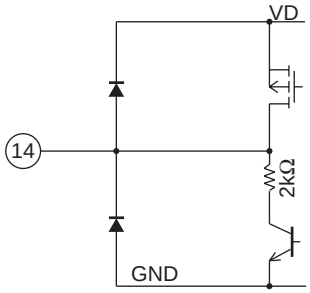
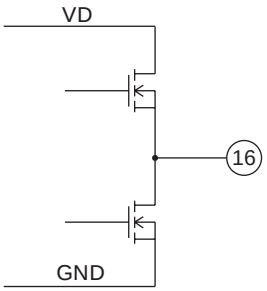
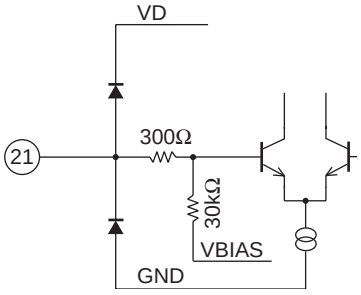
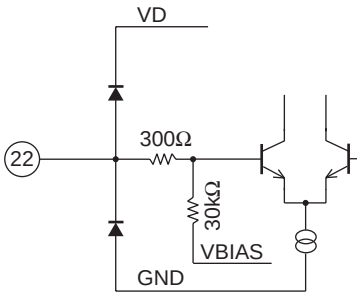
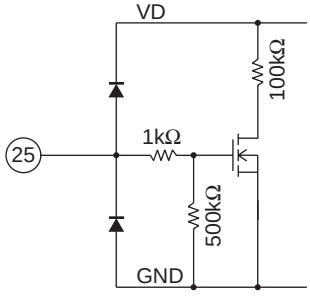
Pin No.	Pin	I/O	Description	Equivalent Circuit
14	$V_{DD}2$	O	Internal power supply decoupling capacitor connection	
15	BOOT2+	I/O	Bootstrap I/O pin, channel 2 power supply low side	
16	OUT2+	O	Channel 2 high side output	
17	PVD2		Channel 2 power system power supply	
18	PVD2		Channel 2 power system power supply	
19	NC		No connection	
20	NC		No connection	
21	$V_{IN}2+$	I	Channel 2 noninverting inputt	
22	$V_{IN}2-$	I	Channel 2 inverting input	
23	NC		No connection	
24	NC		No connection	
25	$\overline{\text{MUTE}}$	I	Muting control	

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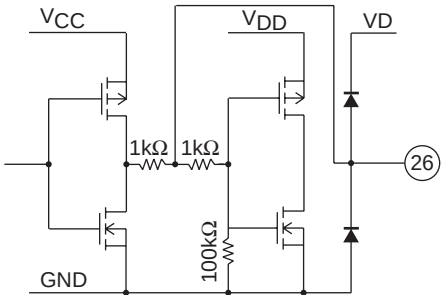
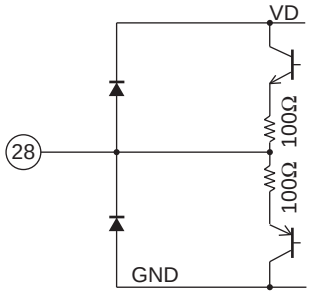
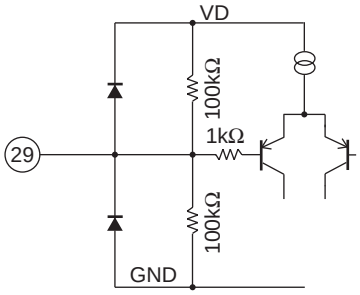
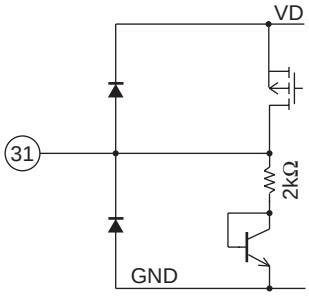
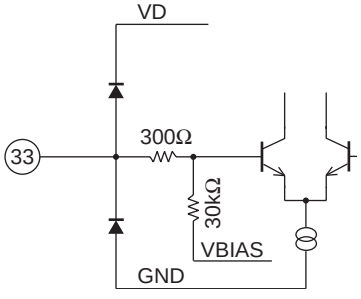
Pin No.	Pin	I/O	Description	Equivalent Circuit
26	MUTECAP	O	Muting system capacitor connection	
27	GND		Analog system ground	
28	VBIAS	O	Internal power supply decoupling capacitor connection	
29	BIASCAP	O	Internal power supply decoupling capacitor connection	
30	NC		No connection	
31	V_{CC}	O	Internal power supply decoupling capacitor connection	
32	NC		No connection	
33	$V_{IN}1-$	I	Channel 1 inverting input	

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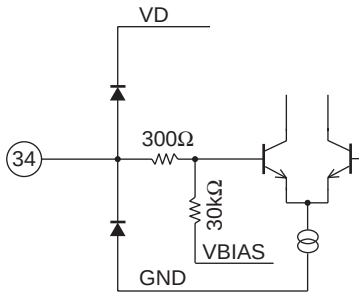
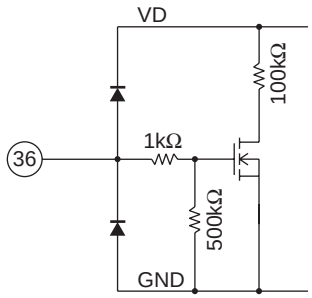
Pin No.	Pin	I/O	Description	Equivalent Circuit
34	$V_{IN}1+$	I	Channel 1 noninverting input	
35	NC		No connection	
36	$\overline{STBY}$	I	Standby mode control	

Note: Smoothing capacitors must be connected to each power supply pin.

Functional Descriptions

System Standby

The bias levels are turned on and off under control of the high/low state of the STBY pin. When the STBY pin is low, the bias levels will be turned off, and when that pin is high, the bias levels will be applied.

Mute Function

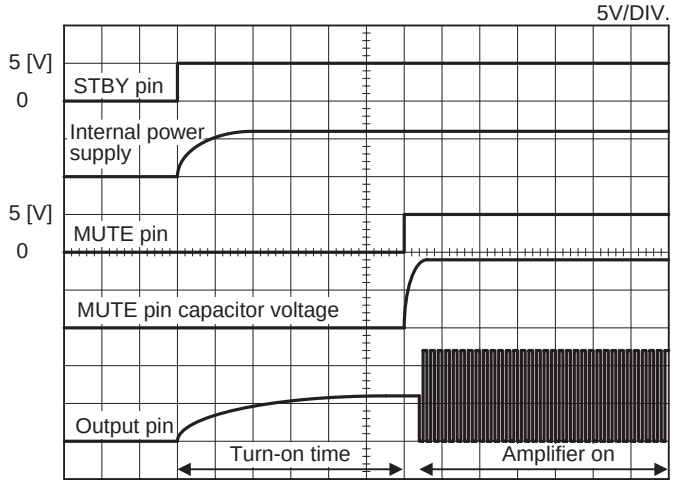
The mute function is provided mainly to mute the output so that impulse noise will not appear in the output when the power supply is being turned on.

(1) Output Muting

The output PWM signal can be turned on or off by setting the MUTE pin high or low. When the MUTE pin is low, the internal oscillator is stopped. This oscillator operates at all times that the MUTE pin is high.

(2) Power On Sequence

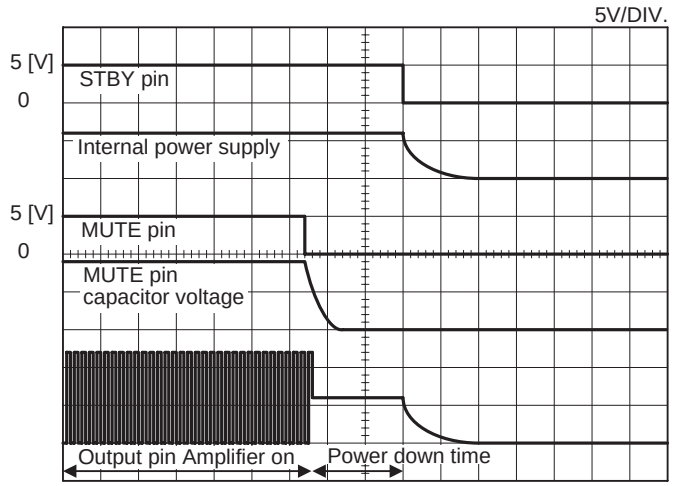
Applications should provide a power-on muting period of at least 500ms to minimize impulse noise.



Turn-on time: the time between the point the STBY pin is set high and the point the MUTE pin is set high.

(3) Power Down Sequence

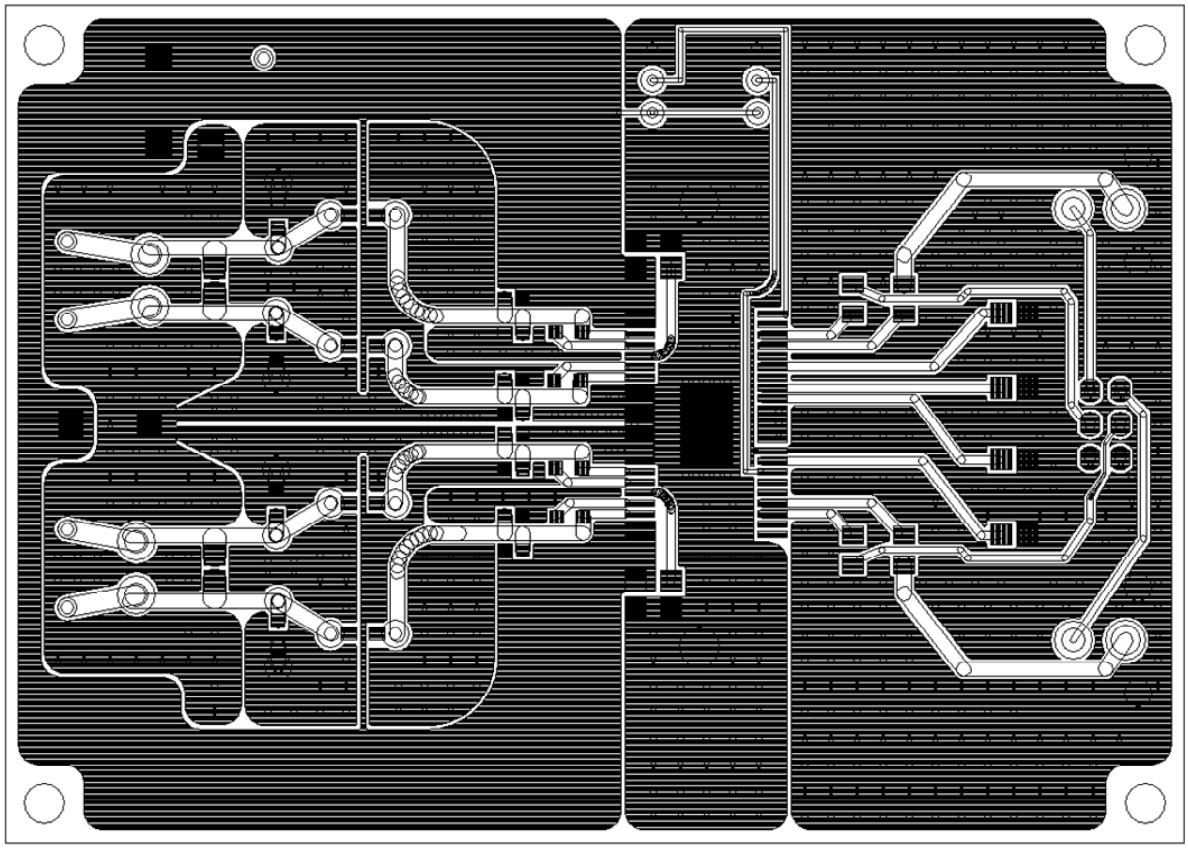
Applications should provide a power down muting period of at least 100ms to minimize impulse noise.



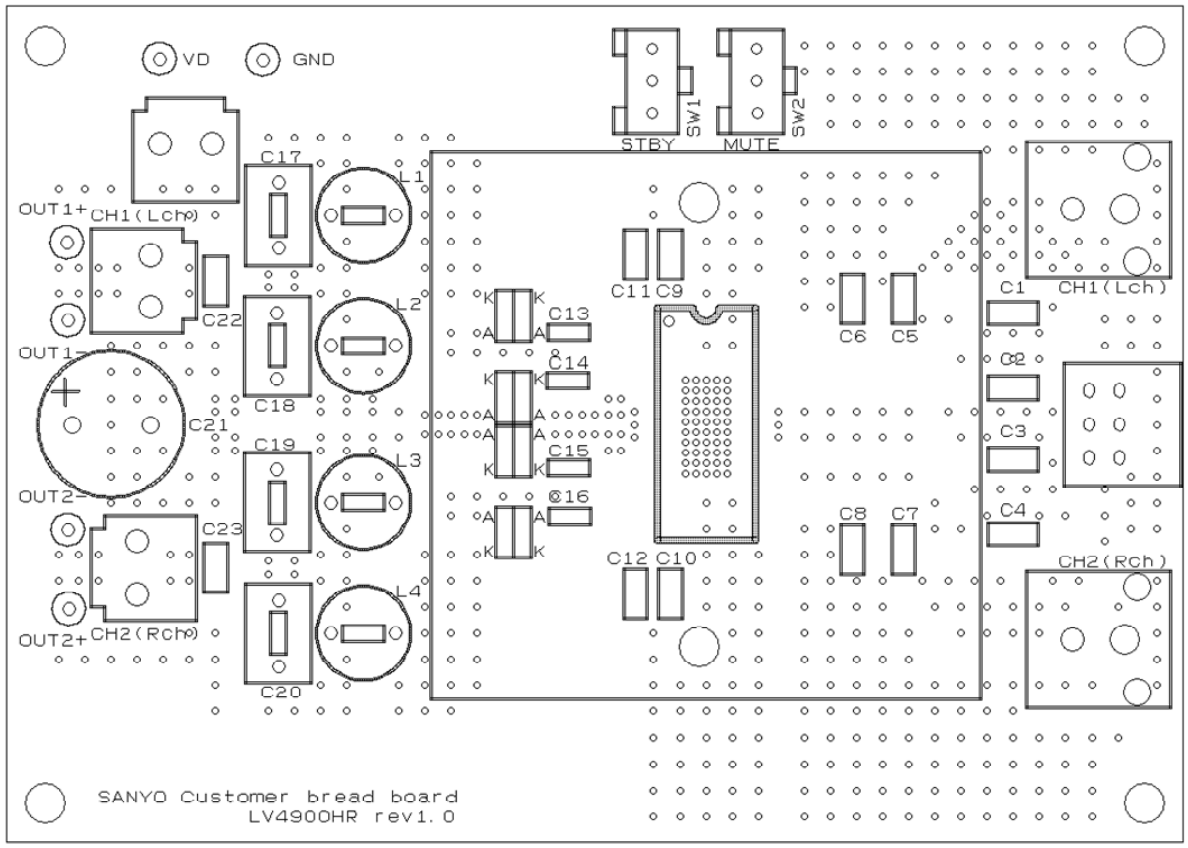
Turn-off time: the time between the point the MUTE pin is set low and the point the STBY pin is set low.

LV4900H customer bread board rev.1.0

Pattern



Silk

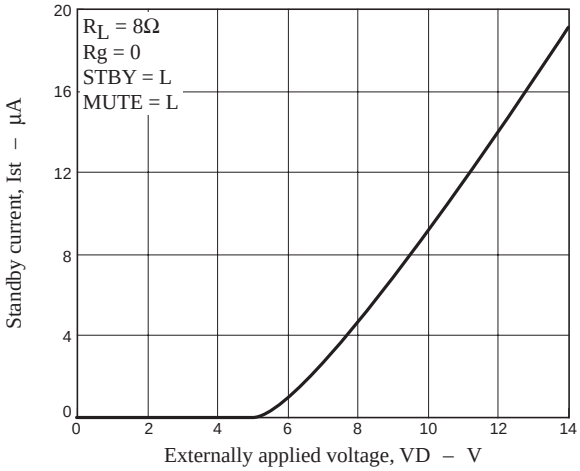


Components

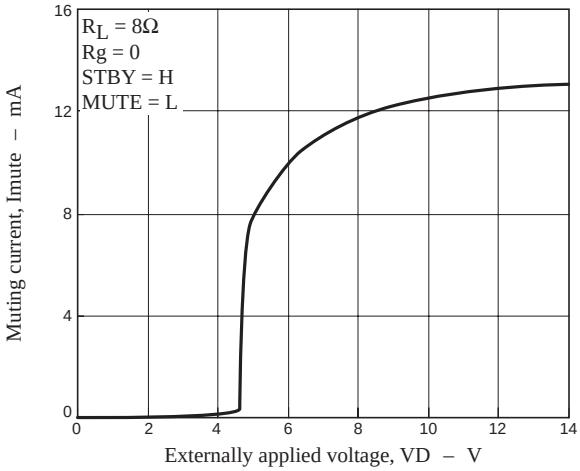
	Symbol	Part No.	Function
	-----	SW1	Standby switch. Lower position: standby state
	-----	SW2	Mute switch. Lower position: mute state
	C_{VCC}	C1	Internal power supply (V_{CC}) output coupling capacitor
	$C_{BIASCAP}$	C2	Internal power supply (VBIAS) input coupling capacitor
	C_{VBIAS}	C3	Internal power supply (VBIAS) output coupling capacitor
	C_{MUTE}	C4	Soft muting time constant adjustment capacitor
	C_{IN}	C5, C6, C7, C8	Input capacitors
*	C_{VDD}	C9, C10	Internal power supply (V_{DD}) output coupling capacitors
*	C_{VD}	C11, C12	VD high-frequency attenuation capacitors
*	C_{BOOT}	C13, C14, C15, C16	Bootstrap capacitor
	L_O	L1, L2, L3, L4	Output low-pass filter coils: fc = 1/ ($2\pi\sqrt{LoCo}$)
	C_O	C17, C18, C19, C20	Output low-pass filter capacitors
	C_{VD}	C21	VD power supply capacitors
	C_{OUT}	C22, C23	Output for capacitors

* C_{VDD}, C_{VD} and C_{BOOT}, Each capacitor is arranged in the neighborhood of IC as much as possible.

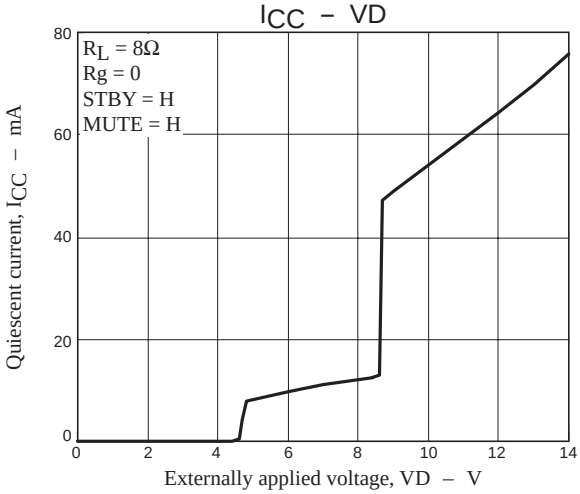
Ist – VD



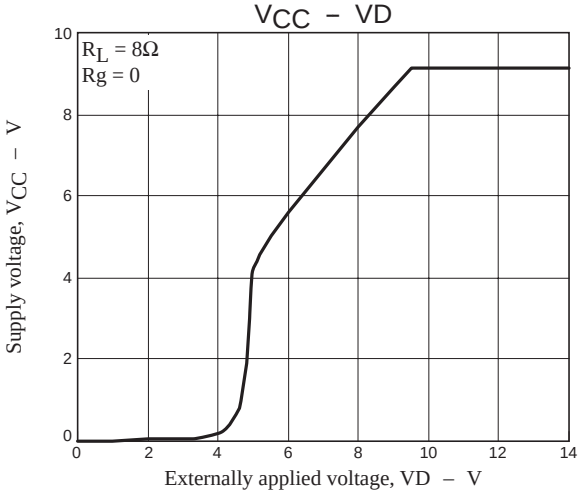
Imute – VD



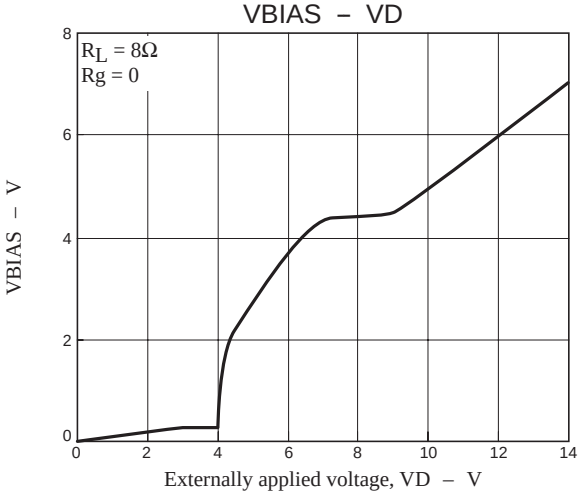
ICC – VD



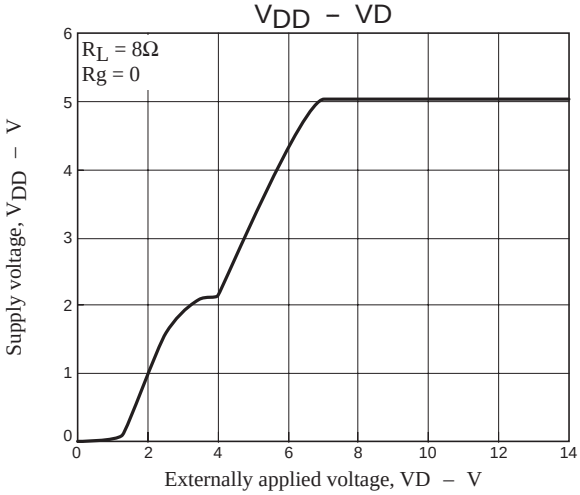
VCC – VD



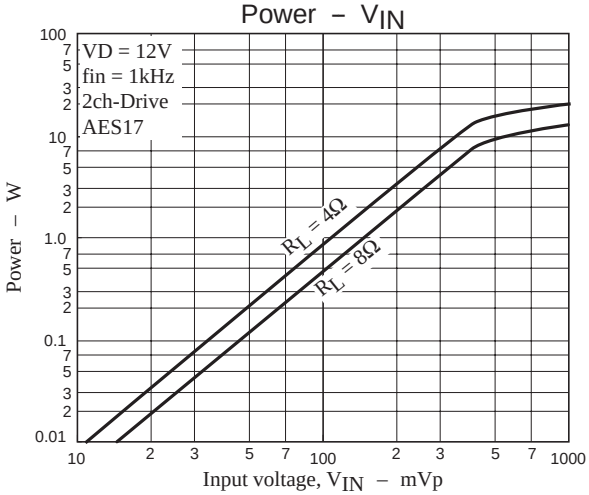
VBIAS – VD



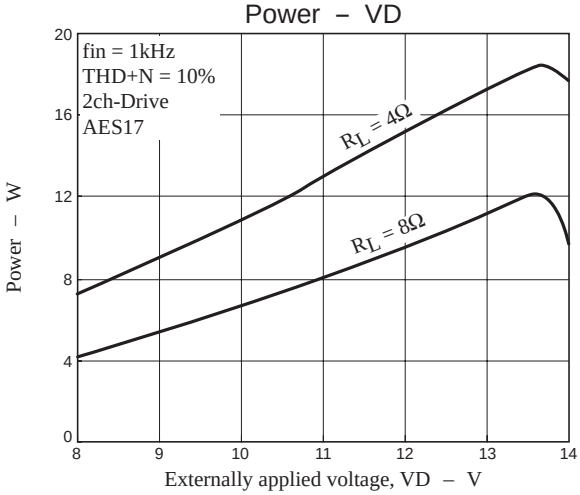
VDD – VD



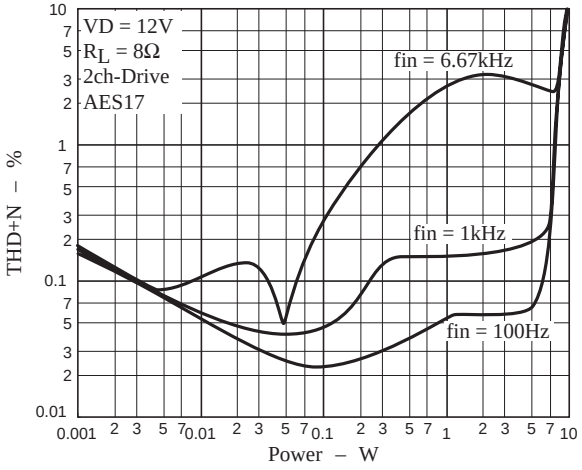
Power – VIN



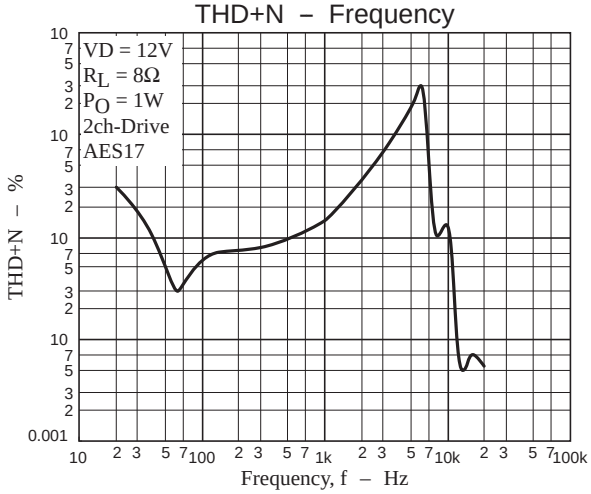
Power – VD



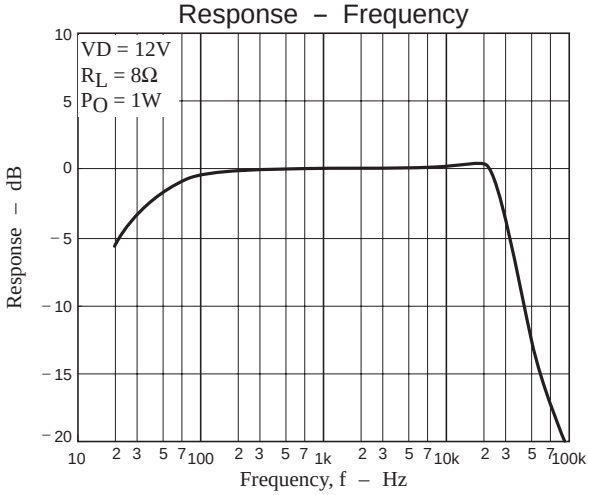
THD+N – Power



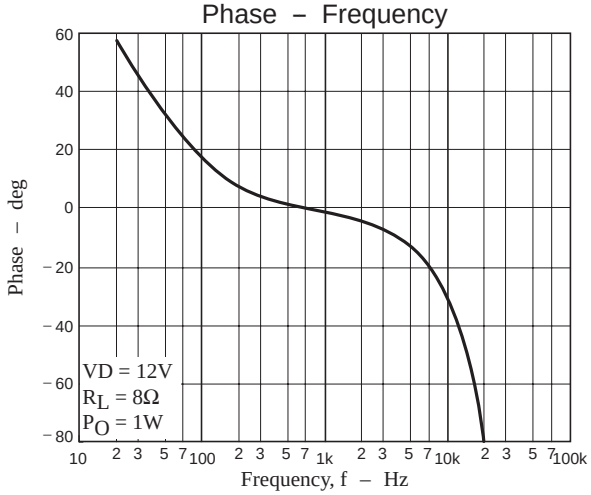
THD+N – Frequency



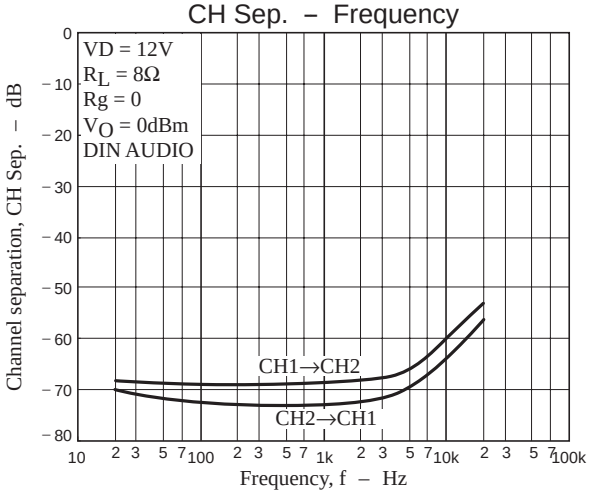
Response – Frequency



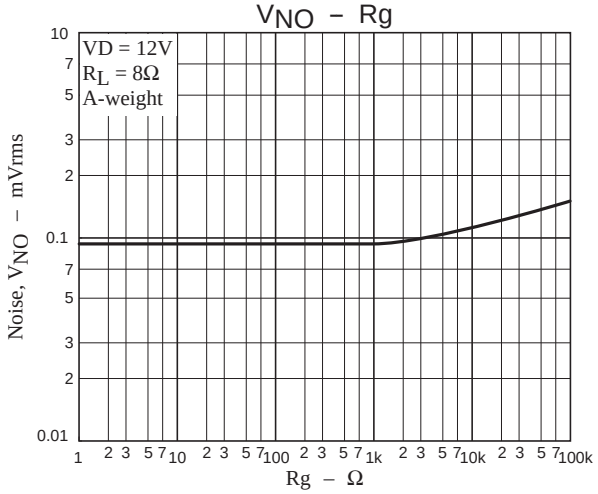
Phase – Frequency



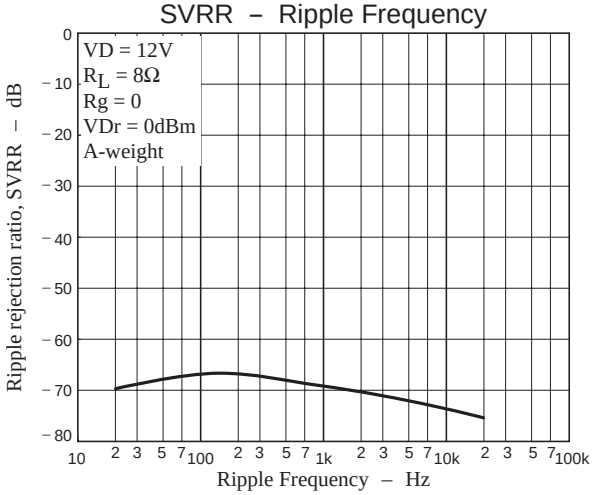
CH Sep. – Frequency



V_{NO} – Rg



SVRR – Ripple Frequency



Efficiency – Power