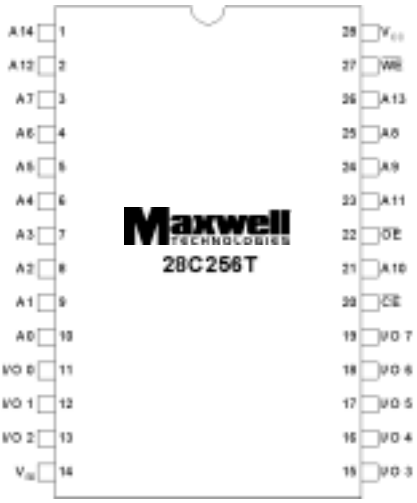
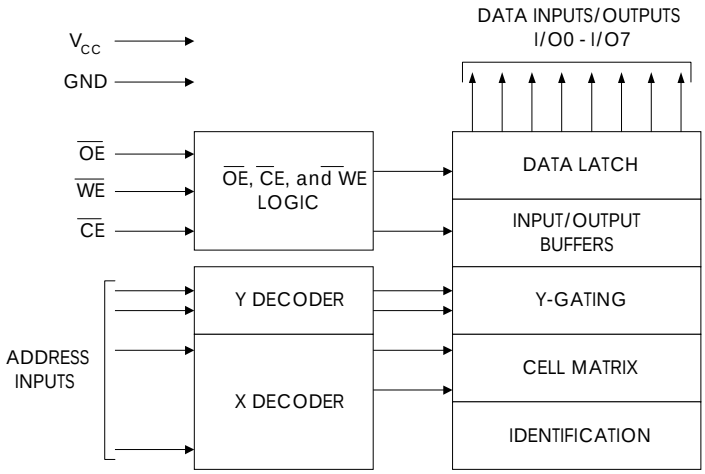
28C256T
256K EEPROM (32K x 8-Bit) EEPROM





Logic Diagram

FEATURES:

- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness:
  - > 100 Krad (Si), dependent upon space mission
- Excellent Single Event Effects:
  - SEL_{TH} LET: > 120 MeV/mg/cm^2
  - SEU_{TH} LET (read mode): > 90 MeV/mg/cm^2
  - SEU_{TH} LET (write mode): > 18 MeV/mg/cm^2
- Package:
  - 28 pin RAD-PAK® flat pack
  - 28 pin RAD-PAK® DIP
  - JEDEC approved byte wide pinout
- High Speed:
  - 120, 150 ns maximum access times available
- High endurance:
  - 10,000 erase/write (in Page Mode), 10-year data retention
- Page Write Mode:
  - 1 to 64 bytes
- Low power dissipation:
  - 15 mA active current (cycle = 1 µs)
  - 20 µA standby current ($\overline{CE}$ = V_{CC})

DESCRIPTION:

Maxwell Technologies' 28C256T high density 256k-bit EEPROM microcircuit features a greater than 100 krad (Si) total dose tolerance, depending upon space mission. The 28C256T is capable of in-system electrical byte and page programmability. It has a 64-Byte page programming function to make its erase and write operations faster. It also features data polling to indicate the completion of erase and programming operations.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

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TABLE 1. 28C256T PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
*10-3, 25, 24, 21, 23, 2, 26, 1	A0-A14	Address
11-13, 15-19	I/O0-I/O7	Input/Output
22	$\overline{OE}$	Output Enable
20	$\overline{CE}$	Chip Enable
27	$\overline{WE}$	Write Enable
28	V_{CC}	Power Supply
14	V_{SS}	Ground

*Refer to diagram on Page 1 for pin relationship.

TABLE 2. 28C256T ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage (Relative to V_{SS})	V_{CC}	-0.6	7.0	V
Input Voltage (Relative to V_{SS})	V_{IN}	-0.5[1]	7.0	V
Operating Temperature Range[2]	T_{OPR}	-55	125	˚C
Storage Temperature Range	T_{STG}	-65	150	˚C

1. V_{IN} = -3.0 V for pulse width $\geq$ 50 ns.
2. Including electrical characteristics and data retention.

TABLE 3. 28C256T DELTA LIMITS

PARAMETER	VARIATION
$I_{CC}1$	±10%
$I_{CC}2$	±10%
$I_{CC}3A$	±10%
$I_{CC}3B$	±10%

TABLE 4. 28C256T RECOMMENDED OPERATING CONDITIONS

PARAMETER	SUBGROUPS	SYMBOL	MIN	MAX	UNITS
Supply Voltage	1	V_{CC}	4.5	5.5	V
Input Voltage	1	V_{IL}	-0.3[1]	0.8	V
	1	V_{IH}	2.2	V_{CC} +0.3	V
	1	V_H	V_{CC} -0.5	V_{CC} +1	V
Thermal Impedance — Flat Package	1	Θ_{JC}	--	0.87	°C/W
Thermal Impedance — DIP Package	1	Θ_{JC}	--	0.86	°C/W
Operating Temperature Range	1	T_{OPR}	-55	125	˚C

1. V_{IL} min= -1.0V for pulse width ≤ 50 ns.

TABLE 5. 28C256T CAPACITANCE[1]

(T_A = 25 ˚C, f = 1 MHz)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance: V_{IN} = 0V [1]	C_{IN}	--	6	pF
Output Capacitance: V_{OUT} = 0V [1]	C_{OUT}	--	12	pF

1. Guaranteed by design.

TABLE 6. 28C256T DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5 V ± 10%, T_A = -55 TO +125 ˚C UNLESS OTHERWISE SPECIFIED)

PARAMETER	CONDITIONS	SUBGROUPS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V	1, 2, 3	I_{LI}	--	2	uA
Output Leakage Current	V_{CC} = 5.5 V, V_{OUT} = 5.5 V/0.4 V	1, 2, 3	I_{LO}	--	2	uA
Standby V_{CC} Current	$\overline{CE}$ = V_{CC}	1, 2, 3	I_{CC1}	--	20	uA
	$\overline{CE}$ = V_{IH}	1, 2, 3	I_{CC2}	--	1	mA
Operating V_{CC} Current	I_{OUT} = 0 mA Duty = 100% V_{CC} = 5.5 V Cycle = 1 us	1, 2, 3	I_{CC3}	--	15	mA
	I_{OUT} = 0mA Duty = 100% V_{CC} = 5.5 V Cycle = 150 ns			--	50	
Input Low Voltage		1, 2, 3	V_{IL}	--	0.8	V
Input High Voltage		1, 2, 3	V_{IH}	2.2	--	V
		1, 2, 3	V_H	V_{CC} -0.5	--	V
Output Low Voltage	I_{LO} = 2.1 mA	1, 2, 3	V_{OL}	--	0.4	V
Output High Voltage	I_{OH} = -400 uA	1, 2, 3	V_{OH}	2.4	--	V

TABLE 7. 28C256T AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION[1]

(V_{CC} = 5V ±10%, T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	SYMBOL	MIN	MAX	UNITS
Address Access Time $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	9, 10, 11	t_{ACC}			ns
-120			--	120	
-150			--	150	
$\overline{CE}$ to Output Delay $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	9, 10, 11	t_{CE}			ns
-120			--	120	
-150			--	150	
$\overline{OE}$ to Output Delay $\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	9, 10, 11	t_{OE}			ns
-120			0	75	
-150			0	75	
Output Hold from Address $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	9, 10, 11	t_{OH}			ns
-120			0	--	
-150			0	--	
$\overline{OE}$ ($\overline{CE}$) High to Output Float $\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH} [2]	9, 10, 11	t_{DF}			ns
-120			0	50	
-150			0	50	

1. Test conditions: Input pulse levels - 0V to 3V; input rise and fall times < 20 ns; output load - 1 TTL gate + 100 pF (including scope and jig); reference levels for measuring timing - 0.8V/1.8V.

2. t_{DF} and t_{DFR} are defined as the time at which the output becomes an open circuit and data is no longer driven.

TABLE 8. 28C256T AC ELECTRICAL CHARACTERISTICS FOR PAGE/BYTE ERASE AND WRITE OPERATIONS

(V_{CC} = 5V ±10%, T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	SYMBOL	MIN[1]	TYP	MAX	UNITS
Address Setup Time		t_{AS}				ns
-120	9, 10, 11		0	--	--	
-150	9, 10, 11		0	--	--	
$\overline{CE}$ to Write Setup Time		t_{CS} [2]				ns
-120	9, 10, 11		0	--	--	
-150	9, 10, 11		0	--	--	
$\overline{WE}$ to Write Setup Time		t_{WS} [3]				ns
-120	9, 10, 11		0	--	--	
-150	9, 10, 11		0	--	--	
$\overline{WE}$ Hold Time	9, 10, 11	t_{WH} [3]				ns
-120			0		--	
-150			0		--	

TABLE 8. 28C256T AC ELECTRICAL CHARACTERISTICS FOR PAGE/BYTE ERASE AND WRITE OPERATIONS

(V_{CC} = 5V ±10%, T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	SYMBOL	MIN[1]	TYP	MAX	UNITS
$\overline{WE}$ Pulse Width	9, 10, 11	t_{WP}[2]				ns
-120			200	--	--	
-150			250	--	--	
$\overline{CE}$ Pulse Width		t_{CW}[3]				
-120			200	--	--	
-150			250	--	--	
Address Hold Time	9, 10, 11	t_{AH}				ns
-120			150	--	--	
-150			150	--	--	
Data Setup Time	9, 10, 11	t_{DS}				ns
-120			75	--	--	
-150			100	--	--	
Data Hold Time	9, 10, 11	t_{DH}				ns
-120			10	--	--	
-150			10	--	--	
Chip Enable Hold Time[2]	9, 10, 11	t_{CH}				ns
-120			0	--	--	
-150			0	--	--	
Output Enable to Write Setup Time	9, 10, 11	t_{OES}				ns
-120			0	--	--	
-150			0	--	--	
Output Enable Hold Time	9, 10, 11	t_{OEH}				ns
-120			0	--	--	
-150			0	--	--	
Data Latch Time[4]	9, 10, 11	t_{DL}				ns
-120			--	230	--	
-150			--	280	--	
Write Cycle Time	9, 10, 11	t_{WC}				ms
-120			--	--	10	
-150			--	--	10	
Byte Load Window[4]	9, 10, 11	t_{BL}				us
-120			--	100	--	
-150			--	100	--	
Byte Load Cycle[4]	9, 10, 11	t_{BLC}				us
-120			0.55	--	30	
-150			0.55	--	30	
Write Start Time	9, 10, 11	t_{DW}				ns
-120			150	--	--	
-150			150	--	--	

1. Use this device in a longer cycle than this value.
2. $\overline{WE}$ controlled operation.
3. $\overline{CE}$ controlled operation.
4. Not tested.

TABLE 9. 28C256T MODE SELECTION [1]

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Write	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_H	X	X	HIGH-Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Deselect	V_{IL}	V_{IH}	V_{IH}	HIGH-Z
Write Inhibit	X	X	V_{IH}	--
	X	V_{IL}	X	--
$\overline{Data}$\ Polling	V_{IL}	V_{IL}	V_{IH}	DATA-OUT (I/O7)

1. X = Does not matter.

FIGURE 1. READ TIMING WAVEFORM

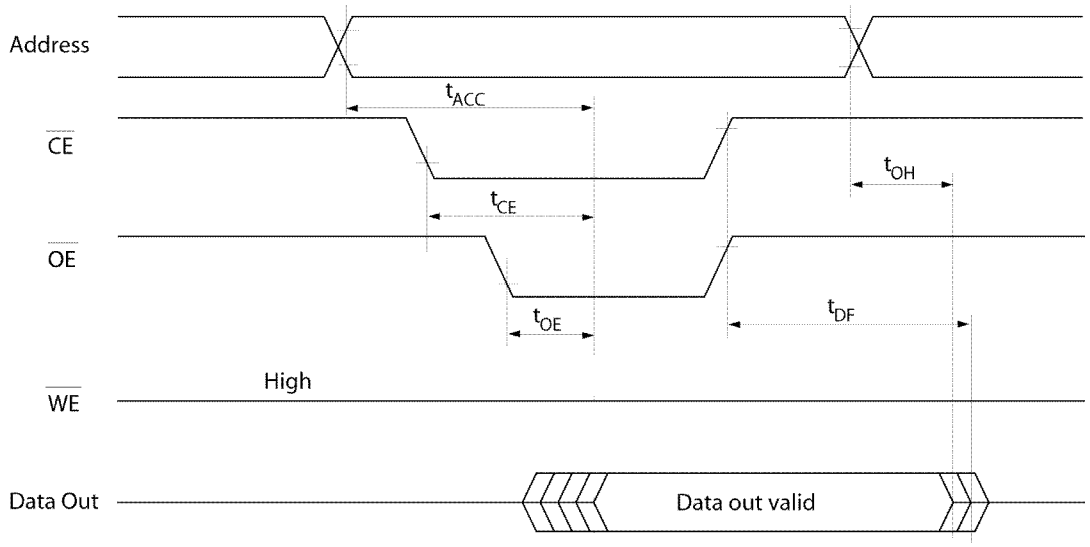


FIGURE 2. BYTE WRITE TIMING WAVEFORM (1) ($\overline{WE}$ CONTROLLED)

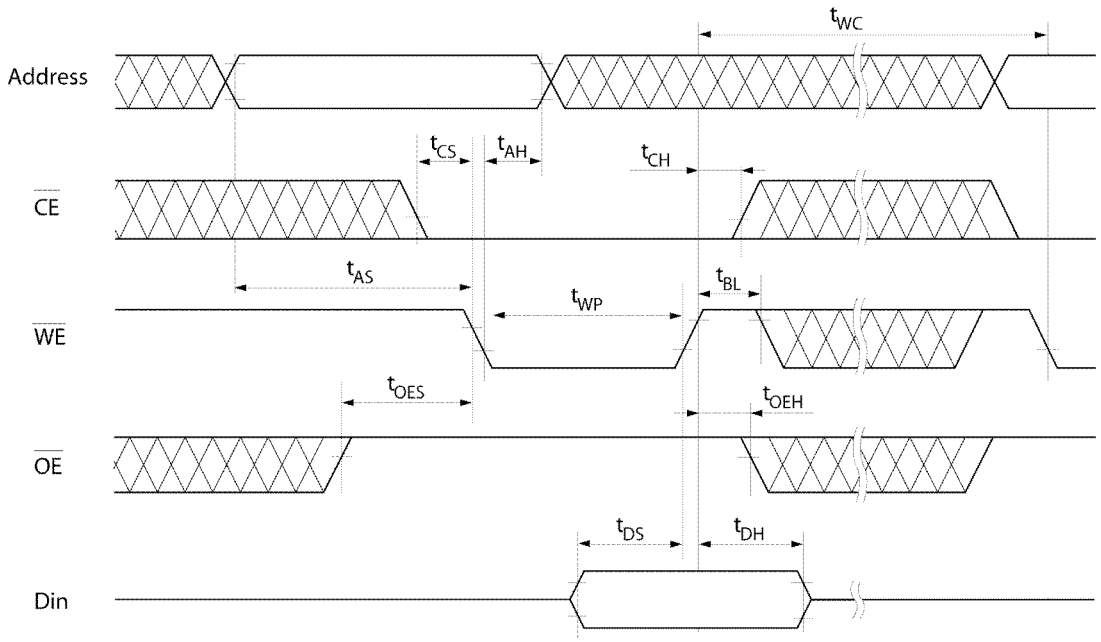


FIGURE 3. BYTE WRITE TIMING WAVEFORM (2) ($\overline{CE}$ CONTROLLED)

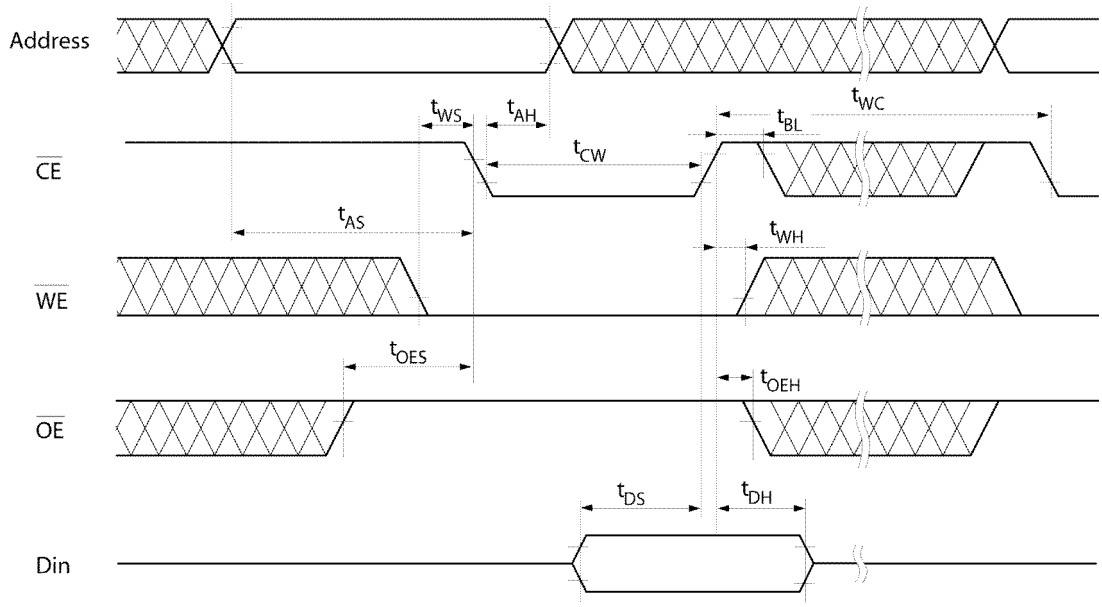


FIGURE 4. PAGE WRITE TIMING WAVEFORM (1) ($\overline{WE}$ CONTROLLED)

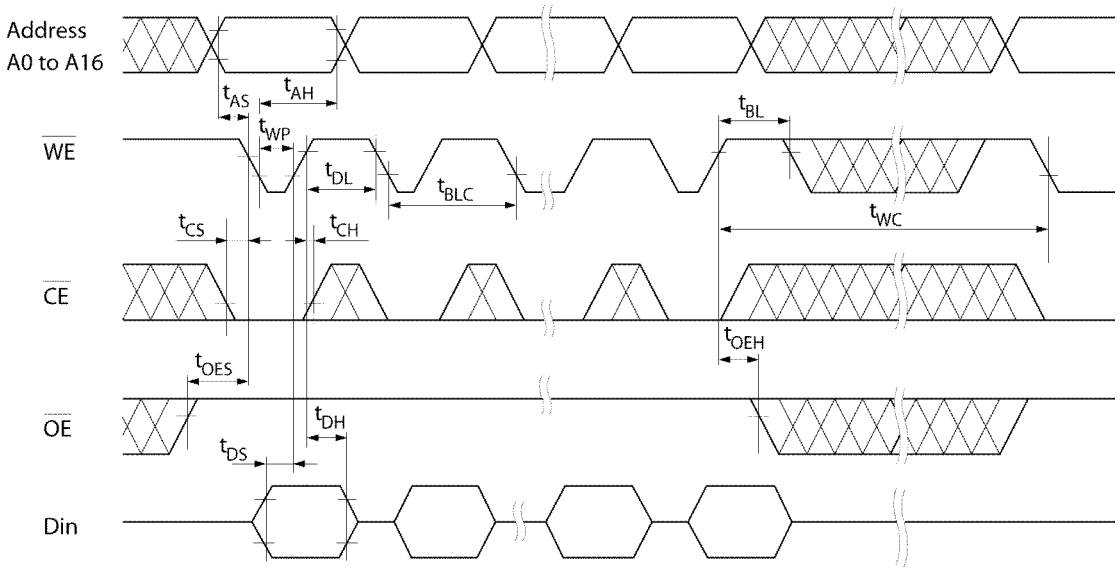


FIGURE 5. PAGE WRITE TIMING WAVEFORM (2) ($\overline{CE}$ CONTROLLED)

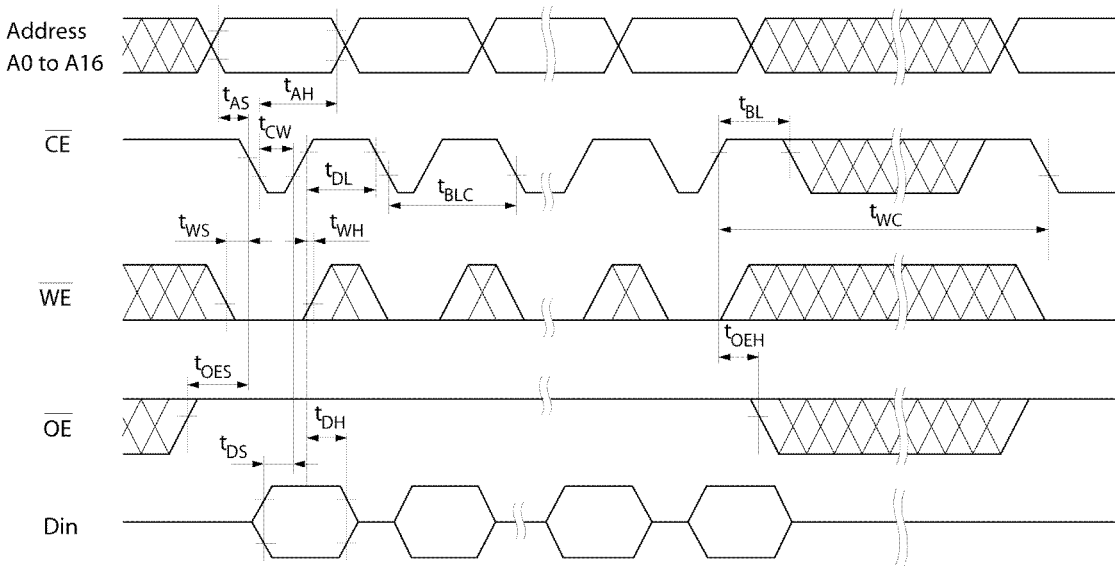
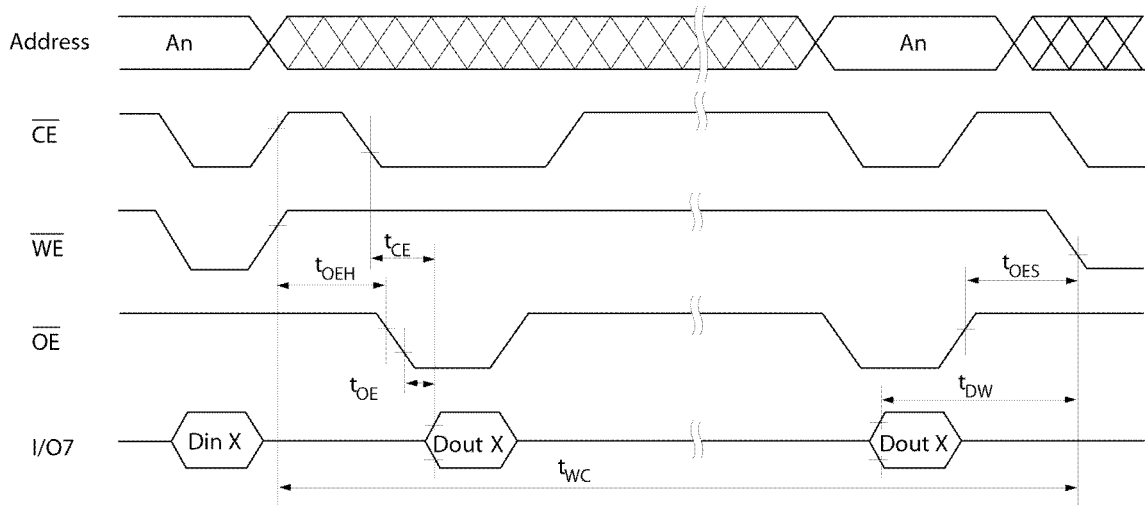


FIGURE 6. $\overline{DATA}$ POLLING TIMING WAVEFORM



EEPROM Application Notes

This application note describes the programming procedures for the EEPROM modules and the details of various techniques to preserve data protection.

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle, and allows the undefined data within 64 bytes to be written corresponding to the undefined address (A0 to A5). Loading the first byte of data, the data load window opens 30 µs for the second byte. In the same manner each additional byte of data can be loaded within 30 µs. In case $\overline{CE}$ and $\overline{WE}$ are kept high for 100(s after data input, EEPROM enters erase and write mode automatically and only the input data are written into the EEPROM.

$\overline{WE}$ $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

$\overline{Data}$ Polling

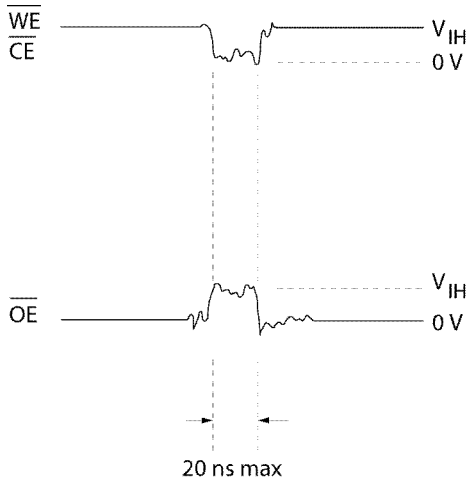
$\overline{Data}$ Polling function allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O 7 to indicate that the EEPROM is performing a write operation.

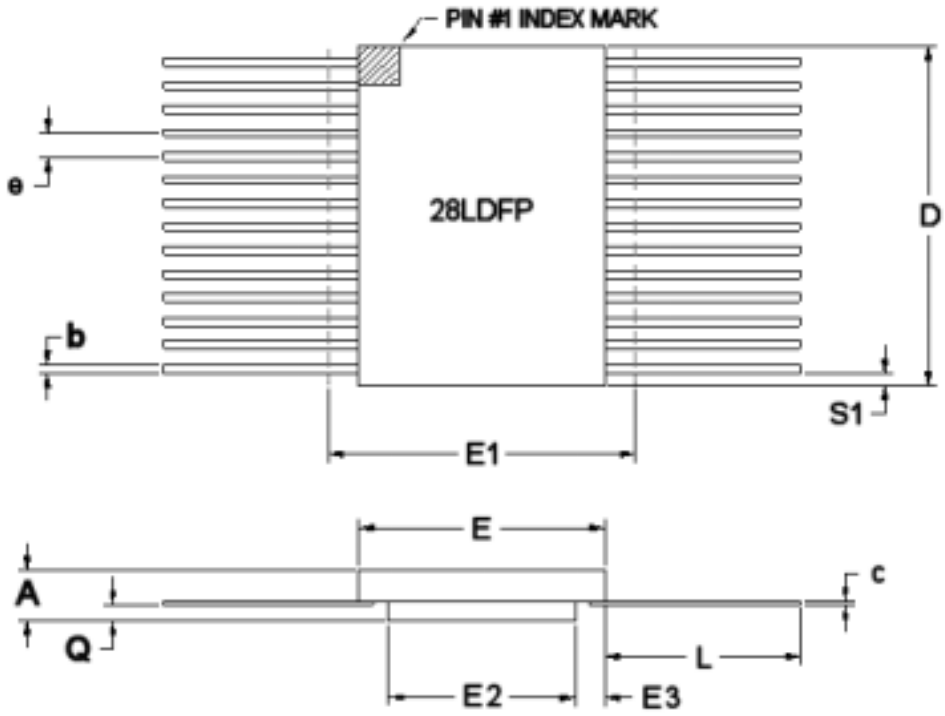
Data Protection

To protect the data during operation and power on/off, the EEPROM has the internal functions described below.

1. Data Protection against Noise of Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.

   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the EEPROM has a noise cancellation function that cuts noise if its width is 20ns or less in programming mode. Be careful not to allow noise of a width of more than 20ns on the control pins.

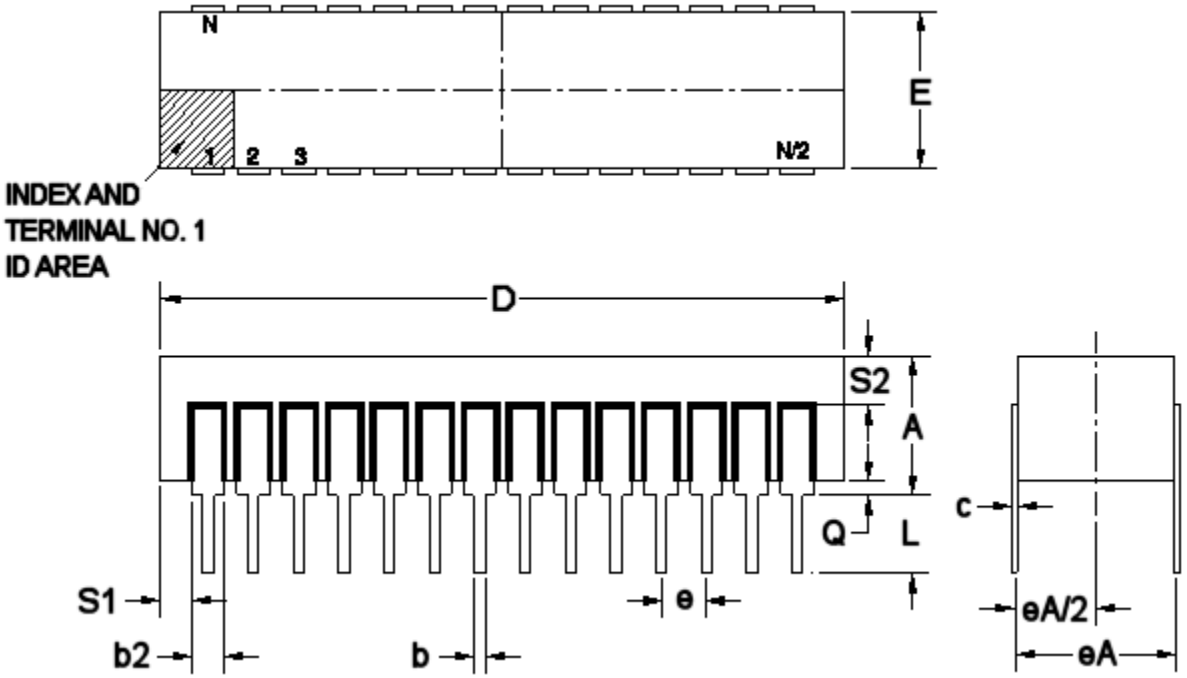




28 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.165	0.177	0.189
b	0.015	0.017	0.022
c	0.003	0.005	0.009
D	--	0.720	0.740
E	0.380	0.410	0.420
E1	--	--	0.440
E2	0.180	0.240	--
E3	0.030	0.085	--
e	0.050 BSC		
L	0.390	0.400	0.410
Q	0.040	0.050	0.053
S1	0.005	0.027	--
N	28		

F28-03
Note: All dimensions in inches.



28 PIN RAD-PAK® DUAL IN LINE PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	--	0.177	0.225
b	0.014	0.018	0.026
b2	0.045	0.050	0.065
c	0.008	0.010	0.018
D	--	1.400	1.485
E	0.510	0.595	0.620
eA	0.600 BSC		
eA/2	0.300 BSC		
e	0.100 BSC		
L	0.140	0.150	0.160
Q	0.015	0.040	0.060
S1	0.005	0.025	--
S2	0.005	--	--
N	28		

D28-03
Note: All dimensions in inches.

Important Notice:

These data sheets are created using the chip manufacturer's published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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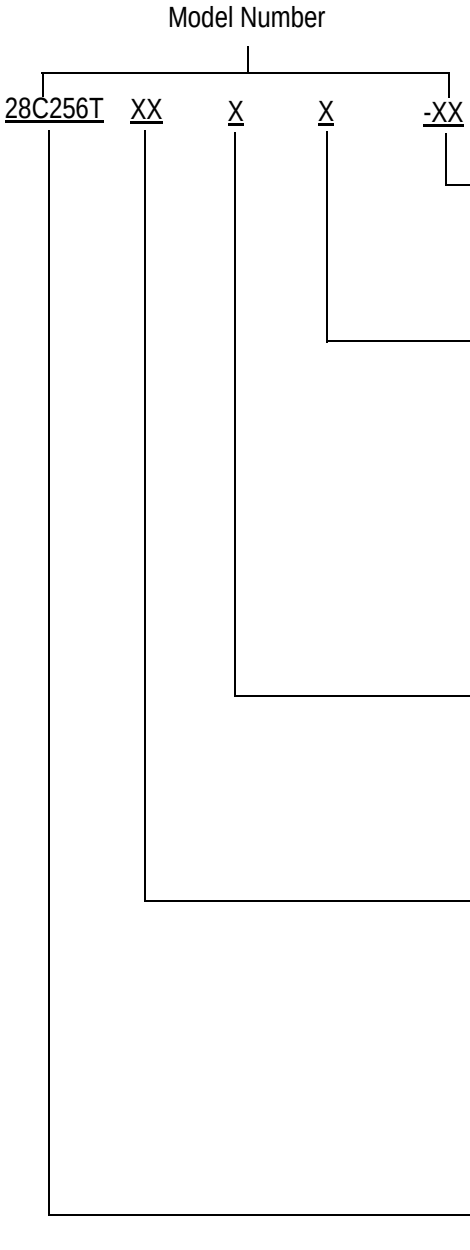
Product Ordering Options



Feature	Option Details
Access Time	12 = 120 ns 15 = 150 ns
Screening Flow	Monolithic S = Maxwell Class S B = Maxwell Class B E = Engineering (testing @ +25°C) I = Industrial (testing @ -55°C, +25°C, +125°C)
Package	D = Dual In-line Package (DIP) F = Flat Pack
Radiation Feature	RP = RAD-PAK® package RT1 = Guaranteed to 10 krad at die level RT2 = Guaranteed to 25 krad at die level RT4 = Guaranteed to 40 krad at die level
Base Product Nomenclature	256K EEPROM (32K x 8-Bit) EEPROM